



Serving the San Francisco, Oakland-East Bay, and Santa Clara Valley Sections of the IEEE For an online version of this Council announcement, with active links, visit www.e-grid.net/announcements/grid0412a.html

[Upcoming Chapter Meetings](#) - summaries

[SJSU Short Courses: VHDL, DSP, Sensors, Device Physics](#)

[Transition to Manager, Thermal Design](#) courses

[Intelligent Control & Soft Computing](#) course

[Subscribe](#)

Download the new [December GRID.pdf](#) (225 kB) Select an opportunity to learn about new developments, master a new skill, and network with fellow professionals. Check for updated information during the month at our [GRID](#) website: www.e-grid.net/

Chapter Meetings for December:

SCV-Ed - 12/1: **Engineering Innovation for the 21st Century** - an educational perspective related to information technology, biotechnology and nanotechnology ... [\[more\]](#)

SCV-CS - 12/2: **Recent Developments in Nanotechnology: An Overview** - Shannon Lecture Series -- novel nanomaterials such as carbon nanotubes and inorganic nanowires and ongoing key developments ... [\[more\]](#)

SCV-LEOS - 12/7: **How to Improve Your Image: It Ain't Magic ... or is it?** - the interesting, subtle and revealing aspects of optical system design, both science and art ... [\[more\]](#)

SCV-CPMT - 12/8: **Replacing Heat Sinks with Thermally Conductive Substrates -- Technology and Tradeoffs** - advantages and applications of substrate constructions that eliminate the need for heat sinks ... [\[more\]](#)

SCV-COM - 12/8: **A Cellular Wi-Fi Mesh Network for Broadband Data** - combining the best features of cellular and Wi-Fi technologies with mesh networking protocols for metro-scale applications ... [\[more\]](#)

SCV-EMS - 12/8: **From Engineer to Entrepreneur and A Sports Analogy for Managing Personal and Team Performance** - views from a technology incubator ... the similarities which translate into higher personal and team performance ... [\[more\]](#)

SCV-MTT - 12/9: **Surface-Mount 2 GHz 30W Power Amplifiers Blend Thick-Film Hybrid and Chip-and-Wire Technology for Communications Infrastructure Applications** - low-cost hybrid PA modules with aggressive performance requirements ... [\[more\]](#)

SCV-SP - 12/13: **Reconfigurable Systems Emerge** - new programmable logic devices based on next-generation non-volatile memory will enable efficient reconfigurable systems ... [\[more\]](#)

SCV-CNSV - 12/13 & 12/27: **Entrepreneurs SIG** - this SIG is part of the Consultants' Network of Silicon Valley, and meets on second and fourth Mondays ... [\[more\]](#)

SCV-CNSV - 12/14: **Taxes and Their Changes in 2005 for Independent Consultants** - recent changes to the tax laws, choice of "S" Corporation status and other issues plus questions and answers on tax or financial topics ... [\[more\]](#)

The Council Marketplace

Do you require someone with special skills -- RF, reliability, project planning, communications, design, patent consultations? ... PCB layout, thermal measurements, SCSI, SANs? See our [Council Marketplace](#) page. Thank you for supporting our advertisers.

IEEE Press - John Wiley

John Wiley is the publishing partner of the IEEE, and many of their books are co-branded by IEEE Press. The SF Bay Area Council's agreement with Wiley grants us a commission on each book that is purchased through one of our "referral" links. So a reminder: when you're shopping for technical or business books (for yourself, or as gifts), don't forget that you can benefit your Council (and its Chapters) by starting your search from the GRID home page (and clicking on any of the "Wiley" graphics or links) -- or from the link above.

SJSU Department of Electrical Engineering: Winter Short Courses

Digital Signal Processing -- 4-day class with labs:

DSP System Design and Implementation [\[more\]](#)

Date/Time: January 18-21, 8:30AM-4:30PM

Instructor: Professor Avtar Singh, Electrical Engineering, SJSU

Location: San Jose State campus

Overview: Today's technology provides DSP processors that can be easily used to design very sophisticated products for instrumentation, control, communications, and wireless systems. This course presents DSP system design and implementation using programmable signal processors. Hands-on laboratory exercises are used to present the design and implementation aspects, using hardware and software tools for system implementation. The 5 laboratory sessions allow participants to apply system design concepts by designing, implementing, debugging and evaluating DSP schemes.

Digital System Design -- 4-day class with labs:

FPGA DSP System Design [\[more\]](#)

Date/Time: January 18-21, 8:30AM-4:30PM

Instructor: Professor Chen Choo, Electrical Engineering, SJSU

Location: San Jose State campus

Overview: This course provides an in-depth and state-of-the-art coverage of the design and FPGA-based implementation of high-performance DSP systems. After presenting FPGA architectures and design tools by Xilinx and Altera, several hands-on design labs on DSP, digital communications and video/imaging will be covered, including FFT, FIR filters, error detection/correction circuits, modem, color space converter, and DWT (Discrete Wavelet Transform). Contents: Basic DSP/Communication theory, HDL (VHDL and Verilog), DSP-specific arithmetic circuits, hardware design of digital filters, FFT circuits, error detection & correction circuits, encryption/decryption circuits, and video/imaging circuits.

Digital Design -- 4-day class with labs:

VHDL for Synthesis and Verification [\[more\]](#)

Date/Time: January 18-21, 8:30AM-4:30PM

Instructor: Professor Tri Caohuu, Electrical Engineering, SJSU

Location: San Jose State campus

Overview: An in-depth study of VHDL methodologies, coding styles and design techniques used to efficiently synthesize and test digital hardware (ASICs and FPGAs), then VHDL structures and simulation, and finally test-bench and verification. Synthesis topics focus on mapping digital hardware structures to vendor-independent VHDL code, with do's and don'ts of coding styles. The Laboratory runs Synopsys's Design Analyzer and Design Compiler and Xilinx's ISE for design, synthesis and verification of a non-trivial digital subsystem with bus and control signals. Students start with simple test benches, progressively increase the level of abstraction, learn how to correctly model and abstract behavior. The final result is a transaction-based, system-level, self-checking test environment.

Microelectronic Device & Technology -- 4-day class:

Device Physics and VLSI Technology [\[more\]](#)

Date/Time: January 18-21, 8:30AM-4:30PM

Instructor: Professor Lili He, Electrical Engineering, SJSU

Location: San Jose State campus

Overview: This course presents an introduction to the basic concepts of microelectronic structures, from the PN junction to BJT and MOSFET devices. The physics of device performance is discussed in some detail. Modern device fabrication technology is covered, including fabrication principles for semiconductor devices, crystal growth, epitaxy, lithography, scaling, and etching. Critical technologies in IC fabrication are related to the performance of the resultant devices.

Networking Engineering -- 3-day class:

Sensor Network Technology [\[more\]](#)

Date/Time: January 18-21, 8:30AM-4:30PM

Instructor: Professor Nader F. Mir, Electrical Engineering, SJSU

Location: San Jose State campus

Overview: A sensor network with chemical, biological or solar sensors can be wired or wireless, depending on where and how the sensors are used. The applications of sensor networks can be military or civilian. In the military field (the battlefield of the future, for instance) a network of sensors enables soldiers to see around corners and to sense the threat of chemical and biological weapons long before they get close enough to cause harm. Sensor networks can also be put to civilian uses, such as environmental monitoring, traffic control, and health care monitoring for the elderly to allow more freedom to move about. The course focus is on architectures, protocols, hardware aspects, and other related issues such as scalability, fault-tolerance, and security. A base-station monitors and controls cluster networks and chooses a cluster head (gateway) for each cluster through which the cluster data is collectively routed to the base-station. Sensor networks are constructed with a five-layer protocol stack: physical layer, data link layer and MAC sub-layer, network layer, transport layer, and application layer.

For full class outlines, prerequisites, fees, and lecturer biographies, see the Course Flyer: www.e-grid.net/docs/sjsu.pdf

Circulate within your department.

Short Courses and Seminars for December and beyond:

Transitioning From Individual Contributor to Manager [\[more\]](#)

Date/Time: Thursday, Dec. 9, 8:30AM-4:30PM

Instructor: Dr. Andrew Oravets

Location: Exar Corp, 48720 Kato Rd., Fremont

Fee: \$350 for IEEE Members; \$425 non-members

Overview: The transition from individual contributor to manager can be the most challenging shift of a career. Management demands a deeper appreciation of the impact of one's style and greater flexibility in order to be able to deal with a variety of people. This program is designed to introduce prospective or newly promoted managers in a technical environment to the concepts and skills critical to a successful assumption of leadership.

Full [course description and registration details.](#)

Thermal Design and Modeling of IC Packages [\[more\]](#)

Date/Time: Wednesday, Dec. 15, Noon - 5:00 PM

Instructor: Dr. Sam Z. Zhao

Location: UCSC Extension, 1180 Bordeaux Drive, Sunnyvale

Fee: \$225 for IEEE Members; \$249 non-members

Overview: This short course provides a systematic approach to the understanding of IC package-related thermal issues, thermally enhanced packages, industry standard thermal tests, IC package thermal modeling techniques, and system thermal design using IC package compact and detailed thermal models. Students completing this class gain basic understanding of IC package thermal characteristics, improve their ability and understanding to make appropriate IC package technology selection and system design decisions, and achieve reliable performance of complex electronic devices.

Full [course description and registration details.](#)

Reliability Engineering [\[more\]](#)

Date/Time: 8 Tuesday evenings, Jan 11 - March 1

Instructor: Jurek Zarzycki, CRE, CQE

Location: Santa Clara

Overview: Reliability is a key attribute of the successful and profitable product. Understanding reliability disciplines and metrics and applying them during design, validation, test, and production yields big rewards.

Key Topics: Reliability Management - Probability and Statistics - Modeling and Prediction - Maintainability and Availability - Reliability Testing - Product Safety and Liability

Full [course description and registration details.](#)

Intelligent Control & Soft Computing -- Neural Networks, Fuzzy Logic, Genetic Algorithms [\[more\]](#)

• Dates: February 1-3, 2005

• Location: NASA Research Park, Moffett Field

• Instructors: **Lotfi Zadeh**, Ph.D., UC-Berkeley; **Kevin Passino**, Ph.D., Ohio State Univ; **Hamid Berenji**, Ph.D., IIS Corp.

Traditional (hard) computing methods do not provide sufficient capabilities to develop and implement intelligent systems. Soft Computing is a subfield of artificial intelligence that is tolerant of imprecision, uncertainty, and partial truth. Soft Computing and Computational Intelligence methods have provided important practical tools for constructing intelligent systems.

This course has been presented at several NASA locations including NASA Marshall and NASA Glen as recently as June 2004. At the completion of this course you will have a full understanding of the benefits of intelligent control, neural networks, fuzzy logic inference, and genetic algorithms. You will have learned significant details about their successful applications and you will have developed the necessary knowledge to design and apply these techniques to your particular applications.

Who Should Attend? Engineers, technical managers, project leaders, scientists, system analysts, and others interested in fuzzy logic, neural networks and intelligent systems.

Cost: \$975 (includes class notes and refreshments)

Registration and more information: On the [class website](#)

SUBSCRIBE yourself to this IEEE Council and e-GRID DList

IEEE Members in the San Francisco Bay Area automatically receive this Announcement at their IEEE "email address of record." Members may unsubscribe from (or re-subscribe to) this mailing list at www.ieee.org/ra/e-notice/sfbac-notice.html; be sure to include your IEEE member number. Members wishing to **also** subscribe an alternate email address (eg, Hotmail, or at work), or who live outside the Bay Area, may follow the instructions below.

Technologists who are not members of IEEE are **encouraged to subscribe, at no cost, to this e-GRID Newsletter**, to find opportunities to "network" with the electrical engineering community and hear about Chapter events through our twice-monthly emails. This is a controlled list (ie, no spam) -- [get more information](#). You provide your own subscribe/unsubscribe services and can join and leave this IEEE DList when desired. To update the list, send an email message to:

listserv@listserv.ieee.org

...with the following choices in the BODY (not Subject) of the message:

to SUBSCRIBE:

subscribe e-GRID FirstName LastName

to UNSUBSCRIBE:

unsubscribe e-GRID

Or, to receive a text-only notification email, use the following in the BODY (not Subject) of the message:

to SUBSCRIBE:

subscribe e-GRID-text FirstName LastName

to UNSUBSCRIBE:

unsubscribe e-GRID-text

Maintain your current DList records at our IEEE LISTSERV website: <http://listserv.ieee.org/>

You may need to "whitelist" our email addresses in your spam filter to allow our Council news to reach you; I suggest whitelisting my email address, plus that of the DLIST: e-GRID@listserv.ieee.org.

Please invite other non-Member technologists in the Bay Area to join this list, to receive notification of Chapter meetings, tutorials, workshops, conferences, and other news within the San Francisco Bay Area Council, IEEE. See <http://www.e-grid.net/>

Correspondence to [Paul Wesling](#), Council Communications Director