Chapter Meetings and Events

SCV-EMS - 3/30 | **Career Checkpoints** and **Introducing Technology to Make Everyday Devices See** - check pointing your career, followed by time-of-flight 3D sensor chips for computer imaging, vision, distance measurement ... [more]

SCV-LEOS – 4/5 | **Semiconductor Ultraviolet Optical Sources: Status, Challenges, and Applications** - operation of AlGaInN materials system down to 340 nm and LEDs operating below 280 nm ... [more]

SCV-ED - 4/12 | **VLSI Devices for Analog and Mixed-Signal App'ns** - carrier-tunneling studies in deep-submicron MOSFETs... [more]

SCV-EMC - 4/12 | **EMI Analysis of complex systems;** and **Electrostatic Discharge - It failed! How to find the root cause** - different data analysis techniques; and ESD failure diagnosis ... [more]

SCV-Comm - 4/13 | **Where is the RFID Puck Going Next?** - Wal-Mart, Target, Albertsons, , casinos, passports: where next? ... [more]

SCV-AP - 4/13 | **A Spatial Channel Model for Multiple-Antenna Systems** - assessing the optimal number of antennas for given transmit and receive areas ... [more]

SCV-EMB - 4/20 | **Tactile Pressure Imaging: A New Tool For In Vivo Physiological Assessment for Gastroenterology** - portable advanced pressure imaging system with high fidelity pressure maps of the gastrointestinal tract ... [more]

SCV-IM - 4/20 | **ISO13485: A PDL and QSR Not Just for Medical Devices** - a Product Development Lifecycle standard that can make the job of a product or program manager easier ... [more]

OEB-IAS - 4/21 | **Electrical Power Generation, Distribution, and Plant Automation on Marine Vessels** - systems have to be as specialized as the vessel to meet modern cargo demands ... [more]

OEB-Comm - 4/21 | **Evolution of Mobile Wireless Technologies to the Year 2008** - new products and services, and China'sinfluence... [more]

SCV-SSC - 4/21 | **Power-aware and Temperature-aware Circuit Design** - max performance under power consumption constraints... [more]

SCV-PACE - 4/26 | **Resume-writing Clinic** - review the structure of a good resume, and bring your own for critique ... [more]

SCV-CNSV - 4/26 | **Who Owns Your Brain? A Consultant's Guide to Patents** - patents and intellectual property ... [more]

SCV-Rel - 4/27 | **When to use HALT and when to use ALT** - predicting a wearout mechanism, with case studies ... [more]

SCV-CPMT - 5/4 | **US Electronics Industry Competitiveness in View of Globalization and Changing Technologies** - IC and systems packaging: competitiveness of US industry ... [more]

SCV-CS - 5/7 | **Sensor Networks – The New Environment** - Saturday seminar, at Stanford ... [more]

Upcoming Conferences in the Bay Area

April 12-14: **IEEE Wescon**, Santa Clara Conv'n Ctr
Exhibits, seminars, tutorials *free admission* **[more]**

May 7: **SENSOR NETWORKS – The New Environment**, held at Stanford Univ **[more]**

May 17-19: **The Vision Show & Conference West**, San Jose Convention Ctr – Exhibits, sessions **[more]**

May 23-25: **Aeroacoustics Conference**, Monterey
Exhibits, seminars, tutorials **[more]**

May 24-26: **Aircraft Noise and Emissions Reduction Symposium**, Monterey
plenary-track session, tutorial, mini-expo **[more]**

June 21-23: **POFWorld '05**, Santa Clara Conv'n Ctr
Plastic Optical Fiber for Home and Auto –
sessions, tutorials, exposition **[more]**

10/3-11/2: **9th Asilomar Conference on Signals, Systems, and Computers** **Call for Papers** **[more]**

Upcoming Courses:

April 12: **Motor Control ... Robot Manipulators ... Control System Design: A Review** **(three)** **[more]**

April 13: **Designs for the High-Speed, Broadband Information Age** **[more]**

April 13: **Packaging Technology for RF and RFID** **[more]**

April 12-13: **Electromagnetic Compatibility Tutorials (four)** **[more]**

April 25-29: **Technology Review and Update**
5-day class, Naval Postgraduate School, Monterey **[more]**

May 4: **SOP vs SiP vs SOC: Technology Directions for Systems Implementation**
Seminar featuring the technical staff at Georgia Tech **[more]**

May 5: **Influential Communication**
listening, filtering, speaking - at KLA-Tencor, San Jose **[more]**

May 21-22: **Computational Aeroacoustics: Methods and Application** **[more]**

IEEE GRID

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April 2005 • *Volume 52 • Number 4*

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IEEE **GRID** is the monthly newsmagazine of the San Francisco Bay Area Council of the Institute of Electrical and Electronics Engineers, Inc. As a medium for both news and opinion, the editorial objectives of IEEE **GRID** are to inform readers in a timely and objective manner of newsworthy IEEE activities taking place in and around the Bay Area; to publish the official calendar of events; to report on IEEE activities of a national and international scope; and to serve as a forum for comment on areas of concern to the engineering community by publishing contributed articles, invited editorials and letters to the editor.

IEEE GRID is published as the **GRID** Online Edition residing at www.e-GRID.net, and in a handly printable **GRID.pdf** edition, and also as the **e-GRID** sent by email twice each month to more than 24,000 Bay Area members.

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From the editor . . .

You're certainly aware by now that Wescon is at the Santa Clara Convention Center in April. We have a one-sheet "guide" to most of the free seminars, panels, and other events – see **page 13** in this issue. You'll want to reserve your seat in one or more of the events during the 3-day run. And I'll plan to see you on the floor at Wescon!

I've found that a good way to find out what the new "hot buttons" are in our technologies is to scan the programs of upcoming conferences to see who is speaking and what the session and paper topics are. If it's an IEEE conference, and you're not able to attend, then the papers should soon be available in the IEEE **XPLORE**™ system. Why is this useful? Most of us work for a company, institution, or university that has "free" access to the full IEEE collection (over 1 million papers – actually, there are over 1,137,000 now). For those without corporate or institutional access, there is the Member Digital Library subscription, which gives you 25 papers each month – about as many as you'd want to read in a month!

You can get to IEEE's on-line database at **ieeexplore.ieee.org**; access to the index and to all abstracts is free to all. Select "Browse Conference Proceedings" and enter the keywords or acronym from the event's title. Did you know that you can also find most of these papers by doing a search in Google?

While you're at the **XPLORE** website, sign up to receive an automatic email alert whenever one or more new issues of specific journals are posted. It's a free service.

Paul Wesling **editor@e-grid.net**

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IEEE Professional Skills Courses

new! Influential Communication

Date/Time: Tuesday, May 17, 8:30AM-4:30PM
Instructor: Barry Flicker
Location: at KLA-Tencor, San Jose –

Without a context of mutual value, trust and respect, techniques alone prove useless. This one-day course asks participants to evaluate their current communication environment according to these standards. We then begin to examine the three primary communication skills - clear goal setting, making our message audience-appropriate, and active/empathic listening - so that participants understand how to improve their working relationships in any situation. This is a highly experiential workshop applicable for people at every level of the organization.

Session Objectives

- Identify things that we may be doing or failing to do that contribute to difficult communication.
- Apply S.M.A.R.T. Criteria to set clear, mutually agreed upon objectives.
- Resolve questions of competence through effective application of the situational speaking model.
- Listen through difference to manage conflict and build influence.

Engineering Management & Components, Packaging and Manufacturing Technology Societies, SCV Chapters

Key Topics

- The Three Levels of Listening
- 8 Blocks to Effective Listening
- Clearing Listening Blocks
- How to Stop Defending
- Value Clarification: Out to Lunch Game
- Listening Through Differences
- How Values Filter What We Hear
- The Communication Triangle
- SMART criteria for Clear Communication
- Situational Speaking

Improve your skills – register for a skills class. Bring a team!

For complete information and registration form, see our Chapter website, right-hand column:

www.cpmt.org/scv/

11th AIAA/CEAS Aeroacoustics Conference

23-25 May **(Course: 21-22 May)**

Co-located with the

AIAA/AAAF Aircraft Noise and Emissions Reduction Symposium

24-26 May **(Tutorial: 23 May)**

Hyatt Regency Monterey

Held on the magnificent Monterey Peninsula

The 11th **AIAA/CEAS Aeroacoustics Conference** provides an international forum for scientists and engineers from industry, government, and universities to exchange knowledge and results of current studies and to discuss directions for future research. Papers that cover all aspects of the generation, propagation, measurement, modeling, and control of vehicle noise, as well as the effect of noise on structures and individuals, will be presented at the conference.

KEYNOTE TALKS

"Prospects for a Quiet Future in Aeronautics"
Dr. Richard W. Wlezien, NASA

"Finding Hope Amidst the Challenges – Views of Aircraft Noise and Emissions Reduction"
John-Paul Clarke, MIT

PROGRAM

Over 30 sessions in 7 tracks, including:

- Acoustic/Fluid Dynamic Phenomena
- Airframe/High-Lift Noise
- Computational Aeroacoustics Methods
- General Acoustics
- Jet Noise Diagnostics
- Fan Noise Measurement and Modeling
- Jet Aeroacoustics Simulation
- Advanced Testing Techniques: Phased Arrays, Sensors and Methods, Facilities
- Community Noise and Metrics

TWO-DAY COURSE (Saturday, Sunday)

Computational Aeroacoustics: Methods and Application
(fee includes full admission to Aeroacoustics Conference)

Computational issues unique to aeroacoustics - CAA time marching algorithms - Radiation, inflow and outflow boundary conditions - numerical solutions - nonlinear wave propagation - multi-scales acoustics - applications to aeroacoustics problems

The **AIAA/AAAF Aircraft Noise and Emissions Reduction Symposium** is a high-level, multidisciplinary technical symposium bringing together leading engineers, scientists, researchers, government and civil aviation officials, industry, and policy makers to discuss the topics and issues of aircraft noise and emissions reduction. The objective is to review challenges and opportunities faced by manufacturers, local communities, air carriers, air navigation service providers, airports, governmental institutions, and non-governmental organizations to address noise and emission abatement and to develop holistic solutions that will ameliorate the pressures associated with air traffic growth.

PRE-SYMPOSIUM TUTORIAL

On Monday afternoon, Barry Scott, Director of the FAA Liaison Office, NASA Ames Research Center, will teach a course providing an overview of air traffic topics in preparation for discussions during the Symposium.

PROGRAM

The format of ANERS is a series of invited talks in a single-session, panel format and includes leading experts in the field. The program features balanced representation from Europe, the United States, and other regions of the world.

MINI-EXPO

There will be a Mini-Expo where organizations and manufacturers display information about their programs and products.

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Special low student, retired rates!

For full information on both events:

www.e-grid.net/conf/aero-aners.html

CALL FOR PAPERS

Thirty-Ninth Annual Asilomar Conference on Signals, Systems, and Computers

Asilomar Hotel and Conference Grounds, Pacific Grove, California
October 30 - November 2, 2005

URL: www.asilomarssc.org

Authors are invited to submit papers before June 1, 2005 in the following areas:

A. Communications Systems and Networking: 1. Error Detection and Correction, 2. Signal Representation and Spectral analysis, 3. CDMA, 4. Modulation and Detection, 5. Performance Bounds, 6. Synchronization, 7. Ultra Wideband, 8. OFDM / Multicarrier, 9. Networks, 10. Wireless Communications, 11. Optical Communications

B. Adaptive Systems and Processing: 1. Adaptive Filtering, 2. Adaptive Signal Processing, 3. Adaptive Beamforming, Adaptive Technologies for Communication, 4. Intelligent Hearing Aids

C. Array Processing and MIMO: 1. Array Processing, 2. Array Processing for Wireless Communications, 3. Sonar and Acoustical Array Processing, 4. Radar Array Processing, 5. MIMO / Space-time Coding

D. Biomedical Signal and Image Processing: 1. Medical Image Analysis, 2. Imaging Modalities, 3. Advances in Medical Imaging, 4. Biomedical Signal Processing, 5. Biomedical Applications, 6. Bioinformatics, 7. Image Registration and Multi-modal Imaging, 8. Image Reconstruction, 9. Computer Aided Diagnosis, 10. Functional Imaging, 11. Visualization

E. Signal Processing Algorithms and Applications: 1. DSP in Wireless Communications, 2. Radar and Sonar Signal Processing, 3. Energy Efficient DSP, 4. Low Rank Signal Processing, 5. Cooperative Analog / Digital Signal Processing, 6. Multimedia Signal Processing, 7. Multisensor / Multirate Signal Processing

F. Architecture and Implementation: 1. FPGA Implementation, 2. ASIC Implementation, 3. VLSI Implementation, 4. Computer Arithmetic, 5. Numerical Processing, 6. Architectures for Multimedia, 7. Security

G. Speech, Image and Video Processing: 1. Speech Processing, 2. Speech Coding, 3. Speech Recognition, 4. Narrowband / Wideband Speech and Audio Coding, 5. Document Processing, 6. Mathematical Models for Signal and Image Processing, 7. Image and Video Coding, 8. Image and Video Segmentation, 9. Image and Video Analysis, 10. Image / Video Security, Retrieval and Watermarking, 11. Image and Video Enhancement / Filtering, 12. Biometrics and Security

H. Tools and Strategies for Education

Prospective authors are invited to submit a 50 to 100 word abstract and an extended summary (500 to 1000 words, plus figures). Submissions must include the title of the paper, each author's name and affiliation, and the technical area(s) in which the paper falls with number(s) from the above list. Please visit the conference website (**www.asilomarssc.org**) for specific information on the electronic submission process. **No more than FOUR submissions are allowed** per contributor, as author or co-author. **All submissions must be received by June 1, 2005**. Notifications of acceptance will be mailed by late August 2005, and author information will be available on the conference website by mid September 2005. Full papers will be due at the conference and published in the spring of 2006. All technical questions should be directed to the Technical Program Chair, **Dr. Behnaam Aazhang**, e-mail: aaz@rice.edu, or the General Chair: **Dr. Hui Liu**, e-mail: hliu@ee.washington.edu .

CONFERENCE COMMITTEE

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The site for the 2005 Conference is at the Asilomar Conference Grounds, in Pacific Grove, CA. The grounds border the Pacific Ocean and are close to Monterey, Carmel, and the scenic Seventeen Mile Drive in Pebble Beach.

The Conference is organized in cooperation with the Naval Postgraduate School, Monterey, CA, Mission Research Corporation, Monterey, CA, and the IEEE Signal Processing Society.

The Vision Show and Conference – *West*

May 17-19, 2005

San Jose Convention Center

Tutorials Sessions Exhibits

Machine vision solutions for many industries, including:

- Electronics
- Medical Devices
- Security
- Aerospace
- Automotive
- Lab Automation
- Semiconductors
- Pharmaceuticals
- Biometrics
- Food & Beverage
- Defense/Military
- Consumer Products

The Vision Show West is North America's leading showcase of machine vision components, systems and solutions. Held every other year in the heart of Silicon Valley, the Show is the perfect venue for suppliers and system integrators to meet with system designers and users to share information on new products and real-world solutions.

Morning and afternoon technical sessions include talks by Industry experts giving presentations designed specifically to provide practical, real-world solutions to attendees. Topics cover all key issues that current and potential users need to know in order to successfully apply machine vision.

Half-day Tutorials (Monday, May 16)

- How to Select Machine Vision Components
- Lighting & Optics: The Basics
- Integrating Machine Vision Systems: From Basic Concepts to Systems Integration
- Advanced Lighting & Optics

Sessions (Tues-Wed AM/PM, Thurs AM)

- Machine Vision Software for Part Identification/Classification
- Non-Visible Imaging
- Advances in Camera Technology
- Integrating a Machine Vision Solution into Capital Equipment
- Advances in Vision Guidance
- Advances in Smart Cameras and Sensors
- Successful and Emerging Machine Vision Applications
- Selecting the Right Camera Interface for Your Needs
- Latest Developments in Gigabit Ethernet for Machine Vision
- Advances in 3-D Machine Vision Technology

(For details on session papers, see the website)

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Exhibits

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- Lighting Equipment
- Peripherals
- Vision Processors
- Cameras
- Frame Grabbers
- Lenses & Optics
- Smart Sensors
- Vision Software

New Product Showcase

Visit the **New Product Showcase** on our website to preview the newly introduced products that you can see at Vision West.

Straight Talk on New Products

In this special area right on the show floor, you'll hear presentations from technical experts at companies with new products on display, and get updates on important industry issues such as the Camera Link ® and GigE Vision™ standards. These talks will run continually throughout the show — they're free to all show and conference attendees!

Register Today

Free admission to the three days of exhibits – register on the website!

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For information, and to register on-line:

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To display at **Vision West**, contact Carol Calini at (203) 483-5774 or carol@reuterexpo.com

Technology Review and Update

A Short Course for Technical Personnel and Decision Makers

Five Days – April 25 through April 29, 2005
Held at the Naval Postgraduate School, Monterey

This annual 5-day short course is designed for civilian, military, and government technical personnel and decision makers interested in refreshing and updating their knowledge in important technical areas. The success and popularity of this short course is ensured through recruiting of outstanding experts from industry, academia and the government and by constantly fine tuning the contents. It provides an excellent overview and stresses the more practical aspects of the topics discussed.

TOPICAL AREAS:

- Internet Security – Opportunity or Oxymoron
- Integrated Circuits
- Information Systems, Operations and Strategies
- Microelectromechanical Systems (MEMS) - An Introduction and 5-Year Vision
- Electro-Optical and Infrared Systems
- Bioengineering and Biotechnology
- Military Satellite Communications Technology
- Commercial Satellite Communication Technologies and Trends
- Tour of Selected NPS Laboratories
  - Space Systems Laboratories
  - Fiber-optics Laboratory
  - Radar and EW Laboratory
  - Virtual Reality Laboratory

Hosted by: The Naval Postgraduate School, Monterey

Cost: $800 (checks only, no credit cards) Includes all sessions, tours, and Wednesday dinner

Registration: Trinh Hoang, 831-656-2958
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Register on-line through April 20!

For full schedule, module outlines, and instructors, download the Course Flyer at:

www.e-grid.net/docs/trau.pdf (PDF, 50 kB)

Further information and on-line registration:

CLICK!

www.sp.nps.navy.mil/trau/

IEEE Computer Society, SCV Chapter, and the North America Taiwanese Engineers' Association

SENSOR NETWORKS – The New Environment

7th IEEE/NATEA Annual Conference

Place: Braun Auditorium, Stanford University
Date: Saturday, May 7th, 2005

This one-day conference focuses on emerging Sensor Networks technologies. Sensor Networks move computing from being a distinct entity within an environment to becoming a seamless part of the environment. This profound change touches both computing and the way we operate in daily life. Sensor Networks and the technologies they represent are fast becoming a new reality. In order to better understand this emerging technology and its complex interactions, we present this one-day conference on Sensor Networks. Starting with the hardware, this conference will cover such vital issues as wireless networking, distributed algorithms and applications at the engineering level. The aim of this conference offering is to provide members of the engineering communities with enough basic information to be able to make decisions regarding sensor networks and their applicability in new and emerging technical environments.

Program:

- **Keynote: Sensor Network Overview**
- **Hardware Design in Integration of Sensor Networks**
- **Wireless Networking**
- **Distributed Algorithms**
- **System Design including Transceivers, Transmitters and Receivers**
- **Applications of Sensor Networks**

REGISTER TODAY!

Rregister early to ensure a seat for this technical program.

REGISTRATION	By April 30	After April 30
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NON-MEMBER	$60.00	$70.00
STUDENT (fulltime)	$25.00	$30.00
UNEMPLOYED*	$25.00	$30.00

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www.natea.org/NFIC/

APRIL 12-14
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D2M: Design to Manufacture Solutions

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Wescon is the re-engineered industry event for the total design-to-manufacture process. The Wescon/2005 Exhibit and Conference Program broadens its focus to the needs of the design, systems, production, and support engineer to bring new visions of where technology is taking us, today and tomorrow.

Wescon brings engineers and scientists together in an environment that advances their education and careers by opening doors to a wealth of intellectual property, a wide range of technology tools and components, and access to immediate solutions for commercial applications.

Keynote:

Is the Wireless Industry Disconnected?
Martin Cooper,
Array Communications

Special Sessions (free):

Spintronics: A New Spin on Electronics
Kevin Roche, Staff Engineer/Scientist, IBM Almaden

Advances in Wireless Communications
Dr. Arthur W. Astrin, Senior VP, STEP Communications

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Test & Measurement Track

Free Tutorials and Panels:

Advances in Signal Integrity Testing
Rick Nelson, Editor in Chief,
Test & Measurement World

Testing and Troubleshooting Serial Data Signals and **Getting More Out of Your Digital Oscilloscope**
Dr. Michael Lauterbach,
LeCroy Corporation

Productivity Features in Mid-range, Windows Oscilloscopes Bill Leineweber, Tektronix

Debugging Elusive Digital System Problems Using Sophisticated Logic Analyzer Triggering and **Faster Ways to Characterize Transients RF Signals**
David Hayworth, Tektronix

Test Data Management System Optimizes Product Development Process Don Holley, VI Technology

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Roland Crop, Tektronix

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Innovative Approaches to Tackling the Challenges of D2M Steve Schulz, President and CEO, Si2
Morning session topics: – DFM: The Physics – Yield: The Basics – Lithography Challenge – Design Optimization Yield – Test to Yield Prediction – Design for Yield: Mixed Signal Analog – Library Challenge

Meeting the Challenges of Complex Systems Design
Henry Potts, Vice President and GM, Mentor Graphics

Advanced Interconnect David Wiens, Mentor Graphics

Also:

Cost Trade-offs and Design Techniques for Embedded Passives and HDI Technologies

Integrated Systems Design -- Trends, Challenges and Solutions

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Continued, next page ➔

Tutorials and Seminars co-located at WESCON in Santa Clara – April 12-14

SCV Microwave Theory & Techniques Chapter

Designs for the High-Speed, Broadband Information Age

- **Wednesday, April 13, 2005**
- **Seminar: 8:30 AM – Noon**
- **Registration/Breakfast: 8 AM – 8:30 AM**
- **Santa Clara Convention Center**
- **In conjunction with IEEE WESCON'05**
- **Includes free admission to WESCON exhibits**

More information on **Page 10**

SCV Control Systems Chapter

Three Seminars
(choose one, or all three)

General Concepts of Motor Control
8:30 AM – 11:00 AM

Understanding Robot Manipulators
11:30 AM – 2:00 PM (includes lunch)

Control System Design: A Review
2:30 PM – 5 PM

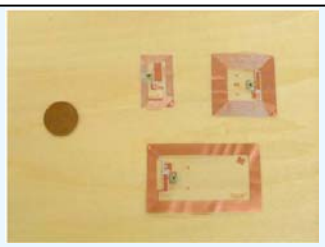
- **Wednesday, April 13, 2005**
- **Santa Clara Convention Center**
- **In conjunction with IEEE WESCON'05**

More information at

www.ewh.ieee.org/r6/scv/css/

SCV Components, Packaging & Mfg Technology Chapter

Packaging Technology for RF & RFID



- **Wednesday, April 13, 2005**
- **Seminar: 1:00 – 5:30 PM**
- **Registration: begins at Noon**
- **Santa Clara Convention Center**
- **In conjunction with IEEE WESCON'05**
- **Includes free admission to WESCON exhibits**
- **Plenty of free parking**

With the advent of RFID chips in the commercial sphere, many companies and individuals are taking an interest in this emerging market. Major retail outlets as well as government uses of the devices are spurring a great deal of speculation about the future of the technology and creating demands for lower cost. Because of the small size and extreme cost constraints, packaging and test of these unique devices presents a challenge in terms of handling, yield and cost. This seminar will bring together leading experts in the field to discuss manufacturing, infrastructure, packaging and cost reduction efforts in the industry. The seminar also addresses packaging trends for RF subsystems and systems, with a focus on the latest in System-in-Package technology. (see also the **"SoP/SiP/SOC" Seminar** on May 4.)

The topics include:

- RFID technology and deployment
- Packaging technology and standards
- Manufacturing and cost considerations
- Training opportunities and sources of more information

PROGRAM

Introduction and Overview – Seminar Chairman

- Al Scott - Besser Associates "**Overview of RFID Technology and Deployment**"
- Raj Bridgelall - Alien Technology – "**Packaging Technology for UHF RFID Tags**"
- Prof. Vivek Subramanian, UC-Berkeley – "**Prospects for all-printed RFID: Technology, Opportunities, and Challenges"**
- Telesphor Kamgaing, Intel Corporation – **"Design of Small-Form-Factor RF packaging for Wireless Communication Systems "**
- Norm Owens, Freescale Semiconductor – "**RF/Microwave Packaging Technology at Freescale Semiconductor**"

REGISTER TODAY!

The seminar is filling up fast, so register early to ensure a seat for this interesting technical program.

REGISTRATION	By April 1	After April 1
IEEE MEMBER	$75.00	$95.00
NON-MEMBER	$110.00	$125.00
STUDENT (fulltime)	$30.00	$35.00
UNEMPLOYED*	$30.00	$35.00

*With proof of unemployment

Regiser through PayPal or use **registration form**:

www.cpmt.org/scv/courses/rfid.html

Tutorials and Seminars co-located at WESCON in Santa Clara – April 12-14

Explore Wescon at

www.wescon.com

SCV Electromagnetic Compatibility Chapter

Four Half-Day Tutorials *(choose one, or all four)*

Fundamentals of Electromagnetic Compatibility
April 12 – 8:00am – noon

Fundamental Concepts of Signal Integrity & EMC Related to Printed Circuit Boards
April 12 – 1:00pm – 5:00pm

Testing for EMC Compliance – Approaches and Techniques
April 13 – 8:00am – noon

Fundamentals of Grounding and Shielding for System Level Noise Reduction
April 13 – 1:00pm-5:00pm

Instructor: Mark Montrose
Montrose Compliance Services, Inc.

Other Tutorials:

Key Issues of EMI/EMC
April 14 – 9:00am – Noon

High-Frequency Digital Design and PCB Layout
April 14 – 1:00pm – 4:00pm

Get full information and **register** at

www.wescon.com

Exhibits

Discover innovative design tools, test equipment, services and component-level products for the next generation of electronic systems. Products that include:

- Design and Analysis
- Test and Measurement
- Prototype Production
- Power Components
- Active, Passive & Electro-mechanical Components
- Interconnects

Two-one-day seminars (no cost)

Designing low cost systems using Xilinx Spartan-3 Generation FPGAs

XILINX®
The Programmable Logic Company℠

April 12 - **Low Cost DSP Systems**
April 13 - **Low Cost Embedded Processing Systems**

Register though the Wescon website

Industry Leaders

Respected leadership from across industry sectors join together to determine IEEE Wescon's content and direction. The Advisory Committee for this spring's event includes:

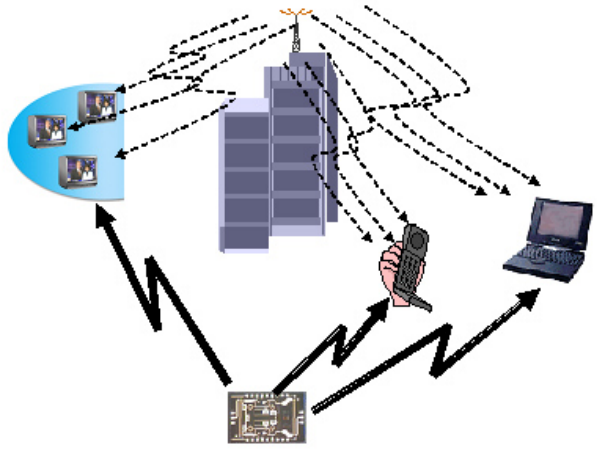
Dr. Meyya Meyyappan, Director, Center for Nanotechology, NASA Ames Research Center
Larry Tracewell, President and CEO, Tracewell Systems
Dr. Jack Pearson, Former Vice President and General Manager, Air Combat and Strike Systems, Raytheon
Masami Yamamoto, Co-founder and Chairman, Beganto, Inc.
Mark Strauch, Deputy Program Director, Engineering, Lawrence Livermore National Laboratory
Dr. Anthony F. Laviano, Council on Nanotechology, National Academy of Science
Bernie Siegal, IEEE Fellow & Director, Thermal Engineering Associates, Inc.

Annual Half-day Workshop:

Designs for the High-Speed, Broadband Information Age

- **Wednesday, April 13, 2005**
- **Seminar: 8:30 AM – Noon**
- **Registration/Breakfast: 8 AM – 8:30 AM**
- **Santa Clara Convention Center**
- **In conjunction with IEEE WESCON'05**
- **Includes free admission to WESCON exhibits**
- **Plenty of free parking**

Microwave Theory & Techniques Society
Santa Clara Valley Chapter



As the need for higher data rates and faster user interfaces increases, demands are placed on both the technology used to transmit and receive this information and on its designs. Previously, the realm of high speed, high frequency, high bandwidth circuits was relegated to III-IV materials like GaAs or InP. Recently, advances in materials like Si and SiGe have forced designers to look at these technologies to keep the cost low and to be competitive. Additionally, innovations like those in newer materials like GaN have been sought to provide advantages for these types of circuits.

Therefore, the ability to understand how the requirement for higher speed and faster data rates drives microwave circuit designs and the ability to design circuits in these various technology choices is an important part of the contemporary engineer's job as well as his/her value to an organization. The main challenges for today's microwave circuit designer are to understand which technology to use for a given application and know the tradeoffs and limits when designing in these technologies.

This seminar will explore the advances that have been made in these various material technologies and their affect on IC designs. Speakers will cover:

- The applications and requirements for higher speed and faster data rates
- The advantages and disadvantages of these technologies for handling higher speed/data rate applications
- How the need for faster and increased quantity of information affects circuit designs
- Current examples of designs and the tradeoffs addressed

To register, send your contact information and the fee to: Benson Chan (MTT Treasurer)
M/A-Com 5300 Hellyer Ave
San Jose, CA 95138
Phone# 408-624-3359

PROGRAM

100GHz CMOS Circuits and the High Speed Broadband Information Age
Dr. Luiz Franca-Neto, Technical Leader and Manager, Broadband Wireless Division (BWD) Intel Communications Group (ICG), Intel Corporation

SiGe and RFCMOS Technology for the High Speed Information Age
Dr. Xiaojuen (Ben) Yuan, Ph.D, IEEE Senior Member, Vice Chair, SSC/AP/MTT IEEE San Diego Chapter, IBM West Coast Foundry Applications

InP HBT Design for 100 to 200GHz IC's
Dr. Zachary Griffiths, Post Doc Researcher, UC Santa Barbara

SiC and GaN Based Transistor and Circuit Advances
Mr Simon Wood Principal RF Design Engineer, Cree Microwave

REGISTER TODAY!

Space is limited, so please mail in your registration before **April 9**. Registration fee includes breakfast and the course CD (proceedings).

Registration Fee:	Pre-Reg'n by **Apr 9**	After **Apr 9**
IEEE Members	$50	$65
Nonmembers	$75	$90
Students	$30	$30
Unemployed *	$30	$30

* Bring or send a photocopy of unemployment check receipt dated within 2 weeks of registration to qualify

For Workshop registration information, please visit the MTT Chapter website:

www.mtt-scv.org

IEEE

Wescon

Connecting Engineers, Business and Technology

April 12-14, 2005
Santa Clara Convention Center

NO CHARGE For All Events Listed Below. *(Please circulate)*
Complete conference information
available at www.wescon.com
Seminar/Course Info: www.e-grid.net/docs/wescon05.pdf
Priority Code: GRID

Express Registration — for Exhibit Floor and Complimentary Conference Events

Name _____ Title _____

Company _____ Address _____

City, State, Zip _____ Email: _____

Please check each event you plan on attending (all at No Charge)

IEEE Wescon Exhibit Hours		10-5 Tue 4/12	10-5 Wed 4/13	10-4 Thu 4/14
IEEE Wescon Conference Hours		8:00-5:30	8:00-5:30	9:00-4:00
Tuesday, April 12				✓
P1	Panel - Advances in Signal Integrity Testing		10:00am-11:30am	
SS1	Spintronics: A New Spin on Electronics		1:00pm-2:30pm	
T1	Testing and Troubleshooting Serial Data Signals		1:30pm-3:00pm	
T2	Productivity Features in Mid-Range, Windows Oscilloscopes		3:30pm-5:30pm	
Wednesday, April 13				
K3	Keynote - Nanometer Era Design for Manufacturability		8:00am-8:45am	
SD4	Design for Manufacturing Fundamentals		8:45am-9:15am	
SD5	Design for Yield Fundamentals		9:15am-9:45am	
SD6	Optical Lithography Forever…and DFM, The Good, The Bad and The Ugly		9:45am-10:15am	
T3	Getting More Out of Your Digital Oscilloscope		10:00am-11:30am	
SD7	Design for Manufacturability in an Analog World		10:15am-10:45am	
SD8	Design Optimization for Yield		10:45am-11:15am	
SD9	Redefining Test for the DFM Era		11:15am-11:45am	
SD10	Library Challenges		11:45am-12:15pm	
K1	Keynote - Meeting the Challenges of Complex Systems Design		1:00pm-1:50pm	
T4	Debugging Elusive Digital System Problems Using Sophisticated Logic Analyzer		1:00pm-2:30pm	
P2	Panel - Coming Issues and Innovation		2:00pm-3:30pm	
SD1	High Speed Design – Not Just Simulation; a Process		2:00pm-2:45pm	
SD2	Cost Trade-Offs and Design Techniques for Embedded Passives and HDI…		2:45pm-3:30pm	
T5	Faster Ways to Characterize Transient RF Signals		3:00pm-4:30pm	
T5	Faster Ways to Characterize Transient RF Signals		3:00pm-4:30pm	
SD3	Integrated Systems Design – Trends, Challenges and Solutions		3:45pm-4:30pm	
P3	Panel - Integrated Systems Design Panel Discussion		4:30pm-5:30pm	
Thursday, April 14				
S1	Frequency Control Technical Seminar			9:00am-10:15am
K2	Keynote - Is the Wireless Industry Disconnected?			10:00am-11:30am
T6	Test Data Management System Optimizes Product Development Process			10:00am-11:30am
T7	High Speed Probing and Signal Fidelity			1:00pm-2:30pm
SS2	Advances in Wireless Communications			1:00pm-2:30pm

PRIOR TO FRIDAY, APRIL 8 – Fax to 310-410-0164. AFTER April 8, Bring form to IEEE Wescon

Santa Clara Convention Center Plenty of Free Parking

An IEEE Technical Seminar in the S. F. Bay Area

"SOP vs SiP vs SOC: Technology Directions for Systems Implementation"

Emerging and Disruptive Packaging Technologies for the Next Decade

Featuring the technical staff of the NSF-sponsored Georgia Tech Packaging Research Center

Held at the Ramada Inn, Sunnyvale
Wednesday, May 4, 2005, from 8:00 AM - 5:30 PM

System-on-Package (SOP) refers to ultra-miniaturization of systems using thin-film component integration, in contrast to transistor integration for ICs. This provides a "Moore's Law" for system integration, akin to Moore's Law for IC integration. The SOP paradigm changes the current chip-centric System-on-Chip (SOC) methodology to a cheaper, faster-to-market IC-package-system co-design flow. The advantages of the SOP paradigm over SOC appear overwhelming due to SOPs design simplicity, lower cost and higher system functional integration, improved electrical performance, and without the intellectual property issues that dominate SOC. SOP is also different from and offers advantages over 3D packaging and SIP. The 3D packaging is a general concept for stacking of similar or dissimilar chips (such as DRAMS or DRAMs) with processor and flash memory. The SIP can go beyond, to embed both active and passive devices. The SOP focuses on integrating heterogeneous system functions, optimizing the integration of digital, RF, optical, sensor and other technologies.

DATE & TIME:

- Wednesday, May 4, 2005, from 8:00 AM - 5:00 PM
- Registration: 7:30 AM
- Lunch: Noon - 1:15 PM
- Reception/dinner following: 5 - 8 PM (optional)

COST:

- IEEE Members: $95
- Non-Members: $150
- After April 25: Member $110, Non-Member $165
- Includes lunch, class booklet, refreshments, and admission to the optional evening reception

WHO SHOULD ATTEND:

Packaging engineers, photonics engineers, systems engineers, thermal and mechanical engineers, PCB layout engineers, design, process, failure analysis, and reliability engineers and managers.

PROGRAM:

Morning Session (8:00-11:45 AM)
"**SOP: The Second Moore's Law for Systems in Contrast to First Moore's Law for ICs**," Prof. Rao Tummala, Director, GaTech Packaging Research Center
"**Mixed Signal SOP Design**," Prof. Madhavan Swaminathan
High-Density/High-Throughput Chip-to-chip Optical Interconnect SOP for Next-Generation Computing and Communication Systems," Prof. Gee-Kung Chang
"**RF/Wireless 3D Packaging and Integration: Current Challenges and Solutions**," Prof. Manos Tentzeris

Lunch Session (12:00-1:15 PM – includes Buffet Lunch)
Keynote Presentation: "**US and Electronic Industry Competitiveness in view of Globalization and Changing Technologies**," Prof. Rao Tummala

Afternoon Session (1:30-5:00 PM)
"**High Performance Nano Materials for Electronic, Photonic and MEMS Packaging**," Prof. C.P. Wong
"**Multigigahertz Test Methods for SOPs and Wafer-level Packaged Devices**," Prof. David Keezer
"**Thermo-Mechanical Reliability and Design Challenges for Next-Generation Microsystems Packaging**," Prof. Suresh Sitaraman

Evening Session (5:00-8:00PM – optional)
Informal Reception and Social with Drinks and Light Dinner. Meet the Georgia Tech PRC faculty members for informal discussions

For Seminar registration information, please visit the Chapter website:

www.cpmt.org/scv

Use our PayPal registration and payment system online

SCV Magnetics

TUESDAY MARCH 29

Origin of Tunneling Spin Polarization

Speaker: Dr. Stuart Parkin, Director, IBM-Stanford Spintronic Science & Applications Center, IBM Almaden Research Center
Time: Coffee and conversation at 7:30 p.m.
Presentation at 8:00
Place: Komag, 1710 Automation Parkway, San Jose
RSVP: not required
Web: www.e-grid.net/docs/0503-scv-mag.pdf

Stuart Parkin joined IBM Research in San Jose in 1982 as a post-doctoral Fellow, becoming a permanent member of the staff the next year. Dr. Parkin's research interests have included organic superconductors, high-temperature superconductors and, most recently, magnetic thin-film structures and spintronic materials and devices for advanced sensor, memory and logic applications.

In 1991, Dr. Parkin discovered oscillations in the magnitude of the interlayer exchange coupling in transition-metal magnetic multilayered systems exhibiting giant magnetoresistance (GMR). This development led to the creation of GMR sensors that enabled huge increases in hard-disk drive data density. For this and related work, Dr. Parkin shared the American Physical Society's International New Materials Prize (1994) and the European Physical Society's Hewlett- Packard Europhysics Prize (1997). He is a Fellow of the Royal Society, the American Physical Society, the Institute of Physics (London), the Institute of Electrical and Electronics Engineers and the American Association for the Advancement of Science. In 1999 he became an IBM Fellow, IBM's highest technical honor. Dr. Parkin has authored more than 300 published papers and has 47 issued U.S. patents.

Dr. Parkin received his B.A. degree (1977) and was elected a Research Fellow (1979) at Trinity College in Cambridge, England, and earned his Ph.D degree (1980) at the Cavendish Laboratory, also in Cambridge. Since 1997 Dr. Parkin has been a Consulting Professor in the Department of Applied Physics at Stanford University. He is also Director of the IBM-Stanford Spintronic Science and Applications Center, which was formed in April 2004

The relationship of the spin polarization of current tunneling from a ferromagnetic material (through a tunnel barrier) to its magnetization is of considerable current interest, particularly with regard to the development of magnetic tunnel junctions with high tunneling magnetoresistance suitable for magnetic memory and sensor applications1. The tunneling spin polarization (TSP) can be directly measured using superconducting tunneling spectroscopy (STS) or inferred from measurements of tunneling magnetoresistance (TMR). The TSP depends not only on the ferromagnetic material but also on the tunneling barrier. Using crystalline (100) oriented MgO tunnel barriers and bcc CoFe electrodes, TSP values exceeding 85% are found from STS studies at 0.25 K with TMR values greater than 300% at 5K2. The same ferromagnetic electrodes using conventional amorphous alumina tunnel barriers exhibit TSP values of only ~50%. In these cases the sign of TSP is positive corresponding to the preferential tunneling of majority spin electrons. However, using magnetic electrodes formed from the ferrimagnetic rare-earth transition-metal alloys, such as Co-Gd, we show that the sign of the TSP and TMR can be either positive or negative depending on the composition of the alloy and temperature. For alloys of Co and Fe with Pt and Pd we show that the TSP is strongly influenced by bonding at the tunnel barrier/ ferromagnetic electrode interface. In particular, we compare results for CoPt alloys with AlN and Al2O3 tunnel barriers. For AlN barriers the TSP decreases linearly with increasing Pt content whereas for Al2O3 tunnel barriers the TSP has only a weak dependence on Pt content for up to ~50 atomic % Pt. These results can be understood as a consequence of stronger Co - oxygen bonds as compared to Pt – oxygen bonds.

SCV Engineering Management

WEDNESDAY MARCH 30

Forum: **Career Checkpoints**

Speaker: Robyn Chew-Gibbs, HR Training & Development Manager, Juniper Networks

and

Introducing Technology to Make Everyday Devices See

Speaker: Dr. Abbas Rafii, Executive VP, Canesta, Inc.
Time: Forum at 6:00 PM, Dinner at 7:00 PM, after-dinner presentation at 7:45 PM
Place: Prime Hotel, 1300 Chesapeake Terrace, Sunnyvale - off Lawrence Expy/Caribbean Dr at Hwy 237
RSVP: Please reserve in advance through website
Web: www.ieee-scv-ems.org

Robyn Chew-Gibbs, Human Resources Training & Development Manager at Juniper Networks, will lead the group through a working session designed to show how to productively analyze and plan your career direction.

In September of 2004, Robyn joined Juniper Networks as the first Human Resources Training Manager. Responsible for management development and "soft skills" training world wide, Robyn continues to be motivated by the excitement that employees exude when mastering a new skill that results in personal growth and positive business impacts!

Formerly, she was employed for 9 years at Levi Strauss & Co. She was part of the Corporate Training & Development department where she facilitated various training programs including Performance Management, Valuing Diversity and Leadership training. During her tenure at Levi's she was tapped by the CEO to direct the Corporate Work/Family Initiative. This initiative, one of the few of its kind at the time, earned Levi's recognition by Working Mother magazine as one of the "Top 100 Companies for Women."

After achieving her goals at Levi's, Robyn began her own consulting firm, specializing in management and employee development. During the 10 years as a consultant, she amassed a loyal clientele including Wells Fargo Bank, Advanced Fibre Communications, Blue Shield of California, Industrial Light + Magic,

(continued, next column)

Career Checkpoints (before-dinner Forum)

The speed of change causes many to ask: "Where will I be in x years"? The better question is: "Where will I be next year?" Taking it one step further, the ideal question is: "Where do I want to be next year?"

How often have you said, "I wish I could change jobs or change careers!" Chances are this question will remain rhetorical until you closely examine the reasons you state this wish and begin to uncover what is at the root of your desire for change. Once understood, creating an appropriate plan becomes an easier & more successful undertaking.

Introducing Technology to Make Everyday Devices See (After-Dinner presentation)

Despite impressive advances in imaging technology, computers remain essentially blind and unable to make sense of their environment. The advances in time-of-flight 3D sensor chips promise to bring this technology to large volume deployment, making ranging the next big development in computer imaging and vision markets. Canesta's work in this area enables everyday devices to recognize and intelligently interact with their environments. Bringing the technology to the market involved making many challenging technical and business decisions.

(continued)

Skywalker Sound, Intel and Oracle. Robyn holds certifications in Myers Briggs Type Indicator and Project Management.

Robyn is a native San Franciscan and 3rd generation Chinese-American. She earned Undergraduate and Graduate degrees from the University of California at Los Angeles.

Dr. Abbas Rafii is Executive Vice President and one of the founders of Canesta, Inc. He has extensive background in software engineering and business management. His current focus is directing the software development for the company's Electronic Perception Technology. Earlier, he directed the development of Projection Keyboard application. He received his MS and Ph.D. in EECS from Stanford University.

He was a founder and held the position of Vice President in Penware and atPos (now part of Symbol). He recruited the team and directed the design and

development of the company's PDA, Point of Sale, enterprise, and e-commerce applications. He provided technical support in closing large deals and started several technology and business development initiatives in the company.

Earlier, he was a software scientist and an architect of heterogeneous object databases at Hewlett-Packard Laboratories. Prior to that, he was a system performance specialist at Hewlett-Packard's commercial and UNIX operating systems labs. He has published papers on computer performance evaluation and heterogeneous object databases and has also taught Computer Science at University of Oklahoma, U.C. Davis and Santa Clara University. He has authored and been granted several patents

IEEE Professional Skills Courses

new! Influential Communication

Date/Time: Tuesday, May 17, 8:30AM-4:30PM
Instructor: Barry Flicker
Location: at KLA-Tencor, San Jose –

Without a context of mutual value, trust and respect, techniques alone prove useless. This one-day course asks participants to evaluate their current communication environment according to these standards. We then begin to examine the three primary communication skills - clear goal setting, making our message audience-appropriate, and active/empathic listening - so that participants understand how to improve their working relationships in any situation. This is a highly experiential workshop applicable for people at every level of the organization.

Session Objectives

- Identify things that we may be doing or failing to do that contribute to difficult communication.
- Apply S.M.A.R.T. Criteria to set clear, mutually agreed upon objectives.
- Resolve questions of competence through effective application of the situational speaking model.
- Listen through difference to manage conflict and build influence.

Engineering Management & Components, Packaging and Manufacturing Technology Societies, SCV Chapters

Key Topics

- The Three Levels of Listening
- 8 Blocks to Effective Listening
- Clearing Listening Blocks
- How to Stop Defending
- Value Clarification: Out to Lunch Game
- Listening Through Differences
- How Values Filter What We Hear
- The Communication Triangle
- SMART criteria for Clear Communication
- Situational Speaking

Improve your skills – register for a skills class. Bring a team!

For complete information and registration form, see our Chapter website, right-hand column:

www.cpmt.org/scv/

SCV Lasers and ElectroOptics

TUESDAY APRIL 5

Semiconductor Ultraviolet Optical Sources: Status, Challenges, and Applications

Speaker: Dr. Noble Johnson, Palo Alto Research Center
Time: Networking and Pizza Social at 7:00 PM; Presentation at 8:00
Place: National Semiconductor Credit Union Auditorium, 955 Kifer Road, Sunnyvale
RSVP: by email to rsvp-scv-leos@ieee.org
Web: ewh.ieee.org/r6/scv/leos/

Dr. Noble Johnson received his Ph.D. degree from Princeton University in 1974 under a National Defense Graduate Fellowship. From 1974 to 1976 he worked at SRI International (Menlo Park, CA) in the Radiation Physics Group of the Physical Sciences Division. In 1976 he joined the Xerox Palo Alto Research Center (now the Palo Alto Research Center) as a Member of the Research Staff in the Electronic Materials Laboratory. There he is a Principal Scientist and Manager of Optoelectronic Materials and Devices. He has conducted experimental research in the general areas of electronic materials and devices. Dr. Johnson has published over 330 research papers in technical journals and conference proceedings, has organized several topical and international conferences, has served as an editor of five books, and is an inventor on ten patents. In 1987 Dr. Johnson received a Distinguished Senior U.S. Scientist Award from the Alexander von Humboldt Foundation, Germany, and in 1988 he worked in residence at the Institute for Applied Physics, University of Erlangen-Nürnberg, Germany. He received awards for excellence in science and technology from Xerox PARC in 1987 and 1997 and from PARC in 2003. As Manager of the Optoelectronic Materials and Devices Program he has guided the activities of a world-class R&D team that has successfully developed violet and ultraviolet lasers and which has made major contributions to fundamental understanding of the material and devices. Dr. Johnson is a fellow of the American Physical Society and a fellow of the Institute of Electrical and Electronics Engineers.

Over the past 40 years semiconductor optical sources, light emitting diodes (LEDs) and laser diodes (LDs), have been displacing conventional light sources and gaseous lasers in commercial applications throughout the near infrared (IR) and visible regions of the spectrum. And in many cases, newer semiconductor sources with improved performance have displaced older semiconductor sources; an example currently in progress is the replacement of red LDs in DVDs by violet LDs for the next generation Blue-Ray or HD-DVD format.

The new frontier in the development of semiconductor sources is the ultraviolet (UV). This effort is well underway, with LDs already demonstrated in the AlGaInN materials system down to 340 nm and LEDs operating below 280 nm. Such UV sources will enable miniaturization and/or cost/performance improvements for existing UV-based systems, with proliferation of existing functionality and realization of new applications. In comparison with existing UV gas sources (lasers and lamps) and other more complex and costly solid-state lasers (e.g., photo-pumped lasers and frequency-tripled /quadrupled lasers), semiconductor UV sources offer several advantages including compactness, low power consumption, low cost, and long lifetimes. These features will drive a host of commercial applications in areas that include biotechnology, water purification, and UV curing. The first area of commercialization will likely be replacement of Hg lamps for germicidal and (low-power) UV curing applications. In addition, as with any truly destabilizing technology, there will likely be completely new applications that have yet to be conceived.

SCV Electromagnetic Compatibility

TUESDAY APRIL 12

EMI Analysis of Complex Systems; *and* Electrostatic Discharge - It Failed! How to Find the Root Cause!

Speaker: Dr. David Pommerenke, UMR
Time: Social 5:30 PM, Presentation 7:00 PM
Place: Applied Materials Bowers Cafeteria, 3090 Bowers Ave., Santa Clara
RSVP: not required
Info: www.scvemc.org/

David Pommerenke is associated professor at the EMC laboratory at UMR. Dr. Pommerenke's speciality is the combination of electronics and electromagnetics. Such problems can be found in intentional or unintentional disturbances of circuits, Signal Integrity of fast networks and other situations in which the circuit behavior is dominated by "everything that is not on the circuit diagram". His interests are: EMC, ESD, Electronics, Signal Integrity, measurement instrumentations and testing. Before joining UMR he worked as an EMC Engineer at HP for five years. He is member of the ESD standard setting group within IEC TC77b.

Part I: EMI Analysis of complex systems

Many methods and tools exist for the analysis of EMI of complex systems. Examples are different probing methods, time domain data analysis, frequency domain data analysis at different bandwidths and the methods that fall between time and frequency domain, such as zero span spectrum analysis and Joint-Time-Frequency Analysis techniques such as Short Term FFT and wavelet analysis.

This talk will show the application of different data analysis techniques for complex systems. Special emphasis is given on explaining the methods and on showing when which method provides the better insight, not on promoting one or the other method.

Part II: Electrostatic Discharge - It failed! How to find the root cause!

Assume a system has failed an ESD test. Of course, one could improve shielding, but isn't it better to exactly understand which electrical net or IC had been affected and, consequently, just apply a small change to the board or software?

The talk explains methods on how to find the root cause of ESD failures by systematic local injection and how to probe signals with GHz bandwidth, while applying ESD to the system. It will show examples of systems that experienced ESD failures that have been located using this technique. Further, it will discuss how IC-level EMC will influence ESD design.

SCV Electron Devices

TUESDAY APRIL 12

VLSI Devices for Analog and Mixed-Signal Applications

Speaker: Dr. Jason Woo, UCLA
Time: Pizza social (free) at 6:00pm; Presentation at 6:15pm
Place: National Semiconductor Corp. Building 31 Large Auditorium, 955 Kifer Road, Sunnyvale
RSVP: not required
Info: Philippe Jansen, philippe.jansen@nsc.com

As scaling of CMOS approaches sub-100nm, many difficulties are encountered such as short-channel effects, device performance improvement limits, severe reliability issues and gate leakage issues. In terms of analog behavior, these problems translate into lower intrinsic gain and higher non-linearity. This talk will discuss the scaling behavior of scaled CMOS for analog/RF applications. A novel device architecture which has superior analog behavior will also be discussed.

Dr. Jason C.S. Woo received the B. A. Sc. (Hons) degree in engineering science from the University of Toronto, Canada, in 1981, and the M. S. and Ph. D. degrees in electrical engineering from Stanford University in 1982 and 1987, respectively. He joined the department of electrical engineering of UCLA in 1987, where he is currently a professor. He has done work on low-temperature devices for VLSI applications, SOI BiCMOS, SiGe BiCMOS and other novel devices. He has authored and co-authored over 160 papers in technical journals and refereed conference proceedings in these areas.

SCV Microwave Theory & Techniques Chapter

Designs for the High-Speed, Broadband Information Age

SiGe, RF-CMOS, SiC, GaN technologies

- **Wednesday, April 13, 2005**
- **Seminar: 8:30 AM – Noon**
- **Registration/Breakfast: 8 AM – 8:30 AM**
- **Santa Clara Convention Center**
- **In conjunction with IEEE WESCON'05**
- **Includes free admission to WESCON exhibits**

More information on **Page 12**

SCV Antennas and Propagation

WEDNESDAY APRIL 13

A Spatial Channel Model for Multiple-Antenna Systems

Speaker: Dr. Ada Poon, SiBeam Inc.
Time: 6:00 p.m. (pizza & soda), 6:30 p.m. presentation
Cost: none
Place: Cogswell College (Boardroom), 1175 Bordeaux Dr, Sunnyvale
RSVP: d by email to Greg Manassero at greg.manassero@ieee.org
Web: www.ewh.ieee.org/r6/scv/scv_aps.html

Dr. Ada S. Y. Poon received the B.Eng and M.Phil. degrees in Electrical and Electronic Engineering from the University of Hong Kong in 1996 and 1997 respectively, and received the M.S. and Ph.D. degrees in Electrical Engineering and Computer Sciences from the University of California at Berkeley in 1999 and 2004 respectively. From Oct. 2003 to Jan. 2005, she was a senior researcher at Intel Corporation, Santa Clara, where she researched feedback schemes for multiple-antenna systems and implementation of baseband processors for future flexible radios. Currently, she is with SiBeam, Inc., Fremont, a startup company designing Gigabit wireless transceivers leveraging 60 GHz CMOS technology and multiple-antenna systems. Her research interests are wireless communications and information theory, VLSI signal processing, and reconfigurable architecture for wireless systems.

Conventional multi-input multi-output (MIMO) models are not efficient for assessing the benefits of multiple-antenna systems with an area limitation on antenna arrays in realistic propagation environments. Physical models, though capturing these factors, are too complex for tractable analysis. This talk presents a spatial channel model that takes into account these factors without sacrificing analytical tractability. In the model, the Green function for radiation is adapted to account for the array area limitation, and the clustering of physical paths observed in recent spatial channel measurements is exploited to obtain a concise description of channel scattering. Based on these modeling strategies, for a spherical array of effective aperture A in a physical environment of total angular spread Omega in solid angle, the number of independent channels (spatial degrees of freedom) is 2AOmega. The result helps assess the optimal number of antennas that should be put on the given transmit and receive areas in both single-user and multi-user environments. The analysis also sheds light on transceiver architectures that would utilize channel scattering more efficiently.

WEDNESDAY APRIL 13

Where is the RFID Puck Going Next?

Speaker: Sam Patadia, VP of Engineering, eSmart Source, Inc.
Time: 6:00 p.m. (pizza & soda, $1), 6:30 p.m. presentation
Place: National Semiconductor Credit Union, Bldg. 31, 955 Kifer Rd., Sunnyvale
RSVP: by email to rsvp@comsocscv.org
Web: www.comsocscv.org
See also: "Packaging Technology for RF RFID" on page 10

Sam Patadia is a senior information technology professional with over 25 years experience as project manager, software architect, systems engineer, instructor, and trainer in RFID application integration, software design and development, middleware, and data acquisition and control systems. Sam has taught several short courses in RFID technology at places like the Mitre Institute, National Institute of Standards and Technology, Software Development Forum, San Jose State University, and the Singapore Manufacturer's Federation.

He holds a bachelor's degree in Mechanical Engineering from the University of North Carolina and a Master's degree in Computer Aided Engineering from the same institution. He lives with his family in San Jose and enjoys visiting and photographing places with rocks, water, and trees.

Ever since the announcement of mandates to suppliers of Wal-Mart, Target, Albertsons, Best Buy and the U.S. Department of Defense to use radio frequency identification (RFID) to track pallets and cartons in the supply chain, RFID has garnered major interest in all corners of the high-tech industry. The casino industry is just the latest to find new uses for RFID technology. The United States and other nations are incorporating it into passports to catch counterfeits. Other people are planning to use RFID in mobile resource management. That means using both passive and active RFID technologies to track assets, work-in-process, returnable containers and vehicles in a close-loop supply chain. ABI Research estimates the RFID hardware and software market will surpass $4.6 billion by 2008 due to increased market activity, shipments, and mandates. Activities like supply chain, retail, consumer goods, and defense activity will continue to fuel growth, along with increased innovation in homeland security and smart payment markets.

The talk will briefly discuss various components of RFID eco system, role of EPCglobal and various factors which is fueling this growth in the market.

SCV Components, Packaging & Mfg Technology Chapter

Packaging Technology for RF & RFID

- **Wednesday, April 13, 2005**
- **Seminar: 1:00 – 5:30 PM**
- **Registration: begins at Noon**
- **Santa Clara Convention Center**
- **In conjunction with IEEE WESCON'05**
- **Includes free admission to WESCON exhibits**
- **Plenty of free parking**

For further information, see:

www.cpmt.org/scv/

SCV Engineering in Medicine and Biology

WEDNESDAY APRIL 20

Tactile Pressure Imaging: A New Tool For In Vivo Physiological Assessment for Gastroenterology

Speaker: Tom Parks, Ph.D., Sierra Scientific Instruments, Inc.
Time: Dinner with the speaker in the Stanford Hospital cafeteria at 6:15 PM (No reservation needed);
Presentation at 7:30 PM
Place: Clark Center Auditorium (see website for map)
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/embs/pages/upcoming.html

Tom Parks led the development of the ManoScan device and has been CEO of Sierra Scientific Instruments since 2003. He has more than 20 years of experience in technology development, corporate management, and entrepreneurial business. Dr. Parks has led teams of scientists and engineers in research and development initiatives involving aerospace sensors, control systems, and medical products. He founded and grew a sustained business producing engineering laboratory workstations. These systems are considered to be the standard in excellence in their field and are in use in over 400 universities world-wide. He has served as Senior Scientist and line manager for a major aerospace firm with oversight of an organization with a $30M annual budget. Dr. Parks received his Ph.D. from the University of Southern California in mechanical engineering and control systems. He has received numerous academic and technical achievement awards and has 11 patents issued and pending.

Gastroenterological motility disorders are significant both in terms of their impact on public health and on their demand on health care resources. More than 40 million Americans suffer from conditions that include gastroesophageal reflux disease (GERD), achalasia, dysphagia, incontinence, and pelvic floor dysfunctions. SSI has developed advanced pressure imaging systems with proprietary transducers to provide high fidelity pressure maps of the Gastrointestinal (GI) tract. This dramatically improves diagnostic clarity and simplifies clinical procedures when compared to existing technology.

Sierra has completed clinical validation, received FDA 510(k) clearance, and begun commercial production of its first product, the ManoScan™ motility visualization system. This technology was initially developed under NIH funding and is receiving enthusiastic support by experts and clinicians alike. It provides an order of magnitude more pressure transducers (i.e. increased resolution) than current technology to enable novel visualization of gastrointestinal motility physiology (the movement of contents through the GI tract). In this talk operating principles and features of this technology will be discussed; furthermore, developments underway for the next generation device with an additional order of magnitude increase in resolution will be described. A portable version of the device showing real-time pressure data collection and imaging will be demonstrated, and pressure image videos of clinical case studies of normal and pathological conditions will be shown.

SCV Solid State Circuits

THURSDAY APRIL 21

Power-aware and Temperature-aware Circuit Design

Speaker: Prof. Mircea R. Stan, University of Virginia
Time: Refreshments at 6:30 PM; Presentation at 7:00 PM
Place: Cadence Building 5, 2655 Seely Ave, San Jose
Cost: Donation requested for Refreshments
RSVP: Call 408 894-2646 (leave a message) or by email to ssc_scv_rsvp@yahoogroups.com
Web: www.ewh.ieee.org/r6/scv/ssc

Prof. Mircea R. Stan received the Ph.D. and M.S. degrees in Electrical and Computer Engineering from the University of Massachusetts at Amherst, and the Diploma in Electronics and Communications from "Politehnica" University in Bucharest, Romania. Since 1996 he has been with the Department of Electrical and Computer Engineering at the University of Virginia, where he is now an associate professor. Professor Stan is teaching and doing research in the areas of high-performance and low-power VLSI, mixed-mode analog and digital circuits, computer arithmetic, embedded systems, and nanoelectronics. He has more than eight years of industrial experience, and has been a visiting faculty at IBM in 2000 and at Intel in 2002 and 1999. Doctor Stan has received the NSF CAREER Award in 1997 and was a co-author on Best Paper Award at ISCA 2003 and SHAMAN 2002. He is a technical program chair for ISLPED 2005, was the general chair for GLSVLSI 2003 and has been on the technical committees for many conferences. He has been a Guest Editor for IEEE Computer in 2003 and an Associate Editor for the IEEE Transactions on CAS-I since 2003 and for IEEE Transactions on VLSI Systems in 2001-2002. He is a senior member of the IEEE, a member of ACM, Usenix, and also of Eta Kappa Nu, Phi Kappa Phi and Sigma Xi. Professor Stan is currently on a sabbatical leave at UC Berkeley, working on ultra low-power circuit design with professor Jan Rabaey in the Berkeley Wireless Research Center.

Power-aware design techniques aim to maximize performance under power dissipation and power consumption constraints; this scenario is common for high-performance systems. At the other extreme, low-power design techniques try to reduce power or energy consumption in portable equipment for some desired performance or throughput target. All the power consumed by a system gets eventually dissipated and transformed into heat: the power and related thermal issues affect performance, packaging, reliability, power delivery, environmental, and heat removal costs. Temperature is proportional to power density, not just power, so methods to reduce thermal effects can try either to reduce power, or increase area, or both. A thermal model is needed to accurately estimate the temperature landscape. This presentation will span power-aware and temperature-aware design techniques at the circuit level. First there will be some generic results related to figures of merit for power-aware and temperature-aware design and related optimal voltages, followed by issues related to electro-thermal simulation and necessary modeling aspects. This will be followed by the introduction of the concept of temperature-adaptive circuit design with some results that show increased performance across a wide temperature-range. Some issues related to active cooling and electro-thermal simulation with active cooling will be followed by thermal modeling requirements at the circuit level and the inclusion of thermal aspects in a temperature-aware design flow. Finally, if there is time, the presentation will end with a few recent results in the implementation of efficient bus-encoding circuits for power-aware SOC.

OEB Industry Applications

THURSDAY APRIL 21

Electrical Power Generation, Distribution, and Plant Automation on Modern Marine Vessels

Speakers: Robert Jackson; Robert Hammaker; Kirk Allen (Marine Engineers)
Time: No-host social at 5:30 PM; Presentation at 6:15; Dinner at 7:15; Presentation continues at 8:00
Place: Marie Callender's Restaurant (Garden Room); 2090 Diamond Blvd in Concord (near Concord Hilton)
Cost: dinner is $22 for IEEE members, $25 for non-members
RSVP: by April 20, to Gregg Boltz at gboltz@brwncald.com or telephone (925) 210-2571
Web: www.ewh.ieee.org/r6/oeb/ias.html

Robert Jackson holds a B.S. in Marine Engineering Technology, California Maritime Academy, 1976. United States Coast Guard License, Chief Engineer Unlimited Horsepower on Motor, Steam, or Gas Turbine Vessels. ISA CCST Level 1 Instrumentation Certification. ISCET Electronics Technician Certification. He has twenty four years experience as an engineering officer on merchant vessels. He has been teaching at the California Maritime Academy as a Maritime Vocational Instructor since 2000.

Robert Hammaker holds a B.S. in Marine Engineering Technology; California Maritime Academy, 1976. and an M.S. in Industrial and Systems Engineering; CSU San Jose 1992. U.S.C.G. Licenses Chief Engineer Steam Ships UNL. HP/3rd Asst. Eng. Motor Ships UNL. HP. P.E. Control Systems Engineering (State of California). He is Education Chair of the NORCAL Section of ISA and an instructor in Instrumentation and Measurement and Automation at CMA

Kirk Allen has his B.S. in Marine Engineering Technology, California Maritime Academy, 1980. United States Coast Guard License, Chief Engineer Unlimited Horsepower on Motor, Steam, or Gas Turbine Vessels. ISA CCST Level 1 Instrumentation Certification. ISCET Electronics Technician Certification. He is a member of San Francisco Bay Port Engineers Association with twenty five years experience as an engineering officer on merchant vessels.

Today's modern sea-going vessels are designed to carry very specific cargos and therefore the power generation and electrical distribution systems have to be as specialized as the vessel to meet those demands. Marine electrical systems will vary depending upon whether the sea-going vessel is a tanker, a freighter, or a passenger ship. Some other aspects which affect vessel design are the ever increasing requirements to provide for safety, reliability, and efficiency of the vessel. This meeting discussion will provide an overview of the most common types of electrical systems found aboard modern vessels and how they are integrated into the mission of the vessel.

Specific topics to be covered will include:

- Marine electrical power generation and distribution systems and how they are affected by the type of vessel service and prime mover.
- Various types of electric propulsion commonly used aboard merchant vessels.
- Overview of marine control systems and automation.
- Use of shaft generators to improve plant efficiency or provide emergency propulsion.
- Improvement of plant efficiency by production of electricity from waste heat.
- Overview of common vessel types and methods of propulsion.

By attending this meeting you will be informed and educated on how the electrical world aboard a marine vessel is different from what you may be used to on dry land. Come and join us for this interesting voyage!

SCV Instrumentation and Measurement

WEDNESDAY APRIL 20

ISO13485: A PDL and QSR Not Just for Medical Devices

Speakers: David A. Rivkin, Ph.D., Global Consulting and Patents Intl. and SciEssence, LLC

Time: Check-In/Networking: 6:30 PM, Presentation: 7:00 PM

Place: Cogswell College, Room 197, 1175 Bordeaux Drive, Sunnyvale

RSVP: to David Rivkin by April 15 at david.rivkin@ieee.org

Web: www.ewh.ieee.org/r6/scv/ims

ISO13485 defines a Quality Systems Program which encompasses Product Development Lifecycles. Its well-thought-out PDL can make the job of a product or program manager easier by eliminating process design guesswork. Automating the process can make it even simpler, but issues such as Literature Searches and Digital Signatures can be contentious.

OEB Communications

THURSDAY APRIL 21

Evolution of Mobile Wireless Technologies to the Year 2008

Speaker: Dr. Stanley Chia, Senior Director, Vodafone Group R&D-US

Time: 7:00 - 8:30 PM

Place: ChevronTexaco, 6001 Bollinger Canyon Road, San Ramon (map, directions on website)

Cost: none

RSVP: by April 20 to oeb@comsoc.org - for pizza order

Web: www.comsoc.org/oeb/

Stanley Chia, a technology strategist for Vodafone, will discuss his view of these questions and the future of the mobile wireless industry. Specific areas:

- Where is mobile wireless technology going?
- What is driving the changes in this space?
- What new products will we likely see?
- How will the service offerings change?
- How will China be a key influencer on these changes?

Dr. Stanley Chia is Senior Director, Vodafone Group R&D-US. He has been with the mobile communications industry for over 23 years and has held leadership positions in network operations, technology development, and strategy. Prior to joining Vodafone and its predecessor AirTouch, he worked for British Telecom (UK), and SmarTone Mobile Communications (Hongkong). He is a Senior Member of Institute of Electrical and Electronic Engineers and Fellow of the Institution of Electrical Engineers (UK)

SCV Professional Activities Committee for Engineers (PACE)

TUESDAY APRIL 26

Resume-Writing Clinic

Speakers/Leaders: Ken Doniger and Denise Pringle
Time: Dinner (optional) at 6 PM;
Panel/Discussion (no charge) 7 PM
Cost: $15 non-member/$10 member for dinner
Place: Cadence, Building 5, 2655 Seely Ave, San Jose
RSVP: To reserve your dinner, email Jonathan David (j.david@ieee.org) and pay at the door
Web: www.ewh.ieee.org/r6/scv/scv_pace.html

Denise Pringle has extensive experience in both domestic and international human resources. She has held executive positions in high technology and medical device industries. She has worked on transition teams for mergers and outsourcing and has had responsibility for training, organizational development, staffing and university relations. Denise received her Bachelor of Arts in Social Sciences with a concentration in History from San Jose State University. She is currently holds an adjunct faculty position at San Jose State University's Professional Development Center.

Ken Doniger is a long-time IEEE volunteer. He is currently on IEEE-USA's Employment and Career Services Committee. The aim of this committee is to educate IEEE members on employability and career issues. He has written a number of IEEE-USA presentations on these subjects. Ken has had seven jobs with five companies during his 20 years in the valley.

BRING YOUR RESUME!

SCV PACE presents an evening devoted to improving your resume. Topics will include:

1. Different types of resumes
2. Differences between paper and on-line resumes
3. What hiring managers look for

In addition, resumes from audience members will be critiqued. (This part of the evening is strictly voluntary.)

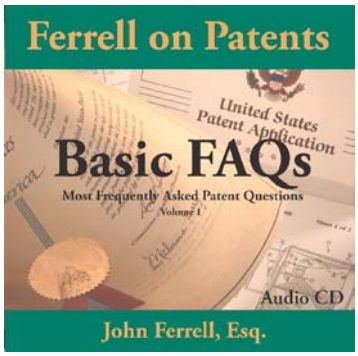
SCV Consultants' Network of Silicon Valley

TUESDAY APRIL 26

Who Owns Your Brain? - a Consultant's Guide to Patents

Speaker: John S. Ferrell, Esq., Carr & Ferrell LLP
Time: 7:00 PM Informal Networking;
7:30 Presentation
Place: Ramada Inn, 1217 Wildwood Ave (Fwy 101 frontage road, between Lawrence Expy and Great America Pkwy), Sunnyvale
Cost: none
RSVP: not required
Web: www.ieee-sv-consult.org/

John Ferrell is a founding partner of the Palo Alto-based Carr & Ferrell LLP, one of Silicon Valley's foremost intellectual property and corporate law firms. John has extensive experience in Strategic Counseling, Patent Opinion and Litigation Analysis, as well as Trademark, Copyright and Trade Secret matters. He's been listed by the Los Angeles Daily Journal as one of California's top Rainmakers, by San Jose Magazine as one of Silicon Valley's top Legal Eagles, and by San Francisco Magazine as one of Northern California's top lawyers. Distinguished by his demonstrated legal and technical expertise in computer, software and electronics issues, John has served as trusted counsel for many of the world's premier technology companies, including Apple Computer, Cisco, Fujitsu, Lucent, Philips, and Sony. In addition, he has authored a number of books targeted toward entrepreneurs and business professionals, including ***Patent Pro Se: The Entrepreneur's Guide to Provisional Patent Applications***. Further information about John and Carr & Ferrell LLP can be found at www.carrferrell.com/attorneys/bios/ferrell.html.



Have you wanted to get a patent to protect one of your ideas? As an individual or consultant without the corporate infrastructure of attorneys or a patent department, how do you get started? What do you have to do, what does it cost, and how do you get a return on your investment? John Ferrell, an eminent intellectual property attorney, will discuss owning your own creative output through patenting, and will be covering:

1. Brief Overview of Patents as Property
2. Consulting Contracts and Patents
3. Steps for Filing a Patent Application and Follow-Through to Issue
4. The Costs
5. V.Review of Recent California Cases Involving Inventions and Consultants

SCV Reliability

WEDNESDAY APRIL 27

When to Use HALT and When to use ALT

Speaker: Mike Silverman, Managing Partner, Ops A La Carte LLC
Time: 6:30 PM Snack Refreshments and social; 7:00 PM Presentation
Place: Hewlett-Packard, Cupertino (19111 Pruneridge Ave, near 280 and Wolfe), Building 48, Oak Room
Cost: none
RSVP: not required
Web and Map: www.ewh.ieee.org/r6/scv/rs/

Highly Accelerated Life Testing (HALT) is a great reliability technique to use for finding predominant failure mechanisms in a product or system. However, in many cases, the predominant failure mechanism is wearout. When this is the situation, we must be able to predict or characterize this wearout mechanism to assure that it occurs outside customer expectations and outside the warranty period. The best technique to use for this is Accelerated Life Testing (ALT). In this presentation, we shall look at when to use HALT and when to use ALT. We will also look at some case studies and examples on how we can use the techniques of ALT to find and measure wearout mechanisms.

Mike Silverman is Managing Partner of Ops A La Carte LLC, a Professional Consulting Firm focused on Reliability Engineering Services, Reliability Management, and Reliability Education to assist companies in developing and executing any and all elements of Reliability throughout an Organization and their Product's Life Cycle. He has over 20 years experience in reliability engineering, reliability management and reliability training. He is an experienced leader in reliability improvement through analysis and testing. Mike is also an expert in accelerated reliability techniques, including HALT and HASS. He set up and ran an accelerated reliability test lab for 5 years, testing over 300 products for 100 companies in 40 different industries. Through Ops A La Carte, Mike has had extensive experience as a consultant to high-tech companies, and has consulted for over 200 companies including Cisco, Ciena, Siemens, Intuitive Surgical, AeroGen, Abbott Labs, and Applied Materials. Mike has authored and published 7 papers on reliability techniques and has presented these around the world including China, Germany, and Canada. He has also developed and currently teaches a number of courses on reliability techniques.

Mike has a BS degree in Electrical and Computer Engineering from the University of Colorado at Boulder, and is a Certified Reliability Engineer (CRE) through the American Society for Quality (ASQ). Mike is a member of ASQ, IEEE, SME, ASME, PATCA, ASPMFG, and IEEE Consulting Network and is currently the IEEE Reliability Society Santa Clara Valley Chapter Chair."

WEDNESDAY MAY 4

US Electronics Industry Competitiveness in View of Globalization and Changing Technologies

Speaker: Prof. Rao Tummala, Director, Packaging Research Center, Georgia Tech
Time: 11:45 AM: Lunch;
12:15 PM: Pesentation
Cost: $15
Place: Ramada Inn, 1217 Wildwood Ave (Fwy 101 frontage road, between Lawrence Expy and Great America Pkwy), Sunnyvale
RSVP: Please reserve and pay in advance using our PayPal on-line system or email John Jackson at john.jackson@analog.com
Web: www.cpmt.org/scv/

Dr. Rao R. Tummala received the B.S. degree in Physics, Mathematics and Chemistry from Loyola College, India, the B.E. degree in Metallurgical Engineering from the Indian Institute of Science, Banglore, India, the M.S. degree in Metallurgical Engineering from Queen's University, and the Ph.D. degree in Materials Science and Engineering from the University of Illinois. He joined the faculty at Georgia Tech in 1993 as a Pettit Chair Professor in Electronics Packaging and as a Georgia State Research Scholar. He is also the Director of the Low-Cost Electronic Packaging Research Center funded by NSF as one of its Engineering Research Centers, the state of Georgia, and US electronics industry.

Prior to joining Georgia Tech, he was an IBM Fellow, where he invented a number of major technologies for IBM's products for displaying, printing, magnetic storage and multichip packaging. He is a Fellow of both the IEEE and the American Ceramic Society, a member of the National Academy of Engineering, 1996 General Chair of IEEE-ECTC, and 1996 President of ISHM. He was recently named by *Industry Week* as one of the 50 Stars in the US, for improving US competitiveness.

He is co-editor of the widely-used **Microelectronics Packaging Handbook**. He has published 90 technical papers and holds 21 U.S. patents and 44 other inventions. He received a number of awards including the David Sarnoff award,

(continued, next column)

IC and Systems Packaging, as a discipline, has been a stepchild in the electronics landscape within the US for decades. This has led the US to concentrate on ICs and systems in design and, in some special cases, fabrication and assembly. Tasks falling under the topic of "packaging" – which includes IC packaging, component fabrication, system-level boards and assembly – therefore became the focal point of Japan in the past, Taiwan and Korea in the more recent past, and China currently. .So, what is the future of this technology in the US and elsewhere?

Most industry experts foresee fundamental limits to IC integration limits for consumer and medical electronics. This has led industry and the electronics community to look for alternatives, both in the short and long run. In the short term, System-in-Package (SIP) and System-on-Package (SOP), which depend on co-developing the "package", seem to offer potential solutions to the above challenges, thus changing the technology landscape from its current stepchild mentality regarding "packaging". But US companies have gotten used to not investing in packaging and instead depending on the Far East. So, what is changing, if anything?

The so–called packaging field is almost as big as the IC field, in total market size. Yet, most universities think of this subject as manufacturing and assembly, without any basis in science. The above SIP and SOP technologies are fundamental and science–based, able to address combining the functions of RF, digital, optical, MEMS, sensors, fluidics, nano and bio in a synergistic fashion. Given this new perspective, the speaker addresses who will educate the new breed of engineers necessary to keep the industry competitive.

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the sustained technical achievement award from IEEE CPMT Society, the John Wagnon award from ISHM, the Materials Engineering achievement award from ASM-Intl, the distinguished alumni award from the University of Illinois, and the Arthur Friedberg Memorial award from the American Ceramic Society.

Dr. Tummala's current research interests include packaging materials (metals, ceramics, and polymers) and processes, mechanical properties of materials, thermal and electrical designs, and integrated passive components.

SCV Computer

SATURDAY MAY 7

One-Day Conference:
New Frontiers in Computing Technology - 2005

Sensor Networks – The New Environment

Time: 9:00 AM - 4:15 PM
Place: Braun Auditorium, Stanford University (free parking)
Cost: $50 Member, $60 non-Member, $25 student/unemployed (more, after 4/20)
Registration: on the NATEA website or contact Belle Tseng, belle@sv.nec-labs.com
Web: www.natea.org/NFIC/

Morning Program (tentative)
8:00-9:00: Registration

9:00-9:15: Opening Remarks
Michael Graebner, IEEE CS Chapter Vice-Chair

9:15-10:00: Keynote: **Sensor Network Overview**
Professor Leonidas Guibas, Stanford University

10:00-10:45: **An Application and Technology Framework for Wireless Sensor Networks**
John Suh, PhD, Crossbow Technology

11:00-11:45: **Wireless Networking**
Professor Prasant Mohapatra, UC – Davis

11:45-1:00: Lunch Break

Afternoon Program (tentative)
1:00-1:45: **Afternoon Keynote**
Professor C. K. Lee, National Taiwan University

1:45-2:30: **Distributed Algorithms**
Dr. Gary Bradski, Intel Corporate Technology

2:45-3:30: **System Design including Transceivers, Transmitters and Receivers**
Chipcon

3:30-4:15: **Applications of Sensor Networks**
Professor Khan, Taiwan

4:15: Program Closing

In each of the last six years, the Santa Clara Valley Chapter of the IEEE Computer Society and the North America Taiwanese Engineers' Association (NATEA) have jointly brought to the Bay Area engineering communities the "**New Frontiers in Computing Technology**" Conference. This year, we bring to you the 7th Annual Conference focusing on the emerging Sensor Networks technologies.

Sensor Networks move computing from being a distinct entity within an environment to being a seamless part of the environment. This profound change touches both computing and the way we operate in daily life. Sensor Networks and the technologies they represent are fast becoming a new reality.

Starting with the hardware, this conference will cover such vital issues as wireless networking, distributed algorithms and applications at the engineering level. The aim of this conference offering is to provide members of the engineering communities with enough basic information to be able to make decisions regarding sensor networks and their applicability in new and emerging technical environments.

Registration Fees (Online or Mail):

	Before 4/30/2005*	After 4/30/2005 or On-site
IEEE, SNF, or NATEA Members	$50	$60
Non-Members	$60	$70
Students/Unemployed Members	$25	$30

All prices include meals.
*Payment must be received by 4/30/2005 via mail (check) or online (Paypal)

CONFERENCE CALENDAR

The **CONFERENCE CALENDAR** is a service to our IEEE Members. It outlines upcoming IEEE workshops and conferences in the Bay Area. Please submit items to the GRID Editor: editor@e-grid.net.

Conferences are also encouraged to purchase display space in the **GRID.pdf** and publicize their events on our website and in our **e-GRID** email notification service. For the Conference Publicity flyer, please download:

www.e-grid.net/docs/conf-flyer.pdf

April 12-14: **IEEE Wescon at the Santa Clara Convention Center**

With the theme "D2M: Design to Manufacture Solutions," Wescon brings together dozens of tutorials and seminars for professional and technical development, alongside exhibits featuring tools and products for the design engineer. A large portion of the program – sessions, keynote talks, panels, pavilions – are without cost. Plan to come and spend the full day. Plenty of free parking.
For more information, see

Pages 9-13 in this GRID

May 17-19: **The Vision Show & Conference West comes to San Jose**

North America's leading showcase of machine vision components, systems and solutions comes to San Jose. Held every other year in the heart of Silicon Valley, the Show is the perfect venue for suppliers and system integrators to meet with system designers and users to share information on new products and real-world solutions.

See Page 7 in this GRID

May 23-25: **Aeroacoustics Conference is in Monterey**

This international forum for scientists and engineers from industry, government, and universities allows the exchange of knowledge and results of current studies and discussion of directions for future research. Papers cover all aspects of the generation, propagation, measurement, modeling, and control of vehicle noise, as well as the effect of noise on structures and individuals.

See Page 5 in this GRID

May 24-26: **Aircraft Noise and Emissions Reduction Symposium**

A high-level, multidisciplinary technical symposium bringing together leading engineers, scientists, researchers, government and civil aviation officials, industry, and policy makers to discuss the topics and issues of aircraft noise and emissions reduction.

See Page 5 in this GRID

May 24-27: **World Wireless Congress 2005: Converging the Broadband Wireless and Mobile**

WWC'05 is a conference focused on research, development and design of emerging wireless and mobile communications focusing on B3G and 4G technologies, with tutorials, sessions, and networking. It is held this year in Palo Alto.
WWC'05 extends a $100 Instant Rebate to IEEE members, for all registrations by April 15th. Please write rebate code "SF0415CAL" on the registration form. For more information, see

www.b3g.org

June 21-23: POFWorld '05 comes to the Santa Clara Convention Center

Plastic Optical Fiber for Home and Auto – sessions, tutorials, exposition. POF'05 extends a 10% discount to any IEEE Member.

See **www.pofworld.com**