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# PATENT SPECIFICATION

DRAWINGS ATTACHED

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COMPLETE SPECIFICATION

## Improvements in or relating to Electronic Digital Computing Machines

We, NATIONAL RESEARCH DEVELOPMENT CORPORATION, of 1, Tilney Street, London, W.1, a British Corporation established by Statute, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to electronic digital computing machines and is more particularly concerned with improved data word storage arrangements in such machines.

It is accepted that the utility of an electronic digital computing machine, particularly one of the so-called universal type adapted to deal with a wide range of computing problems as compared with a specialist type of machine designed for one specific form of task only, is determined to a large extent by the data word storage capacity thereof. The provision of a very large capacity data word storage in which each word storage location or address is capable of either immediate or high speed access is both expensive and conducive to large physical machine size and as an alternative it is already accepted practice to employ only a limited amount of immediate or high speed access storage and to provide a secondary or backing store of much lower access speed and then to arrange for the transference, usually in blocks of predetermined number, of data words to and fro between the two stores under the control of special transfer orders inserted at appropriate positions in the order programme.

Such a system of high speed and secondary storage, while useful in reducing cost and apparatus bulk, is far from convenient in use, especially by operators of limited experience, in view of the essential need to organise the required data word transfers at the appropriate times and to retain precise identification of the various data words during their change of storage addresses.

One object of the present invention is the provision of an improved data word storage system which reduces or even eliminates the above disadvantages and inconveniences while still employing only a limited amount of high access speed storage in conjunction with an appropriate amount of secondary or backing storage.

This object is achieved, in accordance with one basic aspect of the invention, by assigning a unique address identification definable in any instruction or order to every word storage location which is available in both the high access speed storage and at least a part of the secondary or backing storage, by arranging the address selection means of at least a part of the high access speed storage so that the address signal to which it is responsive can be altered from time to time in accordance with the particular address identification of any word storage location or group of storage locations whose signal content may be temporarily present therein and then providing means for effecting automatically a transfer from the secondary or backing storage to the high access speed storage of the signal content of a word storage location which is defined by the address identification signal of a currently operative order or instruction whenever such address identification signal fails to elicit response in the address selection means of the high speed storage and simultaneously modifying the said part of the high speed storage address selection means in accordance with the different address identification of the transferred signal. Preferably, any such automatic transfer operation is arranged to deal with a block of storage locations of predetermined number and is arranged also to be preceded

by an automatic transfer to the secondary storage of the contents of the particular high speed storage address location or locations into which the newly required data is to be placed.

In order that the above and other features of the invention may be more readily understood, one embodiment thereof will now be described by way of illustrative example only and with reference to the accompanying drawings, in which:

Figure 1 is a block schematic diagram illustrating the principle components of a data word storage arrangement for an electronic digital computing machine; while

Figure 2 is a more detailed but nevertheless schematic diagram of a memory-comparator device and a code signal generator device each forming part of the arrangement shown in Figure 1.

Reference is first made to Fig. 1. In this embodiment, the immediate access or high speed data word storage 10 includes eight magnetic core store matrices, each capable of registering 1024 data words and jointly providing accommodation for a total of sixteen blocks each of 512 words. The secondary data word storage 11 comprises a plurality, e.g. four, magnetic drum stores although, as with the high speed storage, the actual form of the storage devices used is of no concern to the present invention. Each drum store is assumed to have 128 separate block storage locations each capable of registering a single block of 512 data words.

Selection of any word storage location in any of the sixteen 512-word blocks in the high speed store 10 and selection of the required one of such sixteen 512-word blocks is effected by address selection means 12 which may comprise diode tree circuits of known form. Word location selection within any one 512-word block is effected by address digit signals applied by way of a multiple bus 13*a* and derived from the nine address digits *d*3, *d*4---*d*11 of an instruction or control word while block selection is effected by four further address digit signals, hereinafter called the *p*0, *p*1, *p*2, and *p*3 signals, applied by way of multiple bus 13*b*. The signals for selecting a word location within any 512-word block are supplied directly from the instruction or control word sensing means in the control system, shown schematically by the block symbol 14, but the *p*0---*p*3 signals for effecting block selection are supplied from a four-channel multiple code signal generator device 15 under the control of nine further address digits *d*14, *d*15---*d*22 of an instruction or control word in a manner which will be described later. Digits *d*12 and *d*13 are spare positions which are not used.

Selection of the required one of the 512 different 512-word block storage locations in the magnetic drum store 11 is effected by the associated address selection means 16 which may also comprise tree circuits. The signals controlling such selection are applied by way of multiple bus 18*a* and control gate means 18*b* and are also derived, although indirectly, from the nine further address digits *d*12---*d*22 of the instruction or control word.

The code signal generator device 15 is adapted to provide, in response to an output signal on any one of its input leads 19*a*, 19*b*---19*p*, a four-digit binary output consisting of the aforesaid *p*0, *p*1, *p*2 and *p*3 signals on the multiple bus 13*b*, the form of such output signals being related to the particular input lead by which the input signal is supplied. Thus, if the signal is on the first input lead 19*a*, the emitted output signal is indicative of binary digits 0000 to select the first block 0 of the store 10 whereas energisation of input lead 19*p* causes emission of binary digit signal 1111 to select the sixteenth block of the store 10. The device 15 may conveniently comprise sixteen separate trigger circuits with appropriate connections to the bus leads from their opposite polarity output terminals through suitable isolating buffer diodes or the like but a simplified and preferable form will be described later with reference to Fig. 2.

The input signals to the device 15 are provided by a composite memory-comparator circuit arrangement 21 which is adapted to receive the nine separate address digit signals provided by the control system 14 in response to the address digits *d*14, *d*15---*d*22 of an instruction or control signal operative in the control system, to compare each of such supplied digit signals with the existing stored signal states of separate memory devices in each of the sixteen separate vertical banks of nine such memory devices and to provide an output signal on that one of the leads 19*a*, 19*b*---19*p* associated with the respective vertical banks if, but only if, all of the signal states of the memory devices on that bank coincide precisely with the corresponding digit signals from the control system 14.

The circuit arrangement 21 may comprise sixteen separate banks of nine combined trigger and associated equivalence detecting circuits, one input to each equivalence detecting circuit being derived from the associated trigger circuit and the other input being derived from the related address digit signal supplied from the control system 14. The outputs from the nine equivalence detecting circuits of each group are then applied to a nine-input coincidence gate whose output provides the signal on the associated lead 19*a*---19*p* to the device 15. An alternative simplified and preferred form of the arrangement 21 is, however, also shown in Fig. 2 and will now be described.

Referring now to Fig. 2, the memory comparator circuit arrangement 21 comprises sixteen separate banks of nine two-stable-state trigger circuits. Thus the first bank comprises the trigger circuits T1*a*, T2*a*, T3*a*---T9*a*, the second bank the trigger circuits T1*b*, T2*b*, T3*b*---T9*b* and so on. For simplicity of illustration only two of the remaining banks, those of the eleventh bank of trigger circuits T1*k*, T2*k*---T9*k* and the sixteenth bank of trigger circuits T1*p*, T2*p*---T9*p* are shown but the remainder are precisely similar.

The triggering and the resetting inputs of each trigger circuit T1*a*, T2*a*---T9*a* of the first bank are connected by way of individual leads of a multiple bus 30 to related digit storage elements of one address in a separate and so-called V store 31 (Fig. 1) with suitable interposed gate means whereby, when desired, each of the trigger circuits of such first bank can be set to their '0' or '1' state, as the case may be, in accordance with the stored digit values of such V store elements. The triggering and resetting inputs of each trigger circuit of each of the other banks are similarly connected over the multiple bus 30 to related digit storage elements of fifteen further addresses in the V store, there being one address in such V store exclusive to each bank of the circuit arrangement 21.

The respective '0' and '1' state outputs of each of the trigger circuits T1*a*, T2*a*---T9*a* are connected through individual gate circuits G1*a*0, G1*a*1, G2*a*0, G2*a*1---G9*a*0, G9*a*1 to a common lead 32*a* which is connected to the input of an inverter 33*a*. The '0' and '1' state outputs of the second bank trigger circuits T1*b*---T9*b* are similarly connected through individual gate circuits G1*b*0---G9*b*1 to a common lead 32*b* leading to an inverter 33*b*. The similar '0' and '1' state outputs of the remaining banks of trigger circuits are similarly arranged, the common leads of the eleventh and sixteenth banks being shown at 32*k* and 32*p* respectively with their associated inverters 33*k* and 33*p*.

The controlling inputs of the '0' state output gates G1*a*0, G1*b*0---G1*k*0---G1*p*0 associated with the first trigger circuit of each bank are connected in parallel to lead 34*a* while the controlling inputs of the opposite '1' state output gates G1*a*1, G1*b*1---G1*k*1---G1*p*1 are similarly connected in parallel to lead 34*b*. Lead 34*b* is connected to the output of an inverter 35 whose input is connected to lead 34*a* which in turn is connected to the control system 14 to be supplied with a signal representing the value of the address digit *d*14 of the instruction or control word operative in such control system. The remaining gates are similarly connected, those associated with the second trigger circuit in each bank being controlled by the signalled value of the address digit *d*15 and so on with the gates associated with the ninth trigger circuit in each bank controlled by the signalled value of the address digit *d*22 of such instruction or control word.

The output from each of the inverters 33*a*, 33*b*---33*k*---33*p* is applied over an associated input lead 19*a*, 19*b*---19*k*---19*p* to the code signal generating arrangements 15 which merely comprise the connection of such input leads 19*a*, 19*b*---19*p* (through suitable buffer or blocking diodes not shown) to that combination of the four leads forming the multiple bus 13*b* (see Fig. 1) to set up the *p*0, *p*1, *p*2 and *p*3 signals which represent the binary code signal appropriate to that block of the high speed storage 10 which is related to each particular bank of the arrangement. Thus, the lead 19*a* which is associated with the first bank of the arrangement 21 and is related to the first block 0 of the high speed storage 10, is not connected to any one of the leads providing the signals p0---p3 so as, effectively, to cause signalling of the binary value 0000. Lead 19*b*, which is associated with the second bank of the arrangement 21 and the second high speed storage block, is connected only to the lead carrying the signal *p*0 so as to provide the binary signal 0001 whenever lead 19*b* is energised. The remaining leads 19*c*---19*p* are similarly arranged, lead 19*k* being, as shown, connected (through isolating diodes or the like) to the leads carrying the signals *p*1 and *p*3 to provide the binary signal 1010 and the lead 19*p* to all four leads carrying the signals *p*0, *p*1, *p*2 and *p*3 so as to provide the binary signal 1111 when the lead is energised.

Additionally, the output of each of the inverters 33*a*, 33*b*---33*b* is connected through an isolating buffer or diode to a common lead 40 which is connected through a gate 36*a* to an equivalence output lead 37, and also by way of an inverter 38 and a further gate 36*b* to a non-equivalence output lead 39.

The manner of operation of this memory comparator circuit arrangement 21 is as follows. As will be described later, each of the trigger circuits T1*a*, T2*a*---T9*a* of the first bank of trigger circuits of the arrangement 21 is set to its '0' '1' state in accordance with the particular 9-digit block number which identifies, in an instruction word, the particular block of 512 words which is, at the moment, registered in the first block 0 of the high speed storage 10. The second and remaining banks of trigger circuits are or may be likewise set in accordance with the 9-digit block numbers of the fifteen further blocks of 512 words registered in the remaining blocks of the high speed storage 10.

Upon the application of an instruction to

the control system 14 in the normal way during operation of the machine, the address digits $d14 - - - d22$ of that word signal the 9-digit block number of the required data word and cause corresponding energisation of one or other of the gate control lead pairs 34*a*, 34*b*. It will be noted that a value '1' input for any address digit from the control system 14 will condition the '0' value output gates of the associated trigger circuits to open whereas a '0' value input will condition the '1' value output gates of such trigger circuits to open. Accordingly, only when each of the trigger circuits of a bank is set to a state corresponding to the '0' or '1' value of the related address digit input from the control system 14 will the transmission of at least one active trigger circuit output to the related common lead, such as 32*a*, be inhibited. Whenever the setting of one or more of the trigger circuits of a bank does not coincide with the pattern of digit signals $d14 - - - d22$ supplied from the control system, the associated common lead $32a - - - 32p$ will become energised. As a result, the related inverters 33*a*, $33b - - - 33p$ will then cease to provide an output and the related lead $19a - - - 19p$ will not be energised. If, however, the trigger circuits of one bank are set precisely in accordance with the signalled values of the digits $d14 - - - d22$, the common lead of that bank will fail to become energised because the trigger circuit output gate which is in the active one of the trigger circuit output leads will, in each case, be the gate which is not conditioned to open by the related address digit signal. In this case, the absence of an input signal to the related inverter of the group $33a - - - 33p$ will cause the emission of an output signal by that inverter and the consequential energisation of the code signal output leads to form the $p0$, $p1$, $p2$ and $p3$ signals which identify the block in the high speed storage where the block of words having the signalled block address is at the moment located.

For example, supposing the eleventh block of the high speed storage contains a particular word block whose first and last address digits are '0' and '1' respectively. The trigger circuit T1*k* will be in the '0' state and the trigger circuit T9*k* will be in the '1' state. If the active instruction word has address digits $d14 - - - d22$ conforming precisely to the address digit configuration set upon the trigger circuits of the eleventh bank, then the $d14$ signal will be '0' and the $d22$ signal will be '1'. Lead 34*a* supplying the trigger circuits $T1a - - - T1k$ will not be energised but, owing to the inverter 35, the lead 34*b* will be energised. This will condition gate G1*k*1 to open but not gate G1*k*0. This latter is, however, the one in the active output of the trigger circuit and accordingly the possible energisation of common lead 32*k* therethrough is blocked. Similarly with each of the other trigger circuits of the bank. The resultant output from inverter 33*k* energises code signal generator leads $p1$ and $p3$ giving the code signal output 1010 which will select the eleventh block in the high speed storage 10.

Whenever one of the inverters $33a - - - 33p$ provides an output in such manner, lead 40 is also energised so that, at a time determined by the application of a strobing pulse SP to gates 36*a*, 36*b*, an output signal indicating that coincidence has been established and that the required word block is in the high speed storage 10 is transmitted to the control system over lead 37. Conversely, if none of the trigger circuit banks has a setting state pattern corresponding to the block address digit configuration, then every common lead $32a - - - 32p$ will be energised and no inverter $33a - - - 33p$ will provide an output. In this case, the inverter 38 will supply an output to gate 36*b* and when this is opened by the aforesaid strobing pulse SP a signal indicating non-equivalence and indicative that the required word block is not in the high speed storage 10 will be transmitted to the control system over lead 39.

Returning now to Fig. 1, the read outputs and write inputs of the high speed storage 10 are connected by the usual multiple busbars of a parallel mode machine to the various other machine elements which, in the interest of clarity, are not shown since they form no part of the invention. In addition, however, the read outputs of the high speed storage 10 are connected by way of a multiple transfer bus 25, which includes outward transfer gate means 25*a*, to the write inputs of the secondary storage 11 while, in like manner, the read outputs of such secondary storage 11 are connected by way of a further multiple transfer bus 26, which includes inward transfer gate means 26*a*, to the write input of the high speed storage 10.

In addition to the normal machine control system 14, which is of the usual and well known form including an order to instruction register for retaining each sequentially presented order or instruction signal and therefrom providing the necessary series of gate control and other signals, the arrangements of the present invention include a second or transfer control system 27 which is interconnected with the machine elements and with the main control system 14 through switch circuit means illustrated schematically at 28 and which, when actuated, serve to transfer control of the machine from the normal control system 14 to the transfer control system 27. At the instant when changeover from normal control to transfer control takes place, the only-partially completed operation of the machine to deal with the

normal instruction in the control system 14 becomes suspended with the said instruction still retained in the control register of the control system 14.

The transfer control system includes an order register and this is supplied, in a manner analogous to the normal control arrangements of computing machines with a series of special transfer orders forming a transfer sub-routine which is permanently registered to an associated transfer programme store 29 which may be of any convenient type such as a magnetic core store matrix or an endless magnetic tape loop. As already stated, the V-store 31 has sixteen separate storage locations, one for each block of the high speed storage 10, and is provided with address selection means 39 for selecting any one of the sixteen locations in the V-store 31 under the control of an address signal supplied over multiple bus 42 from the transfer control 27. The transfer control 27 is also supplied with a series of signals representing the eleven block address digits $d14 - - - d22$ of the (now suspended) normal instruction registered in the normal control system 14. Signals are supplied to the write input of the V-store 31 by way of bus 43 from the transfer control system 27 while read out signals from such V-store 31 are supplied by way of bus 44, bus 18*a* and gate means 18*b* to the address selection means 16 of the secondary storage 11 and also by way of multiple bus 45 and gate circuit means 46*a*, 46*b* - - - 46*p* to each of the trigger circuit banks of the memory comparator circuit 21. The transfer control system 27 is also connected to the address selection means 12 of the high speed storage 10 by way of bus 13*c*. It will be understood that, in the interests of simplicity and ease of understanding, many circuit details and connections have been omitted; the precise form of these is of no particular interest since many possible arrangements are already well known and established in the art.

Other details of the arrangement not so far dealt with will become apparent from the following description of the manner of operation. A normal instruction or order word, forming part of a computing order programme, is applied in the usual way to the control system 14 and this results in the provision of a group of address digit signals $d0$, $d1 - - - d22$ defining a particular required data word. The digit signals $d0$ and $d1$ are used to define one of four separate character-signal groups in any half-word part of a word storage location while the digit $d2$ is used to define which of the two half-word parts may be required. These three digit signals are accordingly applied to means 24 for effecting the desired half-word and character selection within any selected address location. Such means 24 may conveniently comprise gate circuits in each of the individual read-out and write-in leads of the output and input bus lines of the high speed storage 10.

The address digit signals $d3 - - - d11$ and $d14 - - - d22$ provide a unique identification for each word storage location whether it be in the high speed store 10 or the secondary store 11. The nine digit signals $d3 - - - d11$, by direct application over bus 13*a* to the address selection means 12, serve to select a particular one of the 512 locations in a storage block if, but only if, it is in the high speed store 10. The remaining address digit signals $d14 - - - d22$ define the particular block out of a maximum of 512 blocks and these signals are initially applied to the memory comparator circuit 21.

In a manner as explained later, the nine trigger circuits, e.g. the trigger circuits T1*a* - - - T9*a*, of each of the sixteen banks of such trigger circuits in the circuit arrangement 21 have been pre-set to register the respective block identification of the sixteen 512-word signal blocks already held in the high speed storage 10. If the applied address digit signals $d14 - - - d22$ due to the operative instruction or control word in the control system 14 define one of the sixteen different block numbers already set up in the arrangement 21, coincidence will be registered, as already explained, in one only of the sixteen banks and that bank will provide an output signal to the related input lead 19*a* - - - 19*p* and as a result the appropriate binary signal will be emitted by the code signal generator 15 to set the address selection means 12 in the manner requisite to select the desired word block. The simultaneously developed equivalence signal on lead 37 is fed to the normal control system 14 where it initiates the appropriate reading or writing or other form of machine operation which thereafter proceeds in the wholly normal manner.

In the contra case, where the address digit signals $d14 - - - d22$ supplied by the control system 14 in response to the currently operative instruction or control word define a block number which is different from any of the sixteen already set up in the circuit arrangement 21 and which is therefore not registered in the high speed storage 10, no coincidence will be registered in any of the sixteen banks and no output signal will be present on any of the leads 19*a* - - - 19*p*. At the same time, a non-equivalence signal will be provided on lead 39 and this is applied to the switch means 28 which immediately operate to transfer machine control from the normal control system 14 to the transfer control system 27, at the same time retaining the current and only partially-completed normal instruction in the system 14.

The transfer control system 27 now com-

mences to work through its predetermined sub-routine to transfer instructions drawn one by one from the transfer programme store 29. The first transfer operation is one of clearing one of the 512-word blocks of the high speed storage 10 to that one of the block locations in the secondary store 11 which is identified by the number at present set up on that bank of trigger circuits of the memory comparator circuit 21 which is related to the high speed storage block chosen for clearance. In the machine being described, each of the sixteen 512-word blocks of the high speed storage is cleared sequentially in regular order and for this purpose the transfer control system 27 includes the usual and well known means for altering the value of a number defining an address by adding or subtracting 1 at each operation with the transfer sub-routine. Thus, if the last previous transfer operation cleared and refilled block N of the speed storage 10, the block next to be cleared and refilled in the operation being described will be block N+1 (or N−1).

As will become more apparent later, the particular nine-digit number set up on any bank of trigger circuits of the memory comparator circuit 21 is also registered in the related (N+1) storage address of the V-store 31. The first order of the transfer sub-routine from transfer control store 29 is accordingly one defining the four digits signalling the 512-word block (N+1) in the high speed storage which is next in order to be cleared and a function control signal to read that address (N+1) of the V-store 31 to the address selection means 16 of the secondary store 11. The next transfer sub-routine order is to transfer the contents of the defined high speed storage block (N+1) to the defined secondary storage block by way of the outward transfer bus 25 and its gate means 25*a*, the latter being supplied with the requisite gate opening signals from the transfer control system 27.

When such transfer operation to clear a block of the high speed storage has been completed, the next transfer sub-routine order specifies the clearance of the same address (N+1) in the V-store 31 (i.e. that related to the now-cleared high speed storage block) and the writing therein, over bus 43, of the nine digit signals *d*14 - - - *d*22 of the suspended normal order of the control system 14. The next transfer sub-routine order specifies the reading of the same address (N+1) in the V-store, i.e. the nine-digit number of the required block, over transfer bus 44, bus 18*a* and gate means 18*b* to set the address selection means 16 of the secondary storage 11 and, at the same time, over bus 45 to the related bank (N+1) of the trigger circuits of the comparator circuit 21, the appropriate gate means 46*a* - - - 46*p* being opened at the same time by the address signal (N+1) used for controlling the V-store address selection means 39, whereby the related bank of trigger circuits of the comparator circuit 21 becomes set up with the identification number of the new block. The next transfer sub-routine operation is to use the same (N+1) high speed block address signal for application over bus 13*c* to the address selection means 12 of the high speed storage to select the cleared block in the latter and thereafter to transfer the defined block in the secondary storage 11 to the high speed storage 10 by way of inward transfer gate 26*a* (opened by signal from transfer control 27) and bus 26.

The completion of this last word transfer operation marks the end of the transfer sub-routine in the transfer control 27 which thereupon causes release of the switch means 28 to revert machine control back to the normal control system 14. When this occurs, the re-presented digit signals *d*14 - - - *d*22 immediately find coincidence with the setting of the (N+1) bank of trigger circuits in the memory comparator circuit 21 to allow machine operation to proceed to complete the suspended instruction held in the control system 14.

WHAT WE CLAIM IS:—

1. A data word storage arrangement for an electronic digital computing machine in which a unique address identification signal form definable in any computing instruction or order used within the machine is assigned to every data word storage location available in both a high access speed storage and in at least a part of a secondary or backing storage and in which the address selection means of at least a part of said high access speed storage is so arranged that the address signal to which it is responsive can be altered from time to time in accordance with the particular address identification of any word storage location whose signal content may be temporarily present therein.

2. A data word storage arrangement for an electronic digital computing machine according to claim 1 which includes means for effecting automatically a transfer from said secondary or backing storage to said high access speed storage of the signal content of a word storage location which is defined by the address identification signal of a currently operative computing instruction whenever said address identification signal fails to elicit response in the address selection means of the high access speed storage and means for simultaneously modifying the said part of the high access speed storage address selection means in accordance with the different address identification of the transferred signal.

3. A data word storage arrangement according to claim 2 in which said automatic transfer operation is arranged to deal with a block storage locations of predetermined

number including the particular one defined by the aforesaid address identification signal of the currently operative computing instruction.

4. A data word storage arrangement according to claim 2 or 3 in which said automatic transfer operation is preceded by an automatic transfer to said secondary storage of the signal content of the particular high access speed storage address location or block of such address locations into which the newly required data word or block of data words is to be placed.

5. A data word storage arrangement according to claim 4 in which said preceding automatic transfer to said secondary storage is arranged always to be back to that location or block of locations which was/were defined by the address identification signal used to effect its initial transfer from such secondary storage to said high access speed storage thereby to maintain an uninterrupted record of its identity.

6. A data word storage arrangement according to any of the preceding claims which includes a memory comparator circuit arrangement comprising at least one bank of separate memory elements each for registering the value of a different address digit of a word address signal, means for applying and comparing a group of address digit signals, one with each of the values registered by said memory elements and means for providing alternative output signals indicating respectively equivalence or non-equivalence of said registered digit values with said applied digit signals.

7. A data word storage arrangement according to claims 3 and 6 in which said memory comparator circuit arrangement comprises memory elements for dealing only with those digits of an address identification signal which define the identification number of said block of storage locations.

8. A data word storage arrangement according to claim 6 or 7 in which said memory comparator circuit arrangement includes means for generating a special address selection control signal for operating the address selection means of said high access speed storage upon the establishment of equivalence of said registered digit values with said applied signals.

9. A data word storage arrangement according to claim 7 or claims 7 and 8 in combination in which said memory comparator circuit arrangement comprises a plurality of separate banks of said memory elements for registering respectively the different block identification numbers of a plurality of separate blocks of storage locations whose signal contents are present in different parts of said high access speed storage.

10. A data word storage arrangement according to claim 9 in which said group of address digit signals are applied simultaneously to the related memory elements of each of said banks of memory elements.

11. A data word storage arrangement according to any of claims 6—10 in which said bank or each of said banks of memory elements comprising a plurality of two-stable-state trigger circuit devices providing alternative '0' or '1' state outputs in accordance with the state into which they are set and in which each of said '0' and '1' state outputs of the trigger circuits of the bank or each bank is connected to a common lead through a coincidence gate circuit, the '0' state output gate of each trigger circuit being connected to a signal lead energised when the applied address digit signal is of value '1' and the '1' state output gate of each trigger circuit being connected to a signal lead energised when the applied address digit signal is of value '0' whereby said common lead fails to become energised from any trigger circuit of said bank only when every trigger circuit set to a '0' or '1' state corresponding to the '0' or '1' values of the respective address digit signals.

12. A data word storage arrangement according to claim 2 or any claim dependent thereon in which said automatic transfer is effected by transferring control of the machine from the normal control system to a separate transfer control system.

13. A data word storage arrangement according to claim 12 in which said separate transfer control system includes storage means for registering the particular address identification of very word storage location or of each block of such storage locations whose signal content is present in said high access speed storage.

14. A data word storage arrangement according to claim 12 or 13 in which said separate transfer control system is arranged to control the machine by a predetermined sub-routine of transfer control orders registered in associated storage means.

15. A data word storage arrangement substantially as described and as illustrated in the accompanying drawings.

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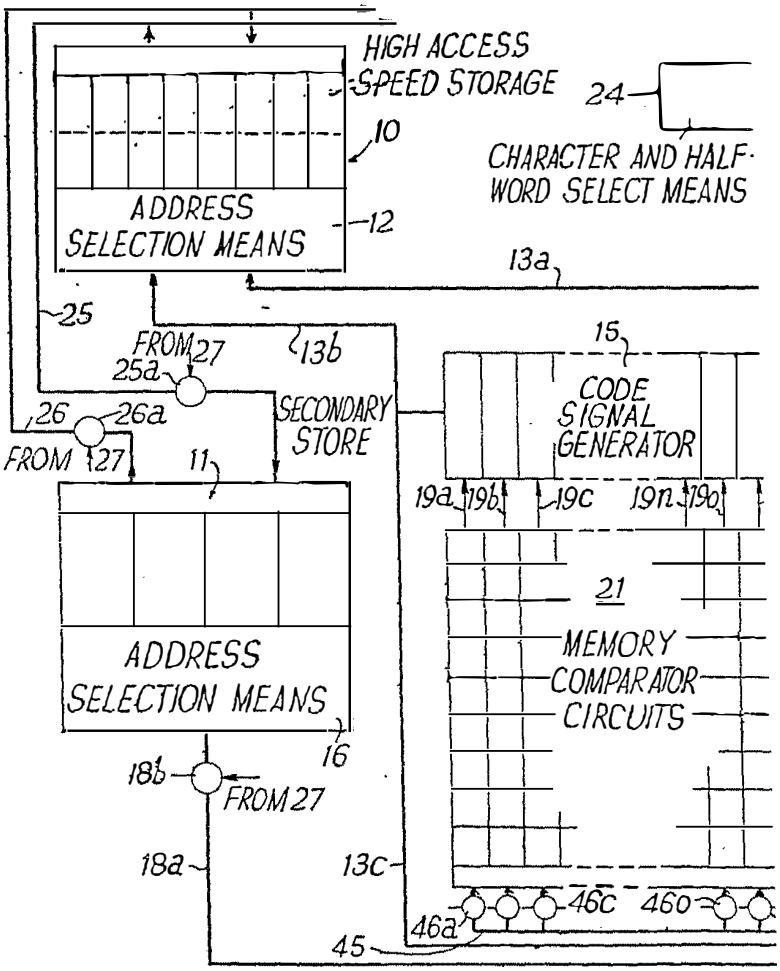
HIGH ACCESS SPEED STORAGE
24
10
CHARACTER AND HALF-WORD SELECT MEANS
ADDRESS SELECTION MEANS
12
13a
25
FROM 27
13b
15
25a
CODE SIGNAL GENERATOR
26
26a
SECONDARY STORE
FROM 27
11
19a
19b
19c
19n
19o
21
MEMORY COMPARATOR CIRCUITS
ADDRESS SELECTION MEANS
16
18b
FROM 27
18a
13c
46c
46o
46a
45

976499 COMPLETE SPECIFICATION
2 SHEETS *This drawing is a reproduction of the Original on a reduced scale*
Sheet 1

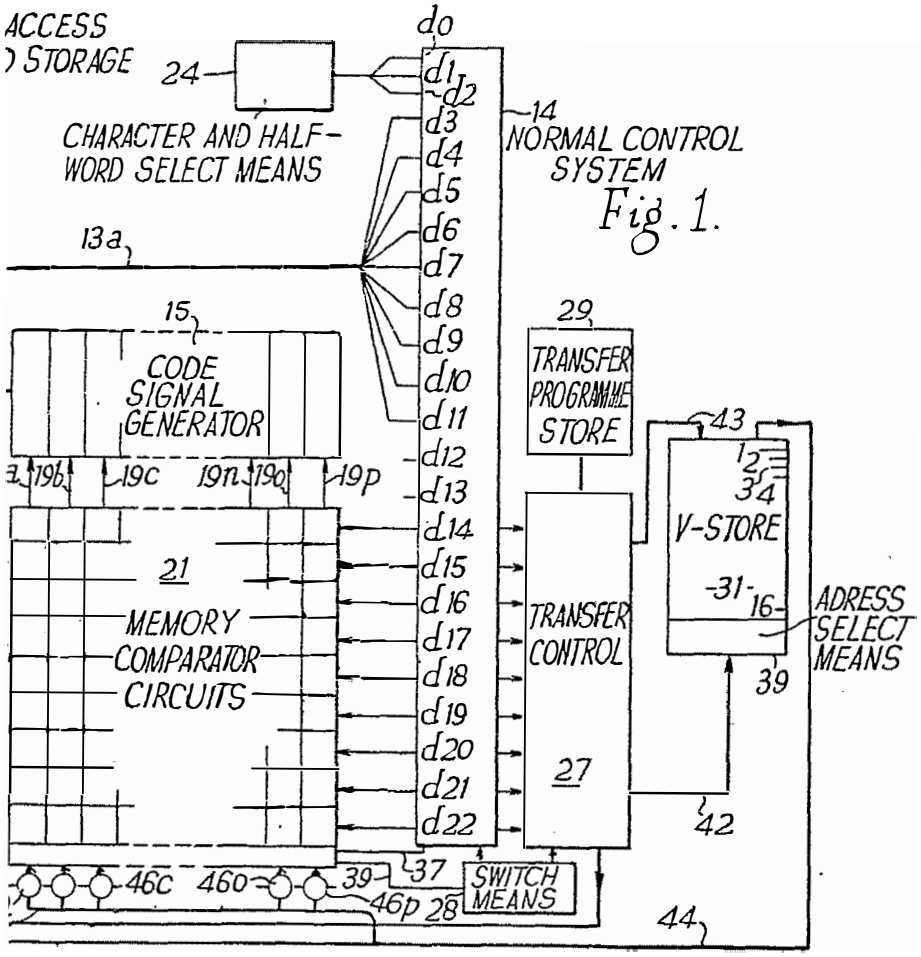


Fig. 1.

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**Sheet 1**

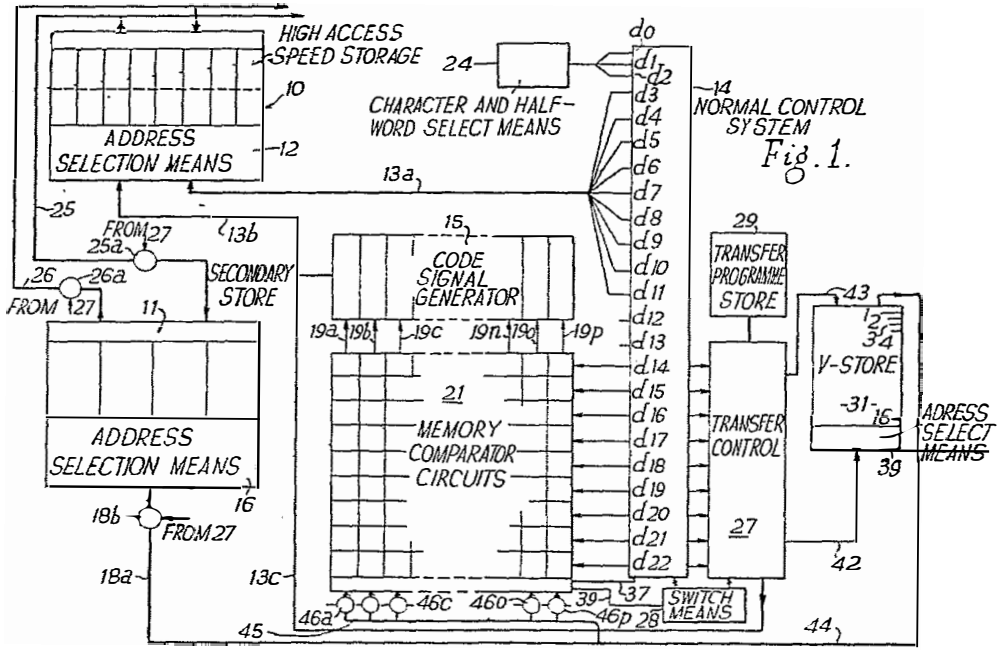


Fig. 1.

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Sheet 2

Fig. 2.