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May 2005

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Chapter Meetings and Events

SCV-Rel - 4/27 | When to use HALT and when to use ALT - predicting a wearout mechanism, with case studies ... [more]

SCV-PSES - 4/28 | Product Liability situations relating product safety to the topic of liability ... [more]

SCV-LEOS - 5/3 | Combining Light with Motion: Hybrid Integration of Light Emitters and Detectors with MOEMS Systems .[more].

SVEC - 4/30 | Career Workshop: Investing in Our Career and Retraining for Our Future - half-day Saturday event ... [more]

SCV-CPMT - 5/4 | US Electronics Industry Competitiveness in View of Globalization and Changing Technologies - IC packaging ... [more]

SCV-CS - 5/7 | Sensor Networks – The New Environment - Saturday seminar, at Stanford ... [more]

SCV-AP - 5/10 | Terahertz Radiation via IC Technology - efficient alternatives for generatng THz radiation with IC technology ... [more]

SCV-EDS - 5/10 | Nanoelectronics: Now or Never? - fundamental limits as a way to understand nanoscale transistors ... [more]

SCV-Com - 5/11 | IEEE 802.11 Wireless LAN Architecture: New Protocols and New Deployment Strategies - increased capacity...[more]

SCV-CPMT - 5/11 | Shielding Packaging for High-Cost Electronics - RF and EMI shielding designed in up-front ... [more]

SCV-MTT - 5/12 | Technologies for Overcoming Interconnect Parasitics and Reducing Costs in the 10 to 100 GHz Range ... [more]

SCV-Mag - 5/17 | Dynamics in Magnetic Micro- and Nanostructures - confined spin wave properties and the noise spectrum ... [more]

SCV-EMB - 5/18 | Architecture and Application of Wireless Communication In Glucose Monitoring for Diabetes... [more]

SCV-IM - 5/18 | Samplify: Lossless and Lossy Data Compression for Instrumentation Signals at 10+ Msamp/sec ... [more]

SCV-SSC - 5/19 | Analog Circuit Design with Submicron Transistors - a methodology that is simple and intuitive, yet accurate ... [more]

OEB-IAS - 5/19 | Arc Flash Hazard Assessment and Electrical Safety in the Workplace - the analysis prior to working on equipment ... [more]

OEB-Comm - 5/19 | Network Visibility @ Wire-Speed for Visibility, Security and Capacity Planning - a modern standards-based network monitoring and export protocol (sFlow) ... [more]

SCV-CNSV - 5/24 | Why Advertising Doesn't Work for Consultants - insights into why many consultants don't see results ... [more]

SCV-CPMT - 6/8 | Reliability Issues in Lead-Free Soldering - the important issues for lead-free solder interconnection systems, including components, PCBs, and solder joints ... [more]

SCV-EMB - 6/15 | A Pendant-Geometry CT Scanner for Breast Cancer Detection: Design and Initial Clinical Assessment - ... [more]

Upcoming Conferences in the Bay Area

May 7: **SENSOR NETWORKS – The New Environment**, held at Stanford Univ **[more]**

May 17-19: **The Vision Show & Conference**, San Jose Convention Ctr – Machine Vision Exhibits **[more]**

May 23-25: **Aeroacoustics Conference**, Monterey Exhibits, seminars, tutorials **[more]**

May 24-26: **Aircraft Noise and Emissions Reduction Symposium**, Monterey plenary-track session, tutorial, mini-expo **[more]**

June 21-23: **POFWorld '05**, Santa Clara Conv'n Ctr **Plastic Optical Fiber** for Home and Auto – sessions, tutorials, exposition **[more]**

Upcoming Courses

Transnational MBA Program - Cal-State East Bay Informational sessions in May throughout SF Bay Area **[more]**

May 4: **SOP vs SiP vs SOC: Technology Directions for Systems Implementation** IC Packaging Seminar - staff from Georgia Tech **[more]**

May 17: **Influential Communication** listening, filtering, speaking - at KLA-Tencor, San Jose **[more]**

May 21-22: **Computational Aeroacoustics: Methods and Application** **[more]**

Professional Skills Courses from EMS, CPMT, ETA:

Breakthrough Project Management
- May 4-5 at LSI Logic, Milpitas
- June 7-8 at H-P, Cupertino

Clear Business, Technical, and e-mail Writing
- May 5 at Cypress Semiconductor, San Jose
- May 18 at National Semiconductor, Santa Clara

Problem-Solving Using Non-Linear Systems Thinking
- June 9 at H-P, Cupertino

Getting Things Done Across Organizational Borders
- May 10 at Sybase, Dublin

Presentation Skill for Engineers, Managers
- May 13 at Cypress Semiconductor, San Jose

Influential Communication
- May 17 at KLA-Tencor, San Jose
- June 15 at National Semiconductor, Santa Clara
[more]

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IEEE GRID

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IEEE **GRID** is the monthly newsmagazine of the San Francisco Bay Area Council of the Institute of Electrical and Electronics Engineers, Inc. As a medium for both news and opinion, the editorial objectives of IEEE **GRID** are to inform readers in a timely and objective manner of newsworthy IEEE activities taking place in and around the Bay Area; to publish the official calendar of events; to report on IEEE activities of a national and international scope; and to serve as a forum for comment on areas of concern to the engineering community by publishing contributed articles, invited editorials and letters to the editor.

IEEE GRID is published as the **GRID** Online Edition residing at www.e-GRID.net, and in a handly printable **GRID.pdf** edition, and also as the **e-GRID** sent by email twice each month to more than 24,000 Bay Area members and other professionals.

From the editor . . .

Most of the Societies in the IEEE have a Distinguished Lecturer program. Certain technologists are recruited as DLs based on their knowledge of particular topics and their willingness to present their specialty talk worldwide. Any local Chapter can ask one of these DLs to speak to their members at an evening meeting or perhaps at a seminar. The Society picks up some or all of the travel and lodging costs of the DL. To see who the DLs are for your Society, check its website.

This month, the Santa Clara Valley Magnetics Society chapter has invited Prof. Burkard Hillebrands, IEEE Magnetics Society Distinguished Lecturer, traveling from the Technical University of Kaiserslautern, Germany. When world-renowned speakers visit the SF Bay Area, it's always a good idea to hear what they have to say. See for details.

As it turns out, I'm a DL for the Components, Packaging & Manufacturing Technology Society. During the month of May I'll be giving my DL talk at a workshop in Garmish-Partenkirchen, Germany, and at an academic conference in Vienna. While I'm there, I'm also chairing meetings of my CPMT Society *Transactions* editors, both in Garmish and in Vienna. And I'm dropping in on faculty at universities in Warsaw and Wroclaw, in Poland. I always try to cover a number of assignments on any particular trip.

Do you have a specialty that would interest one of our local Chapters? If so, give the Chapter officers a call to see if they would like to feature you at an upcoming meeting. After all, there's a lot of practice required on the road to becoming a DL!

Paul Wesling editor@e-grid.net

NOTE: This PDF version of the IEEE GRID – the **GRID.pdf** – is a monthly publication and is issued a few days before the first of the month. It is not updated after that. Please refer to the Online edition and Interactive Calendar for the latest information: **www.e-GRID.net**

IEEE Professional Skills Courses

Engineering Management & Components, Packaging and Manufacturing Technology Societies, SCV Chapters

new! Influential Communication

Date/Time: Tuesday, May 17, 8:30AM-4:30PM
Instructor: Barry Flicker
Location: at KLA-Tencor, San Jose

Without a context of mutual value, trust and respect, techniques alone prove useless. This one-day course asks participants to evaluate their current communication environment according to these standards. We then begin to examine the three primary communication skills - clear goal setting, making our message audience-appropriate, and active/empathic listening - so that participants understand how to improve their working relationships in any situation. This is a highly experiential workshop applicable for people at every level of the organization.

Session Objectives
- Identify things that we may be doing or failing to do that contribute to difficult communication.
- Apply S.M.A.R.T. Criteria to set clear, mutually agreed upon objectives.
- Resolve questions of competence through effective application of the situational speaking model.
- Listen through difference to manage conflict and build influence.

Getting Things Done Across Organizational Borders

Date/Time: Thursday, May 10, 8:30AM-4:30PM
Instructor: Dr. Andrew Oravets
Location: Sybase, Dublin

This seminar introduces you to innovative practices for dealing with people who do not report to you -- but whose assistance and support are critical.

Key Topics
- Learn new strategies for people within or outside your control
- Obtain "mind share" from people who have other priorities
- Reaching people who are now perceived as "impossible"
- Explore alternative ways to describe projects and proposals
- Learn new negotiation tools to bargain for results
- Employ practical techniques for making clear, concise requests
- Reach mutually satisfying agreements

Improve your skills – register for a skills class. Bring a team!

For complete course information, schedule, and registration form, see our website:

www.effectivetraining.com

"IEEE is a magnet bringing engineers together. Engineering is a language that transcends bureaucracy and nationalism. It gives to us all a common language and understanding."

Ya-Qin Zhang, IEEE Fellow
Managing Director, Microsoft Research Asia

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www.ieee.org/join

11th AIAA/CEAS Aeroacoustics Conference

23-25 May (Course: 21-22 May)

Co-located with the

AIAA/AAAF Aircraft Noise and Emissions Reduction Symposium

24-26 May (Tutorial: 23 May)

Hyatt Regency Monterey
Held on the magnificent Monterey Peninsula

The 11th **AIAA/CEAS Aeroacoustics Conference** provides an international forum for scientists and engineers from industry, government, and universities to exchange knowledge and results of current studies and to discuss directions for future research. Papers that cover all aspects of the generation, propagation, measurement, modeling, and control of vehicle noise, as well as the effect of noise on structures and individuals, will be presented at the conference.

KEYNOTE TALKS

"Prospects for a Quiet Future in Aeronautics"
   Dr. Richard W. Wlezien, NASA

"Finding Hope Amidst the Challenges – Views of Aircraft Noise and Emissions Reduction"
   John-Paul Clarke, MIT

PROGRAM

Over 30 sessions in 7 tracks, including:

- Acoustic/Fluid Dynamic Phenomena
- Airframe/High-Lift Noise
- Computational Aeroacoustics Methods
- General Acoustics
- Jet Noise Diagnostics
- Fan Noise Measurement and Modeling
- Jet Aeroacoustics Simulation
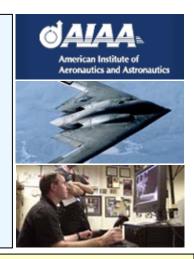- Advanced Testing Techniques: Phased Arrays, Sensors and Methods, Facilities
- Community Noise and Metrics

TWO-DAY COURSE (Saturday, Sunday)

Computational Aeroacoustics: Methods and Application

(fee includes full admission to Aeroacoustics Conference)

Computational issues unique to aeroacoustics - CAA time marching algorithms - Radiation, inflow and outflow boundary conditions - numerical solutions - nonlinear wave propagation - multi-scales acoustics - applications to aeroacoustics problems

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The **AIAA/AAAF Aircraft Noise and Emissions Reduction Symposium** is a high-level, multidisciplinary technical symposium bringing together leading engineers, scientists, researchers, government and civil aviation officials, industry, and policy makers to discuss the topics and issues of aircraft noise and emissions reduction. The objective is to review challenges and opportunities faced by manufacturers, local communities, air carriers, air navigation service providers, airports, governmental institutions, and non-governmental organizations to address noise and emission abatement and to develop holistic solutions that will ameliorate the pressures associated with air traffic growth.

PRE-SYMPOSIUM TUTORIAL

On Monday afternoon, Barry Scott, Director of the FAA Liaison Office, NASA Ames Research Center, will teach a course providing an overview of air traffic topics in preparation for discussions during the Symposium.

PROGRAM

The format of ANERS is a series of invited talks in a single-session, panel format and includes leading experts in the field. The program features balanced representation from Europe, the United States, and other regions of the world.

MINI-EXPO

There will be a Mini-Expo where organizations and manufacturers display information about their programs and products.

REGISTER TODAY!

   Special low student, retired rates!
   For full information on both events:

www.e-grid.net/conf/aero-aners.html

The Vision Show and Conference – *West*
May 17-19, 2005
San Jose Convention Center
Tutorials   Sessions   Exhibits

Machine vision solutions for many industries, including:

- Electronics
- Medical Devices
- Security
- Aerospace
- Automotive
- Lab Automation
- Semiconductors
- Pharmaceuticals
- Biometrics
- Food & Beverage
- Defense/Military
- Consumer Products

The Vision Show West is North America's leading showcase of machine vision components, systems and solutions. Held every other year in the heart of Silicon Valley, the Show is the perfect venue for suppliers and system integrators to meet with system designers and users to share information on new products and real-world solutions.

Morning and afternoon technical sessions include talks by Industry experts giving presentations designed specifically to provide practical, real-world solutions to attendees. Topics cover all key issues that current and potential users need to know in order to successfully apply machine vision.

Half-day Tutorials (Monday, May 16)

- How to Select Machine Vision Components
- Lighting & Optics: The Basics
- Integrating Machine Vision Systems: From Basic Concepts to Systems Integration
- Advanced Lighting & Optics

Sessions (Tues-Wed AM/PM, Thurs AM)

- Machine Vision Software for Part Identification/Classification
- Non-Visible Imaging
- Advances in Camera Technology
- Integrating a Machine Vision Solution into Capital Equipment
- Advances in Vision Guidance
- Advances in Smart Cameras and Sensors
- Successful and Emerging Machine Vision Applications
- Selecting the Right Camera Interface for Your Needs
- Latest Developments in Gigabit Ethernet for Machine Vision
- Advances in 3-D Machine Vision Technology

(For details on session papers, see the website)

Sponsored by the
Automated Imaging Association

Exhibits

The world's leading machine vision system and component suppliers will exhibit at **Vision West**, North America's largest and most targeted machine vision event. These are just some of the products you'll find:

- Complete Vision Systems
- Input/Output Devices
- Lighting Equipment
- Peripherals
- Vision Processors
- Cameras
- Frame Grabbers
- Lenses & Optics
- Smart Sensors
- Vision Software

New Product Showcase

Visit the **New Product Showcase** on our website to preview the newly introduced products that you can see at Vision West.

Straight Talk on New Products

In this special area right on the show floor, you'll hear presentations from technical experts at companies with new products on display, and get updates on important industry issues such as the Camera Link ® and GigE Vision™ standards. These talks will run continually throughout the show — they're free to all show and conference attendees!

Register Today

Free admission to the three days of exhibits – register on the website!

With the **VISION SOLUTIONS PASS**, you can attend four days of in-depth tutorials and conference sessions for just $825. You'll also receive a free copy of the conference proceedings CD and the tutorial handouts — great resources to take back to your company.

For information, and to register on-line:

www.machinevisiononline.org

To display at **Vision West**, contact Carol Calini at (203) 483-5774 or carol@reuterexpo.com

SENSOR NETWORKS – The New Environment
7th IEEE/NATEA Annual Conference
Place: Braun Auditorium, Stanford University
Date: Saturday, May 7th, 2005

This one-day conference focuses on emerging Sensor Networks technologies. Sensor Networks move computing from being a distinct entity within an environment to becoming a seamless part of the environment. This profound change touches both computing and the way we operate in daily life. Sensor Networks and the technologies they represent are fast becoming a new reality. In order to better understand this emerging technology and its complex interactions, we present this one-day conference on Sensor Networks. Starting with the hardware, this conference will cover such vital issues as wireless networking, distributed algorithms and applications at the engineering level. The aim of this conference offering is to provide members of the engineering communities with enough basic information to be able to make decisions regarding sensor networks and their applicability in new and emerging technical environments.

Program:
- **Keynote: Sensor Network Overview**
- **Hardware Design in Integration of Sensor Networks**
- **Wireless Networking**
- **Distributed Algorithms**
- **System Design including Transceivers, Transmitters and Receivers**
- **Applications of Sensor Networks**

REGISTER TODAY!
Rregister early to ensure a seat for this technical program.

REGISTRATION	By April 30	After April 30
IEEE MEMBER	$50.00	$60.00
NON-MEMBER	$60.00	$70.00
STUDENT (fulltime)	$25.00	$30.00
UNEMPLOYED*	$25.00	$30.00

Registration includes lunch. More information and PayPal payments:

www.natea.org/NFIC/

IEEE Professional Skills Courses

Breakthrough Project Management

Date/Time: Wed-Thurs, May 4-5, 8:30AM-4:30PM
Instructor: Barry Flicker
Location: LSI Logic, Milpitas (add'l session: June 7-8)
Fee: $575 for IEEE Members; $625 non-members

This 2-day course provides participants with a common methodology, terminology and tools that produce more efficient results and increased buy-in through improved visibility, reliability and consistency.

Key Topics: - Project Barriers & Breakthroughs - Team Development & Leadership - Define POS & Scope - Use the Trade-Off Flexibility Matrix - Make Fact-Based Decisions - Define Tasks - Create Work Breakdown Structure - Analyze Risks & Contingency Plans - Diagram Dependencies (CPM,PERT) - Manage the Project: Step-by-Step - Effective Meetings

> "The methods and processes used for this class were not just tools and packages. They were a way to approach, manage and think, as well as communicate and deliver projects with less firefighting. I particularly liked the flexibility matrix, POS, risk analysis and critical path analysis."

SCV Chapters, Engineering Management & Components, Packaging and Manufacturing Technology Societies

Presentation Skills for Engineers

Date/Time: Friday, May 13, 8:30AM-4:30PM
Instructor: Peter Rosselli
Location: Cypress Semiconductor, San Jose
Fee: $425 for IEEE Members; $475 non-members

This program is for professionals who are called upon to make formal or informal presentations – to deliver their ideas clearly, demonstrate confidence and enthusiasm, and handle objections with poise. Class size is limited to 10 participants.

Key Topics: - - Conquer "stage fright" - Use effective eye contact & gestures - Optimize opening & closing statements - Make key information memorable - Create & use visual aids - Use notes skillfully - Handle challenging questions & difficult people

Improve your skills – register for one of these classes, or for others coming up in May and June. Bring a team!

For complete course information, schedule, and registration form, see our website:

www.effectivetraining.com

"SOP vs SiP vs SOC: Technology Directions for Systems Implementation"

Emerging and Disruptive Packaging Technologies for the Next Decade

Featuring the technical staff of the NSF-sponsored Georgia Tech Packaging Research Center

Held at the Ramada Inn, Sunnyvale
Wednesday, May 4, 2005, from 8:00 AM - 5:30 PM

System-on-Package (SOP) refers to ultra-miniaturization of systems using thin-film component integration, in contrast to transistor integration for ICs. This provides a "Moore's Law" for system integration, akin to Moore's Law for IC integration. The SOP paradigm changes the current chip-centric System-on-Chip (SOC) methodology to a cheaper, faster-to-market IC-package-system co-design flow. The advantages of the SOP paradigm over SOC appear overwhelming due to SOPs design simplicity, lower cost and higher system functional integration, improved electrical performance, and without the intellectual property issues that dominate SOC. SOP is also different from and offers advantages over 3D packaging and SIP. The 3D packaging is a general concept for stacking of similar or dissimilar chips (such as DRAMS or DRAMs) with processor and flash memory. The SIP can go beyond, to embed both active and passive devices. The SOP focuses on integrating heterogeneous system functions, optimizing the integration of digital, RF, optical, sensor and other technologies.

DATE & TIME:
- Wednesday, May 4, 2005, from 8:00 AM - 5:00 PM
- Registration: 7:30 AM
- Lunch: Noon - 1:15 PM
- Reception/dinner following: 5 - 8 PM (optional)

COST:
- IEEE Members: $95
- Non-Members: $150
- After April 29: Member $110, Non-Member $165
- Includes lunch, class booklet, refreshments, and admission to the optional evening reception

WHO SHOULD ATTEND:
Packaging engineers, photonics engineers, systems engineers, thermal and mechanical engineers, PCB layout engineers, design, process, failure analysis, and reliability engineers and managers.

PROGRAM:

Morning Session (8:00-11:45 AM)
"**SOP: The Second Moore's Law for Systems in Contrast to First Moore's Law for ICs**," Prof. Rao Tummala, Director, GaTech Packaging Research Center
"**Mixed Signal SOP Design**," Prof. Madhavan Swaminathan
High-Density/High-Throughput Chip-to-chip Optical Interconnect SOP for Next-Generation Computing and Communication Systems," Prof. Gee-Kung Chang
"**RF/Wireless 3D Packaging and Integration: Current Challenges and Solutions**," Prof. Manos Tentzeris

Lunch Session (12:00-1:15 PM – includes Buffet Lunch)
Keynote Presentation: "**US and Electronic Industry Competitiveness in view of Globalization and Changing Technologies**," Prof. Rao Tummala

Afternoon Session (1:30-5:00 PM)
"**High Performance Nano Materials for Electronic, Photonic and MEMS Packaging**," Prof. C.P. Wong
"**Multigigahertz Test Methods for SOPs and Wafer-level Packaged Devices**," Prof. David Keezer
"**Thermo-Mechanical Reliability and Design Challenges for Next-Generation Microsystems Packaging**," Prof. Suresh Sitaraman

Evening Session (5:00-8:00PM – optional)
Informal Reception and Social with Drinks and Light Dinner. Meet the Georgia Tech PRC faculty members for informal discussions

For Seminar registration information, please visit the Chapter website:

www.cpmt.org/scv

Use our PayPal registration and payment system online, or mail in your registration with a check.

WEDNESDAY APRIL 27

When to Use HALT and When to use ALT

Speaker: Mike Silverman, Managing Partner, Ops A La Carte LLC
Time: 6:30 PM Snack Refreshments and social; 7:00 PM Presentation
Place: Hewlett-Packard, Cupertino (19111 Pruneridge Ave, near 280 and Wolfe), Building 48, Oak Room
Cost: none
RSVP: not required
Web and Map: www.ewh.ieee.org/r6/scv/rs/

Highly Accelerated Life Testing (HALT) is a great reliability technique to use for finding predominant failure mechanisms in a product or system. However, in many cases, the predominant failure mechanism is wearout. When this is the situation, we must be able to predict or characterize this wearout mechanism to assure that it occurs outside customer expectations and outside the warranty period. The best technique to use for this is Accelerated Life Testing (ALT). In this presentation, we shall look at when to use HALT and when to use ALT. We will also look at some case studies and examples on how we can use the techniques of ALT to find and measure wearout mechanisms.

Mike Silverman is Managing Partner of Ops A La Carte LLC, a Professional Consulting Firm focused on Reliability Engineering Services, Reliability Management, and Reliability Education to assist companies in developing and executing any and all elements of Reliability throughout an Organization and their Product's Life Cycle. He has over 20 years experience in reliability engineering, reliability management and reliability training. He is an experienced leader in reliability improvement through analysis and testing. Mike is also an expert in accelerated reliability techniques, including HALT and HASS. He set up and ran an accelerated reliability test lab for 5 years, testing over 300 products for 100 companies in 40 different industries. Through Ops A La Carte, Mike has had extensive experience as a consultant to high-tech companies, and has consulted for over 200 companies including Cisco, Ciena, Siemens, Intuitive Surgical, AeroGen, Abbott Labs, and Applied Materials. Mike has authored and published 7 papers on reliability techniques and has presented these around the world including China, Germany, and Canada. He has also developed and currently teaches a number of courses on reliability techniques.

Mike has a BS degree in Electrical and Computer Engineering from the University of Colorado at Boulder, and is a Certified Reliability Engineer (CRE) through the American Society for Quality (ASQ). Mike is a member of ASQ, IEEE, SME, ASME, PATCA, ASPMFG, and IEEE Consulting Network and is currently the IEEE Reliability Society Santa Clara Valley Chapter Chair.

THURSDAY APRIL 28

Product Liability

Speaker: Lewis Bass, author of "Products Liability: Design and Manufacturing Defects"

Time: 5:30 PM dinner, 7:00 PM Presentation

Dinner: El Torito Mexican Restaurant, 2950 Lakeside Drive, Santa Clara (just two blocks north of the meeting site) - no host

Place: Presentation at 7:00 PM at Applied Materials, Bowers Cafe, 3090 Bowers Ave, Santa Clara

Cost: dinner is no-host; no cost for presentation

RSVP: none

Please note that this month's meeting of the Santa Clara Valley Chapter of the IEEE Product Safety Engineering Society will be held on THURSDAY (instead of on our normal Tuesday).

Socialize with your colleagues at dinner (no host) from 5:30 to 7:00 pm at El Torito Mexican Restaurant, -- just two blocks north of the meeting site.

We are fortunate to have Mr. Lewis Bass speaking on a topic that underlies much of what we do as Product Safety Engineers -- Product Liability. He previously has addressed our group on that topic with a very interesting and useful presentation.

Lewis Bass, P.E., holds a BS in Mechanical Engineering, an MS in Industrial and Systems Engineering, and a JD in Law, as well as being a registered professional safety engineer. He has taught Safety Science for the University of Southern California Institute of Safety and Systems Management and hazard analysis and liability prevention for the University of Wisconsin - Madison and UCLA.

Mr. Bass is the author of "Products Liability: Design and Manufacturing Defects, 2nd Edition", has published numerous papers and is a frequent speaker on safety law and product liability at professional seminars and conferences. He is a member of the American Society for Quality, American Society of Safety Engineers, National Fire Protection Association, Semiconductor Safety Association and the American Bar Association.

Combining Light with Motion: Hybrid Integration of Light Emitters and Detectors with SOI-based MOEMS Systems

Speaker: Prof. Joel Kubby, EE Dept, University of California at Santa Cruz
Time: Networking and Pizza Social at 7:00 pm, Presentation at 8:00
Cost: none
Place: National Semiconductor Credit Union Auditorium, 955 Kifer Road, Sunnyvale
RSVP: please RSVP to rsvp-scv-leos@ieee.org
Web: www.ieee.org/scv/leos

Joel Kubby is an Associate Professor in the Department of Electrical Engineering at the University of California at Santa Cruz. His research is in the area of Micro-Electro-Mechanical Systems (MEMS). He works closely with the NSF Center for Adaptive Optics at UC Santa Cruz for applications of optical MEMS in astronomy and vision sciences. Prior to joining the faculty at UCSC in January 2005, he was a technical manager in the Xerox Wilson Center for Research and Technology in Rochester, New York, where he led a research group working on the applications of MEMS technology for printing. He has over 50 patents in the design, fabrication and applications of fluidic and optical MEMS, and is a registered patent agent with the United States Patent and Trademark Office.

A multidisciplinary team of end users and suppliers (Maxim Integrated Products, Microcosm Technologies, Microscan Systems, Optical Micro-Machines, Standard MEMS and Xerox) have combined to develop a novel yet broadly enabling process for the design, fabrication and assembly of Micro-Opto-Electro-Mechanical Systems (MOEMS). A key goal is to overcome the shortcomings of the polysilicon layer used for fabricating optical components in a conventional surface micromachining process. These shortcomings include the controllability and uniformity of material stress that is a major cause of curvature and deformation in suspended microstructures. The approach taken by the consortium to overcome these issues is the use of the single-crystal-silicon device layer of a silicon-on-insulator (SOI) wafer for the primary structural layer for MOEMS devices. Since optical flatness and mechanical reliability are of utmost importance in the realization of such devices, the use of the silicon device layer is seen as an excellent choice for devices which rely on the optical integrity of the materials used in their construction. A three-layer polysilicon process consisting of two structural layers is integrated on top of the silicon device layer. This allows for the formation of sliders, hinges, torsional springs, comb drives and other actuating mechanisms for positioning and movement of the optical components. Flip-chip bonding techniques are also being developed for the placement of edge and surface emitting lasers on the front and back surfaces of the silicon wafer, adding to the functionality and broadly enabling nature of this process.

SCV Components, Packaging and Manufacturing Technology

WEDNESDAY MAY 4

US Electronics Industry Competitiveness in View of Globalization and Changing Technologies

Speaker: Prof. Rao Tummala, Director, Packaging Research Center, Georgia Tech
Time: 11:45 AM: Lunch;
12:15 PM: Pesentation
Cost: $15
Place: Ramada Inn, 1217 Wildwood Ave (Fwy 101 frontage road, between Lawrence Expy and Great America Pkwy), Sunnyvale
RSVP: Please reserve and pay in advance using our PayPal on-line system or email John Jackson at john.jackson@analog.com
Web: www.cpmt.org/scv/

Dr. Rao R. Tummala received the B.S. degree in Physics, Mathematics and Chemistry from Loyola College, India, the B.E. degree in Metallurgical Engineering from the Indian Institute of Science, Banglore, India, the M.S. degree in Metallurgical Engineering from Queen's University, and the Ph.D. degree in Materials Science and Engineering from the University of Illinois. He joined the faculty at Georgia Tech in 1993 as a Pettit Chair Professor in Electronics Packaging and as a Georgia State Research Scholar. He is also the Director of the Low-Cost Electronic Packaging Research Center funded by NSF as one of its Engineering Research Centers, the state of Georgia, and US electronics industry.

Prior to joining Georgia Tech, he was an IBM Fellow, where he invented a number of major technologies for IBM's products for displaying, printing, magnetic storage and multichip packaging. He is a Fellow of both the IEEE and the American Ceramic Society, a member of the National Academy of Engineering, 1996 General Chair of IEEE-ECTC, and 1996 President of ISHM. He was recently named by *Industry Week* as one of the 50 Stars in the US, for improving US competitiveness.

He is co-editor of the widely-used **Microelectronics Packaging Handbook**. He has published 90 technical papers and holds 21 U.S. patents and 44 other inventions. He received a number of awards including the David Sarnoff award,
(continued, next column)

IC and Systems Packaging, as a discipline, has been a stepchild in the electronics landscape within the US for decades. This has led the US to concentrate on ICs and systems in design and, in some special cases, fabrication and assembly. Tasks falling under the topic of "packaging" – which includes IC packaging, component fabrication, system-level boards and assembly – therefore became the focal point of Japan in the past, Taiwan and Korea in the more recent past, and China currently. .So, what is the future of this technology in the US and elsewhere?

Most industry experts foresee fundamental limits to IC integration limits for consumer and medical electronics. This has led industry and the electronics community to look for alternatives, both in the short and long run. In the short term, System-in-Package (SIP) and System-on-Package (SOP), which depend on co-developing the "package", seem to offer potential solutions to the above challenges, thus changing the technology landscape from its current stepchild mentality regarding "packaging". But US companies have gotten used to not investing in packaging and instead depending on the Far East. So, what is changing, if anything?

The so–called packaging field is almost as big as the IC field, in total market size. Yet, most universities think of this subject as manufacturing and assembly, without any basis in science. The above SIP and SOP technologies are fundamental and science–based, able to address combining the functions of RF, digital, optical, MEMS, sensors, fluidics, nano and bio in a synergistic fashion. Given this new perspective, the speaker addresses who will educate the new breed of engineers necessary to keep the industry competitive.

the sustained technical achievement award from IEEE CPMT Society, the John Wagnon award from ISHM, the Materials Engineering achievement award from ASM-Intl, the distinguished alumni award from the University of Illinois, and the Arthur Friedberg Memorial award from the American Ceramic Society.

Dr. Tummala's current research interests include packaging materials (metals, ceramics, and polymers) and processes, mechanical properties of materials, thermal and electrical designs, and integrated passive components.

SATURDAY MAY 7

One-Day Conference:
New Frontiers in Computing Technology - 2005

Sensor Networks –
The New Environment

Time: 9:00 AM - 4:15 PM
Place: Braun Auditorium, Stanford University
            (free parking)
Cost: $50 Member, $60 non-Member,
            $25 student/unemployed (more, after 4/20)
Registration: on the NATEA website or contact Belle
            Tseng, belle@sv.nec-labs.com
Web: www.natea.org/NFIC/

Morning Program (tentative)
8:00-9:00: Registration

9:00-9:15: Opening Remarks
Michael Graebner, IEEE CS Chapter Vice-Chair

9:15-10:00: Keynote: **Sensor Network Overview**
Professor Leonidas Guibas, Stanford University

10:00-10:45: **An Application and Technology**
Framework for Wireless Sensor Networks
John Suh, PhD, Crossbow Technology

11:00-11:45: **Wireless Networking**
Professor Prasant Mohapatra, UC – Davis

11:45-1:00: Lunch Break

Afternoon Program (tentative)
1:00-1:45: **Afternoon Keynote**
Professor C. K. Lee, National Taiwan University

1:45-2:30: **Distributed Algorithms**
Dr. Gary Bradski, Intel Corporate Technology

2:45-3:30: **System Design including Transceivers,**
Transmitters and Receivers
Chipcon

3:30-4:15: **Applications of Sensor Networks**
Professor Khan, Taiwan

4:15: Program Closing

In each of the last six years, the Santa Clara Valley Chapter of the IEEE Computer Society and the North America Taiwanese Engineers' Association (NATEA) have jointly brought to the Bay Area engineering communities the "**New Frontiers in Computing Technology**" Conference. This year, we bring to you the 7th Annual Conference focusing on the emerging Sensor Networks technologies.

Sensor Networks move computing from being a distinct entity within an environment to being a seamless part of the environment. This profound change touches both computing and the way we operate in daily life. Sensor Networks and the technologies they represent are fast becoming a new reality.

Starting with the hardware, this conference will cover such vital issues as wireless networking, distributed algorithms and applications at the engineering level. The aim of this conference offering is to provide members of the engineering communities with enough basic information to be able to make decisions regarding sensor networks and their applicability in new and emerging technical environments.

Registration Fees (Online or Mail):

	Before 4/30/2005*	After 4/30/2005 or On-site
IEEE, SNF, or NATEA Members	$50	$60
Non-Members	$60	$70
Students/Unemployed Members	$25	$30

All prices include meals.
*Payment must be received by 4/30/2005 via mail (check) or online (Paypal)

TUESDAY MAY 10

Terahertz Radiation via IC Technology

Speaker: Dr. Yasser A. Hussein, SLAC
Time: 6:00 PM (Pizza and soda, free),
               6:30 PM Presentation
Place: Cogswell College, (Boardroom),
               1175 Bordeaux Dr, Sunnyvale
Cost: none
RSVP: not required
Web: ewh.ieee.org/r6/scv/aps/

Yasser A. Hussein (M'03) received the Ph.D. degree in Electrical Engineering from Arizona State University, Tempe, AZ, USA in 2003, and the B.S. and M.S. degrees, both in Electrical Engineering, from Cairo University, Cairo, Egypt, in 1995 and 1998. He is currently a Post-Doctoral Research Faculty at Stanford Linear Accelerator Center (SLAC)-Stanford University. His current research interests include high-frequency computer-aided-design (CAD) of micro/nano devices, electromagnetics, microwaves, computational electromagnetics, semiconductor device simulations, and wave-device interactions.

Dr. Hussein is a Member of IEEE, an elected Member of Commission D of the United States National Committee of The International Union of Radio Science (USNC-URSI), and a nominated member for Sigma Xi. He has around 30 publications including a recent book chapter on CAD development for microwave and millimeter-wave applications (Kluwer Academic Publishers). He serves as a technical reviewer for several journals.

The terahertz (THz) region in the EM-spectrum is not yet fully explored. This region extends from 330 GHz (WR-3 waveguide) up to 30 THz (CO_2 lasers). It is estimated that about 98% of the radiation ever-produced in the universe since the Big Bang lies in this region. We will present efficient alternatives for generating THz radiation using on-chip IC technology, as opposed to free-electron-lasers (FELs) that are bulky, expensive, inefficient, and need high-power to operate. In this talk, a review of THz region and applications will be provided. Different excitation mechanisms will be discussed (electronically and optically). Finally, simulation results of S-parameters and radiation efficiencies and patterns of a fabricated on-chip micro-structure will be presented. The simulation results are based on a hybrid FDTD approach and are validated through comparison with Ansoft high-frequency structure simulator (HFSS).

TUESDAY MAY 10

Nanoelectronics: Now or Never?

Speaker: Dr. Mark Lundstrom, Purdue University
Time: 6:00 PM (Pizza and soda, free),
6:15 PM Presentation
Place: National Semiconductor Corp. Building 31
Large Auditorium, 955 Kifer Road,
Sunnyvale
Cost: none
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/eds/
announcements/ieee-scv-eds-
20050501.html

MARK LUNDSTROM is the Don and Carol Scifres Distinguished Professor of Electrical and Computer Engineering at Purdue University where his teaching and research center on the physics, technology, and simulation of electronic devices. Lundstrom is the founding director of the NSF-funded Network for Computational Nanotechnology, which has a mission of research, education, leadership, and service to the nation's National Nanotechnology Initiative. He serves on the leadership councils of the NASA-funded Institute for Nanoelectronics and Computing and the MARCO Focus Center for Materials, Structures, and Devices. Lundstrom's work has been recognized by several awards, most recently, in 2005, from the Semiconductor Industry Association in recognition of his career contributions to the semiconductor industry.

After forty years of progress in integrated circuit technology, microelectronics is undergoing a transformation to nanoelectronics. Modern MOSFETs have channel lengths of only 50 nm, and billion transistor logic chips have arrived. At the same time, there are new advances in carbon nanotube electronics, semiconductor nanowires, molecular electronics and spintronics. The traditional approach has already delivered silicon MOSFETs with channel lengths of ~5nm, but scaling down device dimensions with commensurate increase in device and system performance, is increasingly challenging. New techniques have demonstrated molecular switches, nanotube and nanowire FET's, NDR and single electron devices, and ultra-dense memory prototypes. Where is silicon technology heading? How long will the evolutionary approaches that have been so successful continue to fuel progress? What role will new ideas from nanotechnology play in the electronic device technology? Is nanoelectronics the new frontier of electronic device technology? These are questions that I will try to address.

This talk will begin with a discussion of the fundamental limits of transistors that operate by modulating the flow of charge. I'll then describe a very general and very simple way to understand nanoscale transistors. Using this approach, I'll examine the possibility of 10nm-scale silicon MOSFETs and what new channel materials, such as III-V semiconductors might provide. Next, I'll discuss one-dimensional transistors made from nanotubes and nanowires and then take a brief look at molecular transistors. The talk will conclude with some speculations about where electronic device research is heading.

WEDNESDAY May 11

Shielding Packaging for High-Cost Electronics

Speaker: Dr. Fabrizio Montauti, Vice President of Engineering, WaveZero

Time: Seated dinner served at 6:30 PM ($25 if reserved before May 8; $30 after & at door); free presentation at 7:30 PM

Place: Ramada Inn, 1217 Wildwood Ave (Fwy 101 frontage road, between Lawrence Expy and Great America Pkwy), Sunnyvale

RSVP: Please reserve and pay in advance using our PayPal on-line system or email Janis Karklins

Web: www.cpmt.org/scv/

RF and EMI shielding is usually the ignored part of the design, applied as a band-aid to products and packages after many aspects of the design are completed. It should be designed in up-front to provide the most advantageous designs (smaller, lighter, tighter), facilitate products passing regulatory tests, and get to market faster. This talk will discuss a number of innovative shielding solutions and specific case studies. We will contrast older methods of shielding (metal cans and conductive paint on plastic) with a new EMI shielding material based on the thin film metallization of thermoformed structure.

Dr. Fabrizio Montauti has extensive senior level experience with microwave and millimeter wave wireless equipment and network design. Prior to joining WaveZero, he was VP of Marketing & Sales and VP Operations for PointRed Technologies (San Jose, CA). He was responsible for market development for a wireless communication system and was instrumental in securing key sales contracts around the world. From 1999 to 2001, he was co-Founder, Executive VP and COO for EESA (San Jose, CA), a provider of high frequency synthesizers in the 2.4 GHz and 5.7 GHz frequency ranges. From 1996 to 1999, he was Director of Engineering for P-Com, Inc. (Campbell, CA), a public company focused on wireless equipment and networks. He managed a team of 40 engineers working on new wireless equipment and devices. For Siemens Telecommunications, from 1989 to 1995, Dr. Montauti, worked as a Senior Designer on microwave and millimeter wave modules for satellite communications. He received his Doctor of Electronic Engineering at the Universita' degli Studi di Pisa (Italy) in 1989. He has three patents in the field of wireless equipment design and has published journal quality papers at international conferences. WaveZero spoke at the IEEE's Oakland East Bay (OEB) Chapter of the Communications Society in February (See page 20 of the GRID).

WEDNESDAY MAY 11

IEEE 802.11 Wireless LAN Architecture: New Protocols and New Deployment Strategies

Speaker: Matthew Gast, Director, Consulting Engineering, Trapeze Networks
Time: 6:00 PM (pizza & soda), 6:30 PM presentation
Place: National Semiconductor Credit Union, Bldg. 31, 955 Kifer Rd., Sunnyvale
Cost: $1 donation for pizza
RSVP: by email to rsvp@comsocscv.org
Web: www.comsocscv.org/

Matthew Gast is the Director of Consulting Engineering at Trapeze and the author of "802.11 Wireless Networks: The Definitive Guide" (O'Reilly, 2002; second edition expected May 2005). At Trapeze, he helps leading organizations understand and deploy scalable, standards-based wireless LANs. Prior to Trapeze, Matthew held a series of engineering positions in at a variety of network security companies. He is a regular participant and instructor at the Interop Labs (iLabs), where he works with other leading engineers to understand cutting-edge network protcols. Matthew contributed to the National Institute of Standards and Technology (NIST) recommendations on wireless LAN security developed by the U.S. government, and has served on the technical advisory boards of several start-up companies.

Strong user demand for wireless networking poses challenges for designers. Standards bodies must increase the capacity of the network protocols to meet user demand for ever-higher data rates. Even after the speed boosts from IEEE 802.11a and 802.11g, user demand has been barely satiated. 802.11 Task Group N has taken on the challenge of increasing network speeds once again. Bringing products to market, however, is only the beginning. Network architects need to build networks that satisfy user demands. At many institutions, the demand is for ubiquitous network access, even when boundaries of administrative control make it impossible to do so. In response, many distributed networks are being built as "federations," based on IEEE 802.1X and related protocols.

THURSDAY MAY 12

Technologies for Overcoming Interconnect Parasitics and Reducing Costs in the 10 to 100 GHz Range

Speaker: Dr. Ed Stoneham, Endwave Corp.
Time: 6:00pm - Refreshments and social time;
6:45pm - Technical Presentation
Place: Agilent Technologies, Santa Cruz conference room, Bldg 50, 5301 Stevens Creek Blvd, Santa Clara
Cost: none
RSVP: not required
Web: www.mtt-scv.org/

Circuit interconnects are a major contributor to unit-to-unit variability at frequencies above 10 GHz. The variability of conventional bond-wire interconnects will be quantified, and two technologies that increase first-pass yields and reduce costs will be described. Bond-wire effects are completely eliminated from RF circuitry through the use of MLMS™ flip-chip integration technology, which also achieves a 30% cost improvement with respect to MMIC technology through a dramatic reduction in semiconductor content. Waveguide, IF, and baseband interconnections are eliminated by Epsilon™ chip-on-board technology, which achieves an additional 30% cost improvement through elimination of machined metal parts and connectors. Further cost reductions result from high first-pass (untweaked) yields and improved performance margin. The new technologies also result in considerable reductions in size and weight.

Ed Stoneham, a native of California, graduated from U. C. Berkeley with an A. B. in Physics and from Stanford with a Ph. D. in Applied Physics. His doctoral work under Jim Gibbons dealt with the co-implantation of ions into $GaAs_xP_{1-x}$ light emitting material. During thirteen years at Hewlett Packard he developed the company's first one-micron silicon transistor, three generations of reactive ion etching and plasma processing capabilities, and the first production ion-implanted GaAs FET process. From 1984 through 1989 at Microwave Technology Inc. Dr. Stoneham established the production processes for highly linear and rugged 0.3-micron GaAs FETs and for alumina thin-film circuits. From 1989 through 1993 he managed the MMIC foundry interface and MMIC packaging effort at Pacific Monolithics. For the last twelve years Dr. Stoneham, as Advanced Technology Director at Endwave Corporation, has been designing millimeter-wave ICs and interconnects, and developing flip-chip and packaging technologies.

Dr. Stoneham is a member of Phi Beta Kappa and Sigma Xi and a Senior Member of IEEE. He is an author of more than twelve U. S. patents and thirty publications.

TUESDAY MAY 17

Dynamics in Magnetic Micro- and Nanostructures

Speaker: Prof. Burkard Hillebrands, IEEE Magnetics Society Distinguished Lecturer, 2005, Tech. Univ. Kaiserslautern, Germany

Time: 7:30 PM - Refreshments and social time; 8:00 PM - Technical Presentation

Place: Komag, 1710 Automation Parkway, San Jose

Cost: none

RSVP: not required

Web: www.e-grid.net/docs/0505-scv-mag.pdf

Burkard Hillebrands received the diploma and Ph.D. degrees in physics from the University of Cologne, Cologne, Germany, in 1982 and 1986, respectively. After a postdoctoral stay at the Optical Sciences Center, Tucson, AZ, he received the habilitation from the RWTH Aachen, Aachen, Germany, in 1993.   He was an Associate Professor at the University of Karlsruhe, Karlsruhe, Germany, in 1994. Since 1995, he has been a Full Professor at the University of Kaiserslautern, Kaiserslautern, Germany. He is the coordinator of the German priority program "Ultrafast Magnetization Processes," the vice coordinator of the German research unit "New Materials with High Spin Polarization," and he coordinates a European network on "Ultrafast Magnetization Processes in Advanced Devices." He is currently the head of the Material Research Center for Micro- and Nanostructures (MINAS) at the University of Kaiserslautern. He is a member of the granting board for collaborative research centers (SFB) of the senate of the Deutsche Forschungsgemeinschaft and a member of the Editorial Board of the Journal of Physics D: Applied Physics.   His   research   field   is   mostly   in magnetoelectronics. His special interests are in spin dynamics, material properties of thin magnetic films and multilayers, exchange bias, as well as in elastic properties of layered structures. In the field of spin dynamics, he is particularly interested in dynamic magnetic excitations in confined magnetic structures, magnetic   switching,   and   nonlinear   magnetic phenomena using space- and time-resolved Brillouin light scattering spectroscopy and time-resolved Kerr

For applications in sensors and in data storage, the dynamic properties of micro- and nanostructures gain   increasing   attention.   The   fundamental excitations in these objects are confined spin waves, and it is useful in particular to understand their properties in view of the noise spectrum in sensor and MRAM applications.

This   lecture   addresses   the   dynamics   in homogeneously and inhomogeneously magnetized objects, starting with an introduction into spin waves and   the   effects   of   finite   dimensions.   In inhomogeneous systems the excitation spectrum is complex, and new phenomena like localization and tunneling of modes are discussed. The key points are illustrated by results obtained by a space- and time-resolved   Brillouin-light-scattering   technique, which   allows   one   to   follow   experimentally   the propagation of spin wave packets and to present the results in an animated format.   To conclude the lecture, the analysis of ultra-high-frequency dynamic properties (2-100 GHz) of small magnetic elements with spatial resolution in the 300-nanometer range is presented.

effect techniques. He has   published   more than 170 articles, has five   patents   and patent   applications, seven   book contributions, and he is   co-editor   of   the Springer-Verlag   book series   on   "Spin Dynamics in Confined Magnetic Structures."

WEDNESDAY MAY 18

Samplify: Lossless and Lossy Data Compression for Instrumentation Signals at 10+ Msamp/sec

Speaker: Al Wegene, founder, Samplify Systems LLC
Time: Check-In/Networking: 6:30 PM,
               Presentation: 7:00 PM
Place: Cogswell College, Room 197,
               1175 Bordeaux Drive, Sunnyvale
RSVP: to David Rivkin by May 13 at
               david.rivkin@ieee.org
Web: www.ewh.ieee.org/r6/scv/ims

SignalZIP and Samplify offer user-selected compression ratios up to 4:1 at sampling rates up to 100 Msamp/sec. This presentation will also demonstrate how common instrumentation measurements, such as rise time, jitter, spectral analysis, etc., can be improved through the use of Samplify compression.

Al Wegener is a DSP engineer with more than 20 years' experience in defense electronics, professional and consumer audio, and wireless applications. Mr. Wegener founded Samplify Systems LLC in 1999 to bring the benefits of high-speed lossless and lossy compression to those users processing signals at sampling rates above 10 Msamp/sec, where no effective compression solutions had been offered.

WEDNESDAY MAY 18

Architecture and Application of Wireless Communication In Glucose Monitoring for People with Diabetes

Speaker: Charles Nelson, Director of Engineering, Abbott Diabetes Care

Time: optional dinner with the speaker in the Stanford Hospital cafeteria at 6:15 PM; Presentation at 7:30 PM

Place: presentation at Clark Center Auditorium (see website for maps)

Cost: none; campus parking free after 4 PM

RSVP: not required

Web: ieee.org/scv/embs/pages/upcoming.html

Diabetes mellitus, a disease in which the pancreas fails to produce insulin or cells fail to respond to insulin for cellular metabolism of glucose, is a world-wide public health problem in terms of loss of quality of life and corresponding cost of care.

There are over 140 million people with diabetes worldwide, including 18-20 million in the USA. This number is increasing and expected to double by 2030. Approximately 12-14 million diabetics are classified as noninsulin dependent, or Type II, diabetics who can control their glucose levels by changes in life style by the use of medication or by the infrequent use of insulin. For approximately 1-3 million diabetics classified as Type I diabetics, injections of insulin are needed to maintain glucose levels. Data from the Diabetes Control and Complications Trial (DCCT), reported in 1993, show that the quality of life may significantly be improved for people with diabetes if good control of blood sugar (glucose) levels is maintained. Thus, there is a need for frequent and accurate self-testing of glucose.

Diabetes has both chronic and acute morbidity associated with this disease. Chronically elevated blood sugar levels are know to cause blindness, neuropathy, vein necrosis of the extremities, kidney failure, and contribute to heart disease. Acute cases of hypoglycemia, low blood sugar, can cause death. American Diabetes Association estimated in 1997 that the combined health care costs of diabetes management and the co-morbidities related to diabetes in the United States was $98 billion annually.

In 1997, the ADA estimated that a person with diabetes spent $10,071 on health care vs. 2669 for a person without diabetes. These costs are growing 10 to 15% annually in developed nations. Therefore, the combined global estimates for the cost of this disease to society is $200 to $350 billion in 2004.

At Abbott Diabetes Care, formally Therasense, our mission is to improve the quality of lives for our customers through technologically advanced and high quality products. As part of our initiative in diabetes disease management, design and commercialization of cost effective electromechanical solutions is paramount to improve the lives of our customers.

Two Abbott Diabetes Care solution exist that employ wireless data transfer from biosensors to the information technology (IT) infrastructure. One, of these solutions is for discrete glucose whereas the other is for continuous glucose. The discrete glucose meter acts as a pico server and takes the data generated by a blood glucose measurement and send it to another device in the personal area network (PAN) of the user. The continuous glucose meter employs two wireless linkages. The first from the biosensor to the pico server and the second from the pico server to the IT infrastructure.

Our discrete and continuous glucose monitors utilize complicated but elegant application of structured C+ state machines and microprocessors. Our most advanced product, Navigator, employs a novel CPU architecture that improves the function, flexibility, and time to market. One part of the architecture is communication. We have begun to broadly utilize the 802.15 standard and BlueTooth protocol as a cable replacement and PAN linkage.

The novel CPU architecture affords specialization in the function of each module around the most intensive tasks. By breaking the architecture into discrete function based modules, the most appropriate microprocessor, speed, power consumption, and interfaces may be designed. In our design the functions are broken along the lines of duty cycle and job functions. The first module retrieves all of the data and performs the data reduction. The second module manages the user interface. The third module manages the communication link. All of the modules communicate through an internal bus.

The communication to the IT infrastructure utilizes the BlueTooth protocol and commercially available ARM7 based modules. BlueTooth has received broad

acceptance in the consumer electronics space for personal information management, audio data transfer (files and streaming music), device interoperability (phone to computer user interface for dial up), and data transfer. BlueTooth provides the ideal linkage for diabetes management within the personal area network. It is robust, secure, and standard. This allows communication into the burgeoning PAN and machine interactions of the user. The BlueTooth link has been approved by FDA and is a recognized standard, certified protocol globally.

As we look into the future, our bodies will reach new levels of longevity through the application of today's technologies. At Abbott Diabetes Care, we are realizing a small subset of these technologies with future implications for disease management. Evolution of biosensors and their connectivity to our personal area networks and machine interfaces will provide real time and essential feedback on our state of health. Armed with this information, debilitating co-morbidities associated with diabetes will be substantially reduced. Acute morbidity related to diabetes can be reduced or eliminated through user intervention in the response to continuous health status data. As technologist, we have the great opportunity to help the people of society that have no choice, people with debilitating diseases such as diabetes.

Mr. Charles L. Nelson is currently the Director of Engineering for Abbott Diabetes Care, a Division of Abbott Laboratories. Charles has over 20 years of experience commercializing medical technology in the areas of diagnostics, orthopedics, and cardiovascular products. Charles graduated from Purdue University with a Bachelor of Science in Chemical Engineering and holds a Master of Science degree from Northwestern University. Charles is inventor or co-inventor on over 11 issued patents and several pending applications. The engineering team at Therasense launched the Freestyle Flash glucose meter in 2003. This product grew to over $100 million in sales in 2004. Recently, the first commercial design for Navigator, the continuous glucose monitor, was completed.

Analog Circuit Design with Submicron Transistors

Speaker: Prof. Bernhard E. Boser, University of California, Berkeley
Time: Refreshments at 6:30 PM; Presentation at 7:00 PM
Place: Cadence Building 5, 2655 Seely Ave, San Jose
Cost: Donation requested for Refreshments
RSVP: Call 408 894-2646 (leave a message) or by email to ssc_scv_rsvp@yahoogroups.com
Web: www.ewh.ieee.org/r6/scv/ssc

Prof. Bernhard E. Boser received the Diploma in Electrical Engineering from the Swiss Federal Institute of Technology in 1984 and the MS and Ph.D. from Stanford University in 1985 and 1988. From 1988 he was a Member of Technical Staff in the Adaptive Systems Department at AT&T Bell Laboratories. In 1992 he joined the faculty in the Department of Electrical Engineering and Computer Sciences at the University of California, Berkeley where he also serves as a Director of the Berkeley Sensor & Actuator Center. Dr. Boser's research is in the area of analog and mixed signal circuits, with special emphasis on analog-digital interface circuits and micromechanical sensors and actuators. He has served on the program committees of the International Solid-State Circuits Conference, the Transducers Conference, the VLSI Symposium, the Sensor and Actuator Workshop, and was the Editor of the IEEE Journal of Solid-State Circuits. Dr. Boser is a Fellow of the IEEE. Presently he is on leave from the University at SiTime, a startup company he co-founded in 2004.

Most textbooks and courses teach analog circuit analysis (and design) using the so-called "square-law model" for MOS transistors. While simple and intuitive, the behavior of modern thin-gate and short-channel transistors deviates significantly from this simple description. More accurate models are available and used extensively in simulators but are mathematically to complex for design. The resulting significant deviation of designed performance from that predicted by simulation is often overcome with iterative simulation and "tweaking" design parameters. While this approach can work, it is cumbersome, time consuming, and does not easily lead to an overall optimized design. We present a design methodology for analog circuits that is simple and intuitive, yet accurate even for very deep sub-micron transistors. Rather than focusing on geometry, the technique concentrates on key analog circuit performance metrics including speed, power dissipation, noise, and their tradeoffs. First, these metrics are determined based on overall specifications. Bias currents and device sizes are obtained in a final and straightforward step.

THURSDAY MAY 19

Network Visibility @ Wire-Speed for Visibility, Security and Capacity Planning

Speaker: Gopala Tumuluri, Foundry Networks
Time: Pizza at 6:30 PM; Presentation at 7:00 PM
Place: Bishop Ranch 1, 6101 Bollinger Canyon Rd, San Ramon (just off I-680)
Cost: none
RSVP: Please send a quick note to oeb@ comsoc.org to allow us to order the correct number of pizzas, no later than May 18
Web: www.comsoc.org/oeb/

Gopala Tumuluri is the Product Line Manager for Multi-Layer Switching at Foundry Networks. Mr. Tumuluri has extensive experience in multi-layer networking solutions for Enterprise and Service Provider customers. Prior to joining Foundry, he held Product Management and Engineering positions at Elematics, Calient Networks and FORE Systems. Mr. Tumuluri graduated with an MBA from Carnegie Mellon University, and an MS degree in Computer Science from the University of Kentucky.

In the age where networks are ever more vulnerable to security threats, intrusions, attacks and malicious activity, it is unimaginable to manage the network blindly. The need for always-on visibility into the network has never been greater. It is the dream of any network manager to have visibility to the network traffic at every point in the network all the time with zero impact to network performance. Traditional technologies for network monitoring are prohibitively expensive to deploy widely throughout the network, and also choke network performance when enabled. The problem worsens as networks grow in size, speed, and capacity, and as security vulnerabilities increase. Network managers have suffered long by sacrificing network visibility and security in favor of capital cost and performance.

sFlow is a modern standards-based network monitoring and export protocol (RFC 3176) that addresses many of the challenges that network managers have long faced. sFlow technology offers visibility into the network on every port and at every bandwidth speed. By embedding sFlow technology into network router and switch ASICs, sFlow becomes an "always-on" technology that operates at wire speed performance, no matter what protocol or port bandwidth capacity. Cost of implementation is driven down dramatically when compared to traditional network monitoring solutions using mirrored ports, probes, and line tap technologies. A full enterprise-wide monitoring capability for every port in the corporate network is now possible using sFlow.

This talk presents the challenges of current network monitoring technologies, an overview of sFlow technology and its use, and the key benefits of using sFlow for network monitoring, visibility and security.

We will continue our feature at the meeting of providing some networking time for those that want to stand and make a brief announcement. If you're looking for a new position, have a position to fill, want to let us know that your new start-up is ready for business or have a similar announcement, bring your resumes, job descriptions or company brochures and be prepared to make a match. Please keep your statements brief, so we'll have time for everyone. There will be time before and after the formal meeting for one-on-one discussions.

THURSDAY MAY 19

Arc Flash Hazard Assessment and Electrical Safety in the Workplace

Speaker: Anthony Mazy, Consulting Engineer
Time: No-host social at 5:30 PM; Presentation at 6:15 PM; Dinner at 7:15 PM; Presentation continues at 8:00 PM
Place: Marie Callender's Restaurant - The Garden Room; 2090 Diamond Blvd, Concord (near Concord Hilton Hotel)
Cost: $22 for IEEE members; $25 for non-members
RSVP: Please send a quick note to Gregg Boltz at gboltz@brwncald.com or call (925) 210-2571 by May 18
Web: www.ewh.ieee.org/r6/oeb/ias.html

Anthony Mazy received his BSEEE from California State University, Sacramento, in 1977. He has been an energy analyst with a national consulting firm, a project engineer at several military installations including Base Utilities Engineer at Mather and McClellan AFBs, in Sacramento, and a design engineer in projects as diverse as remodeling of the Bonaventure Hotel in Los Angeles, the B-2 (strategic bomber) consolidated flight test facility at Edwards AFB, and the 54,000 Sq. ft. private residence of Aaron Spelling. Most recently a forensic engineer with the California Public Utilities Commission, Mr. Mazy is a recognized expert in Advanced Meter-Reading systems and the utility interconnection of Distributed Generation.

Mr. Mazy is a registered Professional Engineer, in California. He consults privately, with a small group of electrical engineers, who have performed a number of Arc Flash Hazard Assessments in recent months, and regularly participates in IEEE activities, particularly the Industry Applications and Power Engineering societies. In October, Mr. Mazy will be the moderator for two panel discussions on "Rethinking T&D Architecture for DER" at the IEEE-PES T&D Conference and Exhibition in New Orleans.

An arc flash hazard evaluation should be performed prior to working on any energized electrical equipment. Various manual calculation methods as well as computer program packages can be used for this task. Results from such analyses will help determine the appropriate level of personal protective equipment required to be worn. In addition to these topics, the talk will also cover the following relative to arc flash hazards:
* OSHA Requirements and What Has Changed
* Regulatory History and the NFPA 70E
* Applicable Situations
* Protective Measures
* Calculating Incident Energy
* Methodology of Hazard Assessment
* IEEE Calculations
* IEEE Standard 1584 -2002
* Short Circuit & Coodination Studies are needed
* Engineering Aids -- Tables, Spreadsheets, Simulation Software
:

TUESDAY MAY 24

Why Advertising Doesn't Work for Consultants

Speaker: Linda J. Popky, President, L2M Associates
Time: 7:00 PM Informal Networking;
7:30 PM Meeting
Place: Ramada Inn, 1217 Wildwood Ave (101 at Lawrence), Sunnyvale
Cost: none
RSVP: not needed
Web: www.ieee-sv-consult.org/notices.htm

Wondering whether or not adding advertising to your marketing budget will expand your business? Not sure whether you should spring for the extra dollars to create and place ads for your consulting business? Wondering whether there's a better way?

Linda Popky, President of L2M Associates, Inc. will share insights into why many consultants don't see results from traditional advertising programs. She'll review what advertising can and can't do for consultants, and discuss the three key marketing and promotional programs no consultant should be without — even if they never spend a dollar on advertising.

Linda J. Popky is a senior marketing professional with over 20 years of proven performance in the technology and B2B marketing space, including extensive experience with Sun Microsystems, most recently as director of marketing within the Software Division. Her expertise includes corporate marketing/communications and messaging, marketing team development, facilitation, sales training and support, channel/field marketing, marketing operations, industry /market development and product marketing. She has architected leading edge customer loyalty and retention programs with a focus on improved business efficiency, customer advocacy and quality, and has a reputation for strong leadership and team management, as well as strategic program development and delivery skills.

Linda served as a charter member of the Conference Board Council on Customer Strategy, and was a member of the Council on E-Business Strategy. She has an MBA and a BS in Communications from Boston University. Her work with business process improvement includes a study mission to Japan on Employee/Customer Loyalty.

A member of Women in Consulting (WIC), Linda is involved with the WIC Program Committee and Silent Auction. She is also a member of the Northern California chapter of the Institute of Management Consultants, IMC, and is available for speaking engagements through the IMC Northern California Business Speakers Bureau. Linda is currently serving on the planning committee for Consultants' Confab, the premier conference by consultants for consultants. She is also a member of the Society for the Advancement of Consulting (SAC) and the Alliance for Technology and Women (ATW).

WEDNESDAY JUNE 8

Reliability Issues in Lead-Free Soldering

Speaker: Dr. Dongkai Shangguan, Director – Advanced Process Technology, Flextronics

Time: Seated dinner served at 6:30 PM ($25 if reserved before June 5; $30 after & at door); free presentation at 7:30 PM

Place: Ramada Inn, 1217 Wildwood Ave (Fwy 101 frontage road, between Lawrence Expy and Great America Pkwy), Sunnyvale

RSVP: Please reserve and pay in advance using our PayPal on-line system or email Janis Karklins, Karklins@ieee.org

Web: www.cpmt.org/scv/

Dr. Donkai Shangguan received his BS degree in Mechanical Engineering from Tsinghua University, China, Ph.D. degree in Materials from the University of Oxford, U.K., and MBA degree from San Jose State University. He conducted post-doctoral teaching and research at the University of Cambridge and then at the University of Alabama, and lectured at Wayne State University as Adjunct Faculty.

Dongkai worked for 10 years at Ford Motor Co. / Visteon Corporation as Senior Technical Specialist, Supervisor of Advanced Electronics Manufacturing, and Manager of Supplier Quality, before he joined Flextronics International in 2001 where he is currently Director for Advanced Process Technology with the Corporate Technology Group.

Dongkai has published one book and over 150 papers (including many journal publications and several book chapters), has given numerous technical presentations and keynotes, and his latest book on lead-free solder interconnect reliability will be published soon. He has 20 U.S. and international patents issued and a number of U.S. and international patents pending. He is currently a regular columnist for the "Global SMT & Packaging" magazine.

Dongkai is a senior member of IEEE and SME, and actively participates in professional organizations and consortia, and has chaired technical sessions and panels at numerous conferences. He has received a number of recognitions for his contributions to industry, including the "Total Excellence in Electronics Manufacturing Award" from the Society of Manufacturing Engineers (SME), and the "Soldertec Lead-Free Soldering Award".

While a significant volume of work has been conducted in the past ten years by the industry on manufacturing issues to enable the gradual conversion to lead-free solders, reliability studies of lead-free solder interconnects are still emerging. The issue of reliability is complicated by the wide variety of application environments and requirements, which give rise to different loading conditions. The physics of failure, which is directly related to reliability, is a critical topic still under intense investigation for lead-free solders. The topic is further complicated by the fact that the relative reliability comparison between eutectic Sn-Pb solder and the lead-free solder alloys varies with the loading conditions. These complications create great difficulties for the development of appropriate acceleration testing profiles and for reliability prediction. This presentation will review the important reliability issues for lead-free solder interconnection systems, including the components, the PCB, and the solder joints, under different loading conditions (thermomechanical, dynamic mechanical, electrochemical, etc).

A Pendant-Geometry CT Scanner for Breast Cancer Detection: Design, Characterization and Initial Clinical Assessment

Speaker: John M. Boone, Ph.D., UC Davis
Time: optional dinner with the speaker in the Stanford Hospital cafeteria at 6:15 PM; Presentation at 7:30 PM
Place: presentation at Clark Center Auditorium (see website for maps)
Cost: none; campus parking free after 4 PM
RSVP: not required
Web: ieee.org/scv/embs/pages/upcoming.html

John M. Boone, Ph.D., received his undergraduate degree in medical physics from UC Berkeley, and graduate degrees in Radiological Sciences from UC Irvine. After faculty positions at the University of Missouri and Thomas Jefferson University (in Philadelphia), Dr. Boone joined the faculty at UC Davis in 1992. Dr. Boone is currently Professor and Vice Chairman of Radiology (for Research) and Professor of Biomedical Engineering at UC Davis. His is certified by the American Board of Radiology in Radiological Physics, is a fellow of the American Association of Physicists in Medicine and of the Society of Breast Imaging, and won an Outstanding Achievement Award in the Society for Photo-optical and Instrumentation Engineers. Dr. Boone's research interests include the development of a dedicated CT scanner for early breast cancer detection, Monte Carlo evaluation of image quality and radiation dose, and the development of mouse imaging technology combining x-ray and gamma-ray imaging.

The purpose of this investigation was to characterize the performance of a cone-beam CT scanner system custom designed for breast imaging. The breast CT scanner was designed and fabricated using an end-windowed industrial x-ray source and a 30 cm x 40 cm CSI thin-film transistor (TFT) flat-panel x-ray detector. The first prototype scanner (Albion) utilizes 360 acquisitions of 1,000 projection images (768 x 1024) over a 33 second acquisition. The 88 cm source to detector distance and the 48 cm source to isocenter distance allow breasts from 10 cm to 18 cm in diameter to be scanned, and the size-dependent technique factors were determined to allow scanning at the same average glandular dose levels as two-view mammography.

The spatial resolution was characterized using a thin tungsten wire, and the contrast resolution was evaluated using low contrast test objects. Scattered radiation levels were measured as a function of breast diameter, beam energy, and breast composition. The spatial resolution is characterized by a modulation transfer function with 10% modulation at approximately 1.2 inverse millimeters. Contrast resolution was found to be dependent upon breast diameter in the size of the test object in question. Scatter to primary ratio (SPR) at the center of the field of view were measured as 0.25, 0.50, and 0.92 for 50%/50% breast phantoms of 10 cm, 14 cm, and 18 cm in diameter, respectively.

While a number of artifacts proved difficult to remove, the image quality of the scanner based upon its technical performance and subjective analysis of cadaver breast images suggests that the Albion prototype is capable of good performance. A number of technical details in the design of the scanner will be discussed, including the x-ray tube assembly (bow-tie filter and x-ray shutter), rotating gantry system, etc. Validated Monte Carlo techniques were used to assess the average glandular dose of the breast, based upon inferred spectral measurements. Clinical evaluation of the breast CT scanner on volunteers and patients will begin shortly, with initial results should be available in March 2005.

CONFERENCE CALENDAR

The **CONFERENCE CALENDAR** is a service to our IEEE Members. It outlines upcoming IEEE workshops and conferences in the Bay Area. Please submit items to the GRID Editor: editor@e-grid.net.

Conferences are also encouraged to purchase display space in the **GRID.pdf** and publicize their events on our website and in our **e-GRID** email notification service. For the Conference Publicity flyer, please download:

www.e-grid.net/docs/conf-flyer.pdf

May 17-19**: The Vision Show & Conference West comes to San Jose**

North America's leading showcase of machine vision components, systems and solutions comes to San Jose. Held every other year in the heart of Silicon Valley, the Show is the perfect venue for suppliers and system integrators to meet with system designers and users to share information on new products and real-world solutions.

See Page 7 in this GRID

May 23-25**: Aeroacoustics Conference is in Monterey**

This international forum for scientists and engineers from industry, government, and universities allows the exchange of knowledge and results of current studies and discussion of directions for future research. Papers cover all aspects of the generation, propagation, measurement, modeling, and control of vehicle noise, as well as the effect of noise on structures and individuals.

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The 13th Stanford Networking Research Center/ Accel Symp.

May 25: **Next Generation Media Networks - The Future of Content Delivery**

This special Symposium will explore and highlight emerging business and technology trends and potential obstacles surrounding next-generation media networks. Questions include:
- What new types of content are emerging or possible?
- Will IP TV be the next wave or will cable carry the new services?
- What are the possibilities and challenges for mobile content and delivery?
- What are the protection, privacy and rights demands?
- What are the technical challenges for deploying home networks?
- Will power shift toward content owners?

$75 early-registration discount through May 11; more information and list of presenters at

snrc.stanford.edu/symposium.html

May 24-26**: Aircraft Noise and Emissions Reduction Symposium**

A high-level, multidisciplinary technical symposium bringing together leading engineers, scientists, researchers, government and civil aviation officials, industry, and policy makers to discuss the topics and issues of aircraft noise and emissions reduction.

See Page 5 in this GRID

May 24-27: **World Wireless Congress 2005: Converging the Broadband Wireless and Mobile**

WWC'05 is a conference focused on research, development and design of emerging wireless and mobile communications focusing on B3G and 4G technologies, with tutorials, sessions, and networking. It is held this year in Palo Alto.

WWC'05 extends a $100 Instant Rebate to IEEE members, for all registrations by April 15th. Please write rebate code "SF0415CAL" on the registration form.   For more information, see

www.b3g.org

June 21-23: **POFWorld '05 comes to the Santa Clara Convention Center**

Plastic Optical Fiber for Home and Auto
– sessions, tutorials, exposition.
- June 21: Tutorials   - June 22-23: Conference & Exhibits

The only trade show for Plastic Optical Fibers that covers all aspects of the business - technology, markets and applications. This year POFWord features 6 half-day tutorials:
- POF Markets and Applications
- Designing with POF
- Designing with POF for the Home
- Automotive and Consumer Applications
- Hands-on Connector Standards for Installers
- Optical Sources for POF Links

Early Registration fee before May 31st; 10% discount for any IEEE Member.

See **www.pofworld.com**