Chapter Meetings and Events

SCV-EMS - 9/29: before-dinner talk - **The Art of Commitment and The Science of Change** - after-dinner talk - **Walking A Tightrope with Resilient Packet Rings - A Startup Story** - developer insights... [more]

SCV-SSC - 9/29: **Trends in High-performance Computer Aided Design** - the revolution in electronic design tools ... [more]

SCV-Rel - 9/29: **Analyzing Reliability Data: Difference between Repairable Vs. Non-Repairable Systems** - when to use MTBF ... [more]

SCV-Education - 9/29: **Are we Ready for the "Nano World", Education-wise?** - impact on our education system ... [more]

SCV-PACE - 9/30: **Career Defense in the Face of Globalization** - the growth in the movement of information technology work offshore... [more]

SF-PACE – 10/2: **Career Defense in the Face of Globalization** - the growth in the movement of information technology work offshore... [more]

SCV-LEOS - 10/5: **Photonics CMOS Compatibility using Molecularly Engineered Materials** - on-chip integration of photonics ... [more]

SCV-CSS – 10/7: **Shortcuts to Step Motor Selection** - step motor behavior; eliminating the trial and error in motor selection ... [more]

SCV-SP – 10/11: **Converting MATLAB Algorithms to FPGA or ASIC Designs** - a new methodology is needed ... [more]

SCV-EDS – 10/12: **Myths and Truths about High-K/Metal Gate Stack Technology** - studies on instability of high-k devices ... [more]

SCV-Comm – 10/13: **Digital Rights Management for Mobile Content** - a network of trusted devices gives consumers content portability ... [more]

SCV-CPMT – 10/13: **A Novel X-ray Microtomography System for Non-Destructive Imaging of Advanced Packages"** and **"uCT Techniques In Combined 2D/3D High Resolution X-ray Systems** - two approaches to 3-D X-ray inspection for failure analysis ... [more]

SCV-MTT – 10/14: **The Design of WCDMA Zero-IF Receivers: System and Circuit Issues** - integration of the radio on-chip ... [more]

SCV-CNSV – 10/19: **What an Engineer Needs to Know about Business** - the gap in understanding between engng and business ... [more]

SCV-Mag – 10/19: **Is the Next Geomagnetic Reversal Imminent?** - the Earth's field has been decreasing for the past 2,000 years … [more]

SCV-PES&IAS – 10/20: **Technical Issues and Practical Applications of Transient Voltage Surge Suppression (TVSS)** - electrical surge suppression for prevention of production and data loss ... [more]

SCV-EMB – 10/20: **Cochlear Implants for Profound Hearing Loss - Signal Processing Considerations** - signal processing in cochlear implants and impact on sound quality... [more]

SCV-SSC – 10/21: **Power-Performance Optimization Methods for Digital Circuits** - in deep submicron technologies, avoiding prohibitive power consumption ... [more]

SF-IAS – 10/26: **Overview of IEEE Standard 1100-1999 - Recommended Practice for Powering and Grounding Electronic Equipment** - how it is organized, with highlights from chapters; it is now in the balloting process... [more]

SCV-WIE – 10/27: **How to Balance Career Goals and Time for a Family** - insights from successful women engineers on how to maintain skills & not sacrifice the opportunity for a family ... [more]

SCV-Rel – 10/27: **Reliability Horror Stories** - Halloween's truly ghoulish reliability horror stories from speaker & audience ... [more]

SCV-EMS – 10/27: **Startups that Survived the Bust: The Silicon Valley Spirit**- What was unique about survivors of the dot-com bust that allowed them to rise from the ashes … [more]

SCV-CPMT – 10/28: **The Nanotechnology Frontier: Applications of Nano to Materials and Packaging** - the engagement between the Engineer and Nanotechnology ... [more]

Upcoming Conferences in the Bay Area

Sept 30 – Oct 2: Stanford Univ

Engineers for a Sustainable World National Conference -- Solutions for a Shrinking Planet: Sustainable Engineering and Enterprise for Human Development - technologies and social/cultural concerns, environmental issues. **[more]**

Oct 4-7: Santa Clara Marriott

SECON'04: **Sensor & Ad Hoc Communications and Networks** -- Distributed arrays of devices & sensors – applications – tutorials, technical sessions **[more]**

Oct 18-21: Stanford Sierra Camp

IEEE IRW: **Integrated Reliability Workshop –** at Fallen Leaf Lake - ensuring semiconductor reliability through component fabrication, design, characterization, and analysis tools; reliability of deep sub-micron, high speed devices **[more]**

Oct 25-29: San Jose Hilton

BroadNets'04: **International Conference on Broadband Networks** -- next-generation Optical and Wireless broadband networks with ultra-high bandwidth. **[more]**

Second Call for Papers: **ISQED'05** **[more]**

Upcoming Courses:

Quality Engineer Exam Prep class **[more]**
Pb-Free Solder: Reliability Issues **[more]**
Congestion Mgmt in Power Systems **[more]**
Transition From Individual to Mgr **[more]**
Breakthrough Project Management **[more]**

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IEEE **GRID** is the monthly newsmagazine of the San Francisco Bay Area Council of the Institute of Electrical and Electronics Engineers, Inc. As a medium for both news and opinion, the editorial objectives of IEEE **GRID** are to inform readers in a timely and objective manner of newsworthy IEEE activities taking place in and around the Bay Area; to publish the official calendar of events; to report on IEEE activities of a national and international scope; and to serve as a forum for comment on areas of concern to the engineering community by publishing contributed articles, invited editorials and letters to the editor.

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From the editor . . .

Dear Editor,

How do I know about upcoming Conferences and Calls for Papers?
Thanks,
Ramesh Chitor, IBM, Menlo Park

I get a number of email messages each month asking for advice about "navigating" the IEEE. Since I've been an active local and international Member for over 30 years, I have a lot of insight into how IEEE operates and were to find information.

The IEEE is a diffused Institute, broken down into nearly 40 "special interest groups" (we call them Societies) and also into geographic units (Chapters reporting to Sections, to Councils, to our Region 6). It can be very confusing.

So, to answer the question posed by Ramesh, here are several sources I can suggest to you:

- First, most of you belong to one or more Societies. Check their Magazines or Newsletters for upcoming events of interest to you. Review their Conference Calendar and the one-page CFPs and Notices there.
- If you don't belong to a Society but want to track their conferences, visit their websites occasionally. You can find the listing at www.ieee.org/organizations/tab/society.html.
- This is great for events around the world, but what about just for the Bay Area? For this, use the IEEE's search feature: www.ieee.org/conferencesearch/. You can limit the search to California and even to one specific Society (eg, Communications). You'll always find a web link to each event.
- And we have a limited listing of upcoming local conferences in our **GRID.pdf** Calendar toward the end of each issue; see it on page 27. The events highlighted in the **e-GRID** are our paid advertisers, and we especially encourage you to check these out, too.

Send me your opinions on what we're doing!

Paul Wesling **editor@e-grid.net**

NOTE: This PDF version of the IEEE GRID – the **GRID.pdf** – is a monthly publication and is issued a few days before the first of the month. It is not updated after that. Please refer to the Online edition and Interactive Calendar for the latest information: **www.e-GRID.net**

Santa Clara Valley Section:

K-12 Education Committee Needs Volunteers!

It's Back to School time in the Santa Clara Valley! The IEEE Santa Clara Valley K-12 Education committee needs volunteers to assist with...

- Book sorting
- Tutoring and mentoring
- Teaching teachers
- Funding/Donations
- Lego Robotics mentor
- Science Fair judges
- Laser Optics

Can you help out? Please see our listing of opportunities (right) and call David Fong 510-687-4507 or email **daffy@ieee.org** to see where we can best use your talents in helping children.

Our K-12 Opportunities This Year:

September: Lego Robotics (middle school) 2-3 hrs week/ 1 - 6 weeks
October: Lego Robotics (middle school) 2-3 hrs week/ 1 - 6 weeks
November: Lego Robotics (middle school) 2-3 hrs week/ 1 - 6 week
December: Gift of Reading: book sorting at San Jose Mercury, 2-4 hrs week/ 1 week
January: Lego Robotics (middle school)
February: Botball Training, 2-3 hrs week/ 1 - 6 weeks
February: Lego Robotics (middle school)
February: Engineer's Week
February: Tech Challenge, 2-3 hrs week/ 1 - 6 weeks
March: Synopsys Science Fair (sciencepalooza)
March: Science Fair Judge (Santa Clara Valley)
October-May: Mentor High school students interested in Engineering
May-June: Career Fair (high school) 2-3 hrs week/ 1 - 4 weeks

More Details at **www.ewh.ieee.org/r6/scv/k-12/**

UNIVERSITY OF CALIFORNIA, SANTA CRUZ

Information Systems and Technology Management

Assistant Professor Faculty Position #732-05
Associate or Full Professor Faculty Position #732**T**-05

The faculty in Information Systems and Technology Management (ISTM) at the University of California, Santa Cruz invite applications for tenured and tenure track (Assistant, Associate, and Full Professor) faculty positions. Due to the multidisciplinary nature of this program, we expect applicants to have diverse backgrounds, and a combination of undergraduate and graduate degrees in business/economics and engineering/computer science is suggested. Professional experience in industry or close research contacts with industry is preferred. The campus is especially interested in candidates who can contribute to the diversity and excellence of the academic community through their research, teaching, and service.

The emphasis of the program is systems at the boundary between technology and business, through the use of information systems, with a focus on (but not limited to):

- **Innovation Engineering and Management:** new product development and introduction, knowledge management including machine learning, e-business, supply chain management, multi-agent systems, mechanism design; stochastic optimization in enterprise management, finance engineering, computer-based process reengineering, Internet and Web based decision support systems, complex systems-of-systems, venture analytics
- **IT Management:** Data warehousing and data mining; network management; management and control of IT systems, data centers, and computer clusters; competitive use of information systems; software management

Applicants should submit a curriculum vitae; a statement of research plans; a statement of teaching interests; URLs of selected reprints; and ensure that at least **three** confidential letters of recommendation are sent directly, by the deadline of **December 10, 2004**. **We strongly encourage electronic submission of your materials**. Directions are given at www.soe.ucsc.edu/jobs/. All letters will be treated as confidential documents; please direct your references to UCSC's confidentiality statement at www2.ucsc.edu/ahr/policies/confstm.htm. Alternatively, application materials may be mailed to: Information Systems and Technology Management Search Committee, Baskin School of Engineering, 1156 High Street, University of California, Santa Cruz, California 95064. Please indicate clearly whether you are applying for an (**untenured**) Assistant Professor, a (**tenured**) Associate Professor or a Full Professor position. **Refer to position #732-05 for untenured or #732T-05 for tenured.** For further details about the Baskin School of Engineering at UCSC, see www.soe.ucsc.edu/.

IEEE Professional Skills Courses

SCV Chapters, Engineering Management & Components, Packaging and Manufacturing Technology Societies

Transitioning From Individual Contributor to Manager

Date/Time: Tuesday October 26, 8:30AM-4:30PM
Instructor: Roxanna Dunn, HP (retired)
Location: HP Training Center, Cupertino
Fee: $350 for IEEE Members; $425 non-members

The transition from individual contributor to manager can be the most challenging shift in a person's career. This program is designed to introduce prospective or newly promoted managers in a technical environment to the concepts and skills critical to a successful assumption of leadership.

"The class exceeded my expectations! It helped me understand my role and how my own skill set affects the way I lead. This course was very worthwhile."

ROXANNA DUNN holds a Masters in Education and an MBA in Information Technology. She spent 20 years managing engineers at Hewlett Packard Company, including a number of years developing business systems architectures. She weaves the conceptual view of academia with the real-world view of corporate experience and the integration view of architecture. Her emphasis is on how management methods connect long-range, high level plans with daily, individual activities.

Getting Things Done Across Organizational Borders

Date/Time: Wednesday October 27, 8:30AM-4:30PM
Instructor: Dr. Andrew Oravets
Location: HP Training Center, Cupertino
Fee: $350 for IEEE Members; $425 non-members

This seminar introduces you to innovative practices for dealing with people who do not report to you -- but whose assistance and support are critical.

"Great techniques for getting clear agreements and commitments. Andrew provides a mechanism to better understand and interpret personalities which we deal with daily"

DR. ANDREW ORAVETS brings over 25 years in senior positions at major corporations (NCR, Syntex and Hilton Hotels) to his seminars. During his corporate career he acquired "hands-on" skills and practical insights into corporate culture, large scale change, process improvement and managerial coaching.
Since becoming a consultant to companies such as Hewlett-Packard, Altera, Adobe Systems and CoSine Corporation, he has focused on enhancing the effectiveness of individuals, managers and teams by providing innovative principles and practices that apply to the challenges of change and leadership.

Breakthrough Project Management

Date/Time: Thurs-Friday, October 28-29, 8:30AM-4:30PM
Instructor: Richard Simonds
Location: HP Training Center, Cupertino
Fee: $575 for IEEE Members; $625 non-members

This 2-day course provides participants with a common methodology, terminology and tools that produce more efficient results and increased buy-in through improved visibility, reliability and consistency.

Key Topics: - Project Barriers & Breakthroughs - Team Development & Leadership - Define POS & Scope - Use the Trade-Off Flexibility Matrix - Make Fact-Based Decisions - Define Tasks - Create Work Breakdown Structure - Analyze Risks & Contingency Plans - Diagram Dependencies (CPM,PERT) - Manage the Project: Step-by-Step - Effective Meetings

"The methods and processes used for this class were not just tools and packages. They were a way to approach, manage and think, as well as communicate and deliver projects with less firefighting. I particularly liked the flexibility matrix, POS, risk analysis and critical path analysis."

RICHARD SIMONDS spent 21 years in business and industry (17 at Hewlett Packard) doing project management, business process improvement (quality), customer satisfaction systems (customer feedback), and product development, documentation, and training. He worked as a manager in many of these positions. He also spent 21 years in education with his latest assignment on the faculty at the University of California, Berkeley. Richard earned his Ph.D. in Instructional Technology from the University of Southern California. He was also the Executive Producer of award-winning media-based educational programs in the financial services industry.

Improve your skills – register for one of these classes, or for one coming up in November. Bring a team!

Presentation Skills for Engineers

Peter Rosselli -- at VeriSign (Mountain View), Nov 2, or at at Nokia (Mountain View), Nov 3.

Breakthrough Project Management

Richard Simonds -- at VeriSign (Mtn View), Nov 3-4.

Transitioning From Individual Contributor to Manager

Dr. Andrew Oravets -- at Exar (Fremont), Dec 9.

For complete information and registration form, see our Chapter website, right-hand column:

www.cpmt.org/scv/

The First IEEE Communications Society Conference on

Sensor and Ad Hoc Communications and Networks

- October 4-7
- Santa Clara Marriott

The convergence of the Internet, communications and information technologies, coupled with recent engineering advances, is paving the way for a new generation of inexpensive mobile devices, sensors and actuators. It is the distributed and ad hoc deployment of arrays of these network devices and sensors that bears promises for a significant impact, not only on science and engineering, but equally importantly on a broad range of applications relating to critical infrastructure protection and security, health care, the environment, energy, food safety, production processing, quality of life, and the economy.

This new IEEE Communications Society conference provides a forum to exchange ideas, techniques, and applications, discuss best practices, raise awareness and share experiences among researchers, practitioners, standards developers and policy makers in the field of sensor and ad hoc networks and systems. The conference is organized to provide for a degree of collegiality and continuity in the discussions of the various topics among participants from the industrial, governmental and academic sectors.

Tutorials on Monday

Tutorials cover the following topical areas:

- Monday AM: **MAC Protocols for Wireless Sensor Networks**
- Monday- PM: **Location Discovery in Sensor Networks**
- Monday all day: **Low Power Sensor Network Development with IEEE 802.15.4 and TinyOS**
- Monday all day: **Networks of Mobile Sensors**

Technical Session Themes:

- New architectures, protocols and access control to support communication, localization, time synchronization, routing and data dissemination
- Novel algorithms and theories for management, supervisory control and monitoring
- Industrial and commercial developments and applications
- Modeling and performance evaluation of large-scale distributed and ad hoc sensor networks
- Theories and models on fundamental information and communication aspects of wireless ad hoc and sensor networks
- Mechanisms for authenticated, secure communication and data dissemination in sensor and ad hoc networks
- Integration of sensors into engineered systems, including novel techniques for sensor renewable power sources, on-sensor self-calibration and self-testing
- Chip-based systems incorporating multiple sensors, computation, actuation, and wireless interfaces
- Software platforms, middleware and tools for ad hoc and sensor network applications development, deployment and management

Poster and Demo Sessions

The Advance Program is now posted. Pre-register, or register at the door. For more information, go to:

www.e-grid.net/conf/secon.html

Call for Papers

ISQED 2005
6th International Symposium on

QUALITY ELECTRONIC DESIGN

www.isqed.org

March 28-30, 2005
San Jose, CA, USA

Design for Quality in the Era of Uncertainty

ISQED is the pioneer and leading international conference dealing with the design for manufacturability and quality issues front-to-back. ISQED spans three days, Monday through Wednesday, in three parallel tracks, hosting near 100 technical presentations, six keynote speakers, two-three panel discussions, workshops/tutorials and other informal meetings. Conference proceedings are published by the IEEE Computer Society and hosted in the IEL/XPLORE digital library. Proceedings CD ROMs are published by ACM. In addition, continuing the tradition of reaching a wider readership in the IC design community, ISQED will continue to publish special issues in leading journals. The authors of high quality papers will be invited to submit an extended version of their papers for the special journal issues.

Papers are requested in the following areas

- **Design for Manufacturability & Quality**
- **Package - Design Interaction & Co-Design**
- **Design Verification and Design for Testability**
- **Embedded Test Methodologies**
- **Robust Device, Interconnect, and Circuits**
- **EDA Tools & IP Blocks; Interoperability and Implications**
- **Physical Design, Methodologies & Tools**
- **Effect of Technology on IC Design, Performance, Reliability & Yield**
- **Design Quality Definitions, Metrics, and Standards**
- **Quality Driven Design Flows; SoC, ASIC, FPGA, RF, Memory, etc.**
- **Quality of Modeling Abstractions and Methods (Device, Interconnect, Micro and Macro Cells, IP Blocks, ...)**
- **System-level Design, Methodologies & Tools**
- **Redundancy & Self Correction Design Techniques**
- **Management of Design Process, and Design Database**
- **Global, Social, and Economic Implications of Design Quality**
- **Quality based EDA Tools, Design Techniques, and Methodologies dealing with issues such as:**
  - ***Timing Closure***
  - ***R, L, C Extraction***
  - ***Ground/Vdd Bounce***
  - ***Signal Noise/Cross-Talk /Substrate Noise***
  - ***Voltage Drop, Power Rail Integrity***
  - ***Metal Migration, Hot Carriers***
  - ***High Frequency Effects***
  - ***Thermal Effects***
  - ***Power Estimation***
  - ***Plasma Induced Damage, and other yield limiting effects***
  - ***EMI/EMC***
  - ***Proximity Correction & Phase Shift Methods***
  - ***Verification (Layout, Circuit, Function, etc.)***
  - ***EOS/ESD***
  - ***Packaging Modeling and Simulations***

IMPORTANT DATES:

Paper Submission Deadline	**October 28, 2004**
Acceptance Notification	**November 17-19, 2004**
Final Camera-Ready Paper	**December 15, 2004**

Submission Process

The guidelines for the final paper format are provided on the conference web site at **www.isqed.org**. Authors should submit FULL-LENGTH, original, unpublished papers (Minimum 4, maximum 6 pages). To permit a blind review, do not include name(s) or affiliation(s) of the author(s) on the manuscript and abstract. Submit your papers using the **on-line** paper submission procedure available on the ISQED web site. Please check the as-printed appearance of your paper before submitting the paper. Address all other inquiries to **publication@isqed.org**.

IEEE International Integrated Reliability Workshop

- October 18-21, 2004
- Stanford Sierra Camp, Fallen Leaf Lake, South Lake Tahoe
- Technical Sessions, Tutorials

IRW'04 provides a unique environment for envisioning, developing, and sharing reliability technology for present and future semiconductor applications. All Workshop activities take place in a relaxed and rustic setting that promotes an atmosphere of interactive learning and knowledge sharing.

Hot reliability topics of the workshop are Cu-interconnects & low-k dielectrics, reliability of deep sub-micron, high speed, high frequency devices (e.g. SiGe), SOI devices, reliability modeling & simulation, and the reliability of future technologies such as molecular electronics and carbon nanotubes.

Nestled throughout the pines and cedars along the shoreline of Fallen Leaf Lake, a few miles from South Lake Tahoe, are clusters of 2 and 3 bedroom cabins furnished in the rustic style of an alpine resort. Each cabin cluster is equipped with shared bathroom facilities. All rooms have decks with magnificent views of Fallen Leaf Lake and surrounding Sierra peaks. The physical isolation of the location and the absence of distractions, such as in-room phones and television sets, encourages extensive interaction among the Workshop attendees.

Keynote Address: **Managing Tomorrow's Reliability Risks Today** – Timothy Forhan, Senior VP Corporate Reliability, AMI Semiconductor

Tutorials (included in registration fee):

- Gate Oxide Lifetime and Breakdown Degradation
- High-k Dielectrics: Instabilities, Defects
- EM Reliability-Cu/Low k Interconnects
- Advanced Back End of Line Reliability
- NBTI: What we know and need to know
- Modeling NBTI: Kinetics to Circuits
- Reliability of TFTs - Process to Device Issues

Because of limited space (120 attendees maximum) you are encouraged to register early.

For full information and registration, visit the **IRW'04** website:

www.e-grid.net/conf/irw.html

Sponsors: IEEE's Reliability and Electron Devices Societies.

SCV Education

WEDNESDAY SEPTEMBER 29

Are we Ready for the "Nano World", Education-wise?

Speaker: Prof. Cary Y. Yang, Santa Clara University
Time: 6:30PM Social, 7-8PM Presentation (no cost)
Place: Silicon Valley Technical Institute, 1762 Technology Drive, Suite #227, San Jose
RSVP: not required
Web: www.e-grid.net/docs/0409-scv-education.pdf

As Silicon Valley and the rest of the world brace themselves for the dawning of the nano era, one cannot help wondering, aside from the obvious question of hype versus reality, the extent to which this emerging industry will impact our entire education system. On one hand, one can view this excitement as an opportunity to harness the necessary energy and resource to improve and perhaps even overhaul our K-20 education. Even modest success in this direction would result in improved workforce preparation, not only for one industry, but for society in general. On the other hand, one must not lose sight of the impact and potential impact, both intended and unintended, of such a surge on the human condition. A natural question to raise is, will the benefits far outweigh the potential harm, if any? This consideration would create yet another opportunity for further study among social scientists and technologists. These two contrasting but complementary scenarios will be discussed.

Cary Y. Yang received the B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Pennsylvania in 1970, 1971, and 1975, respectively. After working in various research positions at M.I.T., Stanford, and NASA, he founded Surface Analytic Research, Inc. in Mountain View, California and directed sponsored research in surface and nanostructure science. In 1983 he joined Santa Clara University and is currently Professor of Electrical Engineering, Associate Dean of Engineering, and Director of the Center for Nanostructures. Over the past two decades, Professor Yang has initiated innovative programs to educate and train technical professionals in various stages of their careers. In the eighties, he developed and organized short courses on timely topics in silicon technology to Silicon Valley professionals. In the mid-nineties, he offered short courses on semiconductor technology for SEMI as part of a retraining program for professionals in other fields. Since the mid eighties, he has provided opportunities for his students to spend extended periods in companies in Japan, where they collaborated with their hosts on their thesis research. More recently, he founded the Center for Nanostructures at Santa Clara, which offers interdisciplinary research and education opportunities for university students and faculty, high school students and teachers, as well as Silicon Valley technical professionals.

Dr. Yang has been a consultant to industry and government, and a visiting professor at Tokyo Institute of Technology, University of Tsukuba, National University of Singapore, the University of Pennsylvania, and the University of California, Berkeley. He is a Fellow of IEEE and served as Santa Clara Valley Chapter Chair, Regions/Chapters Chair, Vice President, and President of the IEEE Electron Devices Society. From 2002 to 2003, he served as an elected member of the IEEE Board of Directors, representing Division I. He was an editor of the IEEE Transactions on Electron Devices, in the area of MOS devices.

SCV Solid State Circuits

WEDNESDAY SEPTEMBER 29

Trends in High-performance Computer Aided Design

Speaker: Dr. Zoltan Cendes, Founder and CTO, Ansoft Corp, IEEE Fellow, IEEE AP-S Distinguished Lecturer
Time: 6:30PM Social, 7:00PM Presentation (no cost)
Place: Cadence Design Systems, Bldg. 5, 2655 Seely Ave., San Jose
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/ssc/Sep2904.htm

Dr. Zoltan Cendes is Founder and Chairman of Ansoft Corporation, Pittsburgh, PA. He has been a Professor of Electrical and Computer Engineering at Carnegie Mellon University, an Associate Professor of Electrical Engineering at McGill University, Montreal, Canada, and an Engineer with the Corporate Research and Development Center of the General Electric Company in Schenectady, NY. Dr. Cendes received his MS and PhD degrees in Electrical Engineering from McGill University and his BSE degree from the University of Michigan. He is a Fellow of the IEEE and is an IEEE AP-S Distinguished Lecturer.

GHz frequencies, Gb/s transmission rates and Gsps sampling rates are typical in today's high-performance electronics design. Time domain metrics such as eye-diagrams, TDR measurements and jitter are now appearing simultaneously on the same spec sheet with frequency domain metrics such as gain, phase noise, and insertion loss. Large transistor counts, high non-linearities and increased full-wave behavior of on-chip and on-board interconnects have become commonplace. This talk will describe the revolution in electronic design tools that is occurring to meet these challenges. It will describe new approaches to circuit simulation that integrate transient simulation with harmonic balance to handle the complexities of modern monolithic RF circuits. It will describe procedures that combine electromagnetic field simulation with electrical circuit simulation for modeling antenna feed networks, on-chip interconnects, IC packages, and other passive structures. And it will explain the seamless integration of 3D electromagnetics with circuit simulation currently used at IC foundries to model complex RFICs. Ansoft's recent work on Ultra-Wideband radio design, the Xilinx 10 Gb/s Backplane Design Kit, antenna feed and monopulse network EM/circuit co-design, and on-chip spiral inductors based on UMC foundry technology will be presented as application examples.

SCV Reliability

WEDNESDAY SEPTEMBER 29

Are You Analyzing Reliability Data Correctly? Repairable Vs. Non-Repairable Systems: There Is a Difference

Speaker: David Trindade, Sun Microsystems
Time: 6:30PM Social, 7PM Presentation (no cost)
Place: HP-Cupertino Oak Room, Bldg 48. Just North of Hwy 280 (Wolfe Rd Exit) at the corner of Pruneridge Ave. and Wolfe Rd
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/rs/

Dr. David Trindade is a Distinguished Engineer in the Customer Advocates for Reliability (CSCARE) Office of Sun Microsystems, Inc. His previous positions include: Senior Director of Software Quality at Phoenix Technologies, Director of Reliability, Director of Applied Statistics, and the first Senior Fellow at AMD, Worldwide Director of Quality and Reliability at General Instrument, and Advisory Engineer at IBM. His fields of expertise include: statistical analysis and modeling of software, component, and system reliability, and applied statistics, especially design of experiments (DOE) and statistical process control (SPC). He is co-author (with Dr. Paul Tobias) of the book Applied Reliability, 2nd ed., published in 1995. He has been an adjunct faculty member in the Department of Applied Mathematics at Santa Clara University. He has a BS in Physics, an MS in Statistics, an MS in Material Sciences and Semiconductor Physics, and a Ph.D. in Mechanical Engineering and Statistics.

We are all familiar with repairable systems: computers, servers, automobiles, TVs, circuit boards, production equipment, software programs, and so on. If we wanted to model the reliability behavior of such systems, we'd be surprised to discover that the reliability literature focuses mainly on models for the analysis of non-repairable systems. What are the major distinctions between repairable and non-repairable systems? When is MTBF justified for modeling? How could we get into trouble and produce misleading results by applying techniques for the analysis of non-repairable systems to data for repairable systems? In this talk we'll illustrate some pitfalls involving MTBFs and the misapplication of techniques such as probability plotting to repairable system analysis. We'll show some simple graphical and analytical techniques that can be very effective for the analysis and modeling of time dependent repairable system data.

SCV Engineering Management

WEDNESDAY SEPTEMBER 29

The Case For Starting a Business for Yourself … and In Silicon Valley:

Forum: The Art of Commitment and The Science of Change

Speaker: Cynthia Scott, PhD., M.P.H.
Time: 6:00 PM

Presentation: Walking A Tight Rope with Resilient Packet Rings -- A Startup Story

Speaker: Nirmal R. Saxena, VP of Engineering and CTO, Alliance Semiconductor
Time: 7:45 PM

Time: Forum at 6:00pm, Dinner at 7:00pm, after dinner presentation at 7:45pm
Place: PRIME Hotel (former Wyndham), 1300 Chesapeake Terrace, Sunnyvale - off Lawrence Expy/ Caribbean Drive at Hwy 237
Reservations: through website: www.ieee-scv-ems.org
Cost: (with reservations thru Friday Sept 24): $25 (IEEE member), $30 (non member), $5 surcharge thereafter (cash or check at the door). Student IEEE members - $5.
Other information: leave message with Rich Hendrickson at (408) 203-3462

Before-Dinner Forum presentation **-**

The Art of Commitment and The Science of Change

Have you been through enough organizational change to make you curious to find out what you know and might want to know more? Are you currently involved in or leading a change in your organization? Want to increase your competency and capacity to lead and benefit from change? Dr. Scott has provided the models and tools for a wide variety of mergers, cultural transformations, and structural changes over the past 20 years. She will use her books **Getting Your Organization to Change, Managing Change at Work** and **Rekindling Commitment** as a foundation to talk about a basic way to think about mobilizing, designing and implementing change to create organizational performance. She will share her experience from a wide variety of organizations and give you a "change agents" perspective from working at all levels in organizations.

Cynthia Scott is an organizational consultant, author and coach. The depth, scope, and quality of Cynthia's experience have made her a preferred change management resource for Fortune-500 multinational corporations and for smaller, regional firms in a broad spectrum of corporate leaders, including financial, healthcare, high technology, and government sectors.

Cynthia's expertise includes organizational effectiveness, management development, CEO coaching, senior team development, and the strategic planning and implementation of organizational change. She is a frequent keynote speaker at national conferences on the topics of: Leadership, Mastering Change, and Minimizing Risk and Maximizing Performance. Reports of Dr. Scott's work have been featured in publications such as the **Wall Street Journal, Business Week** and the Stanford Business School Newsletter.

Cynthia Scott is co-author of 14 books, among them: **Take This Job and Love it, Getting Your Organization to Change, Rekindling Commitment, Managing Organizational Change, Empowerment, Organizational Mission, Vision and Values,** and numerous articles in management and trade journals.

She holds a Ph.D. in Psychology from the Fielding Institute, a M.P.H. in Health Planning and Administration from the University of Michigan and a B.A. in Anthropology from University of California, Berkeley.

After-Dinner presentation **-**

Walking A Tight Rope with Resilient Packet Rings-- A Startup Story

"Walking a tightrope" is about the technical and management challenges faced at startup (year 2001) and since at Chip Engines (now part of Alliance Semiconductor). Chip Engines was designing chips while the IEEE 802.17 Resilient Packet Ring Working Group was still defining the standard. The main thrust of this talk covers:

- insights (based on real experience) that guide developers in anticipating changes and planning workarounds in the midst of changing requirements.

- challenges faced in working with engineering teams distributed around the globe.

Dr. Nirmal R. Saxena will apply his first hand experience of engineering management as the VP of Engineering and CTO at Alliance Semiconductor. He is responsible for the architecture definition, engineering management, and new product development. Dr Saxena is also a Consulting Faculty in the Electrical Engineering Department at Stanford University.

Prior to joining Alliance, he was VP of Architecture at Chip Engines where he was responsible for the design and development of Resilient Packet Ring controllers. Dr Saxena has served in senior technical and management positions at Tiara Networks (now Tasman Networks), the Stanford Center for Reliable Computing, Silicon Graphics, HaL Computers, and Hewlett Packard.

Dr Saxena holds a BE degree from Osmania University, India; a MSEE degree from the University of Iowa; and a Ph.D. EE degree from Stanford University. He holds more than 10 patents and has published in the IEEE Transactions. He is a Fellow of IEEE (2002) and was cited for his contributions to reliable computing.

SCV Entrepreneurs Special Interest Group

FRIDAYS October 1, 8, 15, 22, 29

Weekly Meeting

Time: 3:00 - 5:00 P.M.
Place: NOVA Private Industry Council - CONNECT! Workshop Center
"Palo Alto" Room (inside 767)
505 W. Olive Avenue
Sunnyvale
Map: www.novapic.org/contact_us/

Info: For further information contact Art Rahman, Chair of IEEE CNSV, at ataur.rahman@worldnet.att.net
Web: www.ieee-sv-consult.org/

The Entrepreneurs SIG – a part of the Consultants' Network of Silicon Valley – meets most weeks on Friday afternoon. You are invited to attend.

For specific information, please contact the SIG chair, Art Rahman: ataur.rahman@worldnet.att.net

SCV PACE

THURSDAY SEPTEMBER 30

Career Defense in the Face of Globalization

Speaker: George McClure, IEEE Life Fellow, Director-elect for Region 3
Time: 6:30 - 9 PM
Cost: $10 - includes refreshments (PayPal link on website)
Place: Cadence, Building 5, 2655 Seely Ave, San Jose (map on website)
RSVP: see website for registration form
Web: www.ewh.ieee.org/r6/scv/PACE/Lecture_McClure.htm

SF PACE

SATURDAY OCTOBER 2

Career Defense in the Face of Globalization

Speaker: George McClure, IEEE Life Fellow, Director-elect for Region 3
Time: Noon (lunch will be provided)
Cost: no cost
Place: San Francisco State Univ Science Building, Room 210, San Francisco
RSVP: not required
Web: http://www.ieee.org/sf/section_pdf/Oct_02_SF_PACE.pdf
Information: Dan Sparks, (415) 260-4613

The talk traces the development of the outsourcing movement, and the growth in the movement of information technology work offshore. The trend started with call centers and business operations, but gradually, the skill level of work sent abroad has increased, to include software development and engineering design. While the trend has been accelerating, and is likely not reversible, ways are discussed that IEEE members can use to direct their own careers to minimize their vulnerability to being displaced by it.

George F. McClure

Having worked as a teacher, design engineer, a systems engineer, a technical director, a research & technology manager, a program manager and an engineering department manager, George McClure has experienced and appreciated all aspects of an engineering career.

In professional activities for IEEE-USA, he chaired the Pensions Committee, organized the program for several PACE Conferences, and served on the board for United States Activities as chair for the Career Activities Council. More recently, he has served as vice chair for Technology Policy Activities, as editor for Technology Policy, as a member of the Communications Committee, as past chair of the Career & Workforce Policy Committee, and as a member of the regional PACE Committee. For his work with IEEE-USA, in 1999 he was awarded the "Distinguished Contributions to Engineering Professionalism," their highest award.

Currently, he serves as Director-elect for Region 3, as chair of the Communications Committee for IEEE-USA, and as member of the Individual Benefits & Services Committee. He is also a member of the Board of Governors for the IEEE Vehicular Technology Society.

An IEEE Life Fellow, Mr. McClure has over 30 years' experience in military and commercial communications system design in industry.

SCV Lasers and ElectroOptics

TUESDAY OCTOBER 5

Photonics CMOS Compatibility using Molecularly Engineered Materials

Speaker: Dr. Ron Kubacki, Ionic Systems
Time: Networking and Pizza Social at 7:00 pm, Presentation at 8:00 pm
Place: National Semiconductor Credit Union Auditorium, 955 Kifer Road, Sunnyvale
RSVP: to ramsivaraman@ieee.org

Dr. Ron Kubacki received an Sc.D. in Physics in 1976 and founded Ionic Systems in 1979 after holding positions at Bell and Howell, Armorlite Corp. and Tencor Instruments. He has guided the development of revolutionary PECVD technology and materials since that time. He has presented numerous papers, and is again an invited speaker at Photonics West 2005, on work for the US Department of Energy, Missile Defense Agency, Defense Threat Reduction Agency, and National Science Foundation in material development for advanced microelectronic and photonic devices.

The monolithic, on-chip integration of CMOS microelectronics with photonics is inevitable and benefits both technologies. Photonic integration to microelectronics on-chip provides such solutions as overcoming microprocessor communication roadblocks through the use of optical interconnection. Conversely, microelectronic integration provides benefits to photonic structures by optimizing electronic signals generated by photonic biosensors for example. Photonic integration must complement, build on, and enhance the existing state of CMOS microelectronic technology for practical implementation. Photonic approaches that ignore the realities of CMOS architectures (such as power and thermal limitations), provide little benefit to the CMOS device performance, are incompatible with CMOS silicon manufacturing processes, or are incapable of providing levels of long term reliability already well demonstrated by microelectronic devices, provide little incentive for on-chip photonic/microelectronic integration.

Dr. Kubacki will detail architectures to integrate photonics and microelectronics that address CMOS fabrication realities, increase performance of both the electronic and optical functions, and maintain current levels of reliability. Fabricating these structures with the limited CMOS material set and/or typical photonic materials has proven challenging and produced less than ideal results. Nanotechnology presents the opportunity to molecularly engineer materials such as self assembled silicon quantum dot nanocomposites. Nanocomposites can provide useful and in many instances, unique properties, such as Variable In Plane Index of Refraction (VIPIR®), that permits embedding of optical elements in waveguide structures. This presentation will focus on the ability of nano-engineering to provide near term solutions to technical challenges. Dr. Kubacki will present results from the development of both active and passive materials that enable practical fabrication of photonic structures on CMOS microelectronic devices. Examples will be given of characteristics and results for optical interconnect and sensing applications. The role of Small Business Innovative Research (SBIR) funding in the ten year development of the presented materials and processes will be briefly discussed.

SCV Control Systems

THURSDAY OCTOBER 7

Shortcuts to Step Motor Selection

Speaker: Ted Lin, Lin Engineering
Time: 7:00 PM - 8:30PM
Place: Room 230, Sullivan Engineering Center (Bldg 404), Santa Clara Univ, Santa Clara
Parking: Free, in parking structure (Bldg 714)
Registration: not required
Information and Map: www.ewh.ieee.org/r6/scv/css/

Ted T. Lin is a recognized technology leader in the field of step motors, spindle motors, voice coil actuators and control devices. He received a M.S. degree in physics from Northern Illinois University. He is an experienced technologist, holds eight patents and is the author of twelve publications. Mr. Lin's technical experience covers several fields of science including magnetic field design and control, mechanical structures and electronic control systems. He has been involved with the design of motors and components for hard disk drives since 1982. During his career, he has served as Manager of Advanced Motor Development for Warner Electric and Executive VP for Rotorque Technology. He is the President and CEO of Lin Engineering, a company that he founded.

Most step motor sales engineers would like to know the dynamic torque requirement of the application before selecting a motor for their prospective customers. However, this is the most difficult question for a step motor user to answer. Therefore, the sales engineer will request the user's holding torque requirement rather than the dynamic torque. When the motor does not work, the sales engineer selects another motor with higher holding torque, but this motor also fails. Thus a trial and error process begins. In reality, the motor with higher holding torque does not always give you a higher dynamic torque. It depends on the operating speed. Also, the motor with a higher holding torque always come with large rotor inertia, which will slow down the acceleration. There are several key factors outlined in the presentation that will help eliminate the trial and error between the step motor manufacturer and the customer engineer. For engineers with no time to waste, "Shortcuts to Step Motor Selection" is the perennial reference presentation for understanding step motor behavior.

SCV Signal Processing

MONDAY OCTOBER 11

Converting MATLAB Algorithms to FPGA or ASIC Designs

Speaker: Michael Bohm, CTO, Vice President, AccelChip
Time: 6:30pm: Fast Food & drinks ($1 Donation Recommended); 7:00pm: Presentation
Place: National Semiconductor Credit Union Building (Building 31), 955 Kifer Rd., Sunnyvale (Near Lawrence and Central Expy)
Registration: not required
Information and Directions: www.ewh.ieee.org/r6/sps/

Michael Bohm is the chief technology officer and vice president of Engineering for AccelChip Inc. Bohm was most recently chief scientist and Technology Fellow for Mentor Graphics.

Prior to AccelChip and Mentor Graphics, Bohm ran IC/ASIC development at Harris Semiconductor, where he worked closely with the founders of Synopsys when they started their company in Research Triangle Park, North Carolina. Bohm worked onsite at Synopsys/Cadence/Cross Creek as a Harris semiconductor employee from 1989 - 1991, where he contributed to the development of their Design Compiler technology.

Bohm joined Mentor Graphics in 1991 and led the development of AutoLogic II. He later became vice president and chief scientist at Exemplar. When Mentor Graphics folded Exemplar into the company, Bohm oversaw the technical development and direction of their HDL tool set for FPGA design. He holds a B.S. in Electrical Engineering degree from the Florida Institute of Technology.

In the DSP domain, MATLAB is the DSL of choice with 97% of DSP design implemented on dedicated DSP processors. MATLAB provides both an efficient system-level verification environment and an efficient path to implementation. Unfortunately, the process of converting MATLAB to "C" code to run on the processor is reaching its limits. A DSP processor's inherent limitation of serial operation is becoming a bottleneck for advanced high-performance algorithms. To solve this problem, a new methodology must be in place to convert algorithmic MATLAB to a register-transfer language (RTL) that can be used by industry-standard synthesis and verification tools. Companies that use the new methodology will benefit from greater productivity, both in terms of the domain-specific language and from the new breed of best-in-class tools they will enable.

This presentation will show the process of taking a MATLAB algorithm down to a silicon representation. It will demonstrate a design style and methodology for implementing this algorithm in either an FPGA or an ASIC.

SCV ELECTRON DEVICES

THURSDAY OCTOBER 12

Myths and Truths about High-K/Metal Gate Stack Technology

Speaker: Dr. B. H. Lee, IBM assignee, Front End Process Devision, International SEMATECH
Time: Pizza social at 6:00pm; Presentation at 6:15pm
Place: National Semiconductor Corp. Building 31 Large Auditorium, 955 Kifer Road, Sunnyvale
Cost: Free
Registration: not required
Information: Philippe.Jansen@nsc.com

Recent studies on the device instability of high-k devices indicate that the methodologies developed for electrical characterization of MOS devices with SiO2 gate dielectric may not be accurate enough for high-k devices. While the physical origin of instabilities in high-k devices is yet to be identified, it is found that many of the abnormal electrical characteristics of high-k devices can be explained by assuming fast and slow transient charging in high-k dielectric. In this talk, transient charging effects in high-k gate dielectrics will be reviewed and its implications on test methodologies will be discussed.

Byoung Hun Lee received a B.S. (1989) and a M.S. (1992) in Physics from Korea Advanced Institute of Science and Technology and Ph.D (2000) in electrical and computer engineering from the University of Texas at Austin. He is an IBM assignee to International SEMATECH (ISMT) and manager of the advanced gate stack program, leading the development of metal/high-k gate stack technology. He has authored and co-authored more than 100 journal and conference papers in various semiconductor research areas including gate oxide reliability, SOI devices and processes, strained silicon devices, and high-k and metal gate processes and devices.

One-Day IEEE Short Course:

"Mandated Pb-Free Solder Assemblies: Exploring the Transition's Impact on Product Reliability"

- Tuesday, October 5, 2004
- At Hewlett-Packard Co, 10435 N. Tantau, Cupertino
- 8:00 AM Registration; 8:30 AM - 4:30 PM Symposium
- Fee: $125 (IEEE Members), $150 (non-Members)
- For managers, engineers, program/production mgrs

As governments in Europe and Asia begin the phase-in of their "Removal of Hazardous Substances" regulations, electronics designers and manufacturers are in the final stages of changing from classic tin-lead solders to various compositions of Pb-free solders. The industry has 100 years of experience and reliability optimization for tin-lead solders; the new solders present us with considerable uncertainty. Will our computers, wireless devices, and other products show considerably lower reliability over the next few years? What are the risks for which we must be planning?

The focus in this special one-day event is on the technical engineering impact of the transition. What do we know, what do we not know, and where are the remaining significant risks?

Lectures:

- "**Lead-Free Solder Joint Reliability**" - Jean-Paul Clech, Solder Reliability Solutions
- "**Managing Compatibilities for Lead-Free Transition and Environmental Compliance**" - Dr. Dongkai Shangguan, Flextronics
- "**Failures at the Customer and the Influence of Pb-Free**" - Dr. Craig Hillman, Univ of Maryland
- Plus panel discussions based on attendee concerns, experiences

More Information: **www.cpmt.org/scv/**

SCV Components, Packaging & Manufacturing Technology

WEDNESDAY OCTOBER 13

A Novel X-ray Microtomography System with High Resolution and Throughput For Non-Destructive Imaging of Advanced Packages

Speaker: David Scott, Xradia; and

µCT Techniques In Combined 2D/3D High Resolution X-ray Systems

Speaker: Dr. Udo Frank, Feinfocus

Time: Seated dinner at 6:30; Presentation 7:30
Cost: $25 if reserved before Oct 9;
$30 after & at door
Place: Ramada Inn, 1217 Wildwood Ave (Fwy 101 frontage road, between Lawrence Expressway and Great America Parkway), Sunnyvale
RSVP: to allen.m.earman@intel.com
Web & Map: www.cpmt.org/scv

David D. Scott received his BS in Aerospace Engineering from the Univ of Kansas and his MS in Biomedical Engineering from the Univ of Colorado. He served as Senior Biomedical Engineer at Walter Reed Army Institute of Research, Washington, DC, and then as a Medical Technology Program Staff Scientist at Lawrence Livermore National Laboratory. At LLNL he was Lead Project Engineer for a three-year $11M medical imaging system, performed algorithm development and implementation of tomographic imaging algorithms and graphical user interface, and was in charge of algorithm implementation on DSP's and hardware software interface. He is currently Product Line Manager for Xradia, Inc., Concord.

Udo E. Frank is the Director of Technology Development of FEINFOCUS GmbH, Germany. He studied physics and chemistry, and received his Ph.D. in molecular physics from the University of Ulm, Germany. Dr. Frank joined FEINFOCUS in 1992, and has gained a comprehensive knowledge of high-resolution X-ray microscopy. He is an expert especially in the inspection of electronic components. During the last five years, under his direction, the FEINFOCUS R&D team has developed several innovative high-resolution X-ray systems with revolutionary new operating and functional designs, several of which have been honored with respected industry awards.

"A Novel X-ray Microtomography System" -- Complex advanced package designs present challenging problems for the failure analysis community. X-ray imaging techniques provide a unique way to perform package FA non-destructively, however, the complexity of the new advanced packages proves problematic for 2D x-ray imaging alone. Xradia's Micro-XCT 3D tomographic imaging microscope resolves this problem by providing high resolution 3D imaging of advanced IC structures non-invasively. The Micro-XCT system has demonstrated visualization of wire bond lifts, solder-bump non-wetting problems, solder wicking, voids, cracks and delaminations that are difficult if not impossible to image using 2D x-ray techniques.

The Micro-XCT includes a fully automated tomographic data acquisition system and real-time reconstruction engine. An interactive 3D visualization package allows the user to view and analyze the 3D data in various ways, including 3D rendering and virtual cross-sectioning and de-layering. The system's unique capability of imaging at high-resolution without compromising throughput makes it a powerful tool in non-destructive imaging applications for Advanced Package FA as well as microtechnology and biotechnology (for example, imaging embedded MEMs structures, material stress failure mode analysis, bone implant interface, etc). Since it is non-destructive it is ideally suited for stress and thermal fatigue testing, new process development and failure analysis.

"µCT Techniques In Combined 2D/3D High Resolution X-ray Systems" -- All physical objects, we know, are 3-dimensional. But X-ray inspection shows only 2-dimensional shadow images of their absorption structure. Micro- or even nanofocus X-ray systems provide 2D resolution below 1 µm for inspecting small hidden structures - widely used in the electronics industry (BGA, Flip Chip, CSP, bond wires, die-attach, PCB, etc.) For many applications images of 2D X-ray inspection provide sufficient information for conceiving even the third dimension of a sample. Nevertheless, recent developments have made available various techniques for complete 3D reconstruction of small samples using axial or planar computed tomography. The talk will give an overview on that technique, showing practical examples and images.

WEDNESDAY OCTOBER 13

Digital Rights Management for Mobile Content

Speaker: Chris Parkerson, RSA Security
Time: 6:00 p.m. (pizza & soda), 6:30 p.m. presentation
Fee: $1 donation to partially cover food cost
Place: National Semiconductor Credit Union, Bldg. 31, 955 Kifer Rd., Sunnyvale, CA
RSVP (required): rsvp@comsocscv.org
Web Site: http://www.comsocscv.org

Chris Parkerson is the DRM Evangelist at RSA Security. In his role, Chris is responsible for market strategy and messaging for all RSA developer solutions. Chris has a long history of working with developers and has worked with several pioneering companies in XML and Web Services technology prior to joining RSA. He has worked as a product manager for two Valley start-ups including Vianeta Communications which provides XML-based solutions for health information management and Ipedo which provides XML-based solutions for enterprise information integration. Prior to the move to the West, Chris was a product manager for eXcelon Corp. where he was responsible for the first XML database, XIS, and first XML application development environment, Stylus Studio, on the market. Chris graduated from Boston University with a BS in Computer Systems Engineering.

Forrester Research predicts that digital content owners will be losing $4.6 billion per year by 2005 due to piracy. This has created an impetus in the market to find solutions that will protect the rights of content owners in the digital world. However, to date, most rights management solutions have been hard to use, easy to circumvent, or place unnecessary restrictions on consumers.

Successful digital content services such as Apple's iTunes have proven that a significant segment of consumers will pay for protected digital content if the process is as frictionless as possible. Consumers believe that the digital content they pay for should be usable on any device they own, from their personal computer to their portable music player to their home or car stereo. The only way to provide this content portability is by enabling rights portability through a trusted value chain that binds the identity of consumers to their devices and licensed content and the identity of devices to the network. Creating this network of trusted devices will give consumers the content portability they want by ensuring that content providers can trust the devices they own. Enabling these trusted devices requires strong security capabilities to be built into the devices to protect the rights of content owners. Content providers also want to tap into the popularity of "peer-to-peer" services by offering legal versions of these services that offer the advantages of viral marketing with the confidence that their content is suitably protected. All of this helps create a frictionless commerce experience that provides significant value to consumers over "free" services.

The industry is already working on putting the infrastructure in place to build this trusted network. Standards bodies like the Open Mobile Alliance (OMA) are working to develop rights management standards that are widely supported by content owners, service providers, and device manufacturers. The standards utilize existing, proven security technologies in the areas of encryption and public key infrastructure combined with new protocols and techniques to enable rights portability. Participants in this session will learn about these standards efforts underway, the security hurdles that must be overcome to deliver a digital rights management system as ubiquitous and transparent as SSL is to e-commerce, and the technologies and principles currently being used that will facilitate faster creation of this network of trusted devices.

THURSDAY OCTOBER 14

The Design of WCDMA Zero-IF Receivers: System and Circuit Issues

Speaker: Osama Shana'a, Maxim Integrated Products
Time: 6pm - Refreshments and Social Hour,
7pm - Technical Presentation
Place: Agilent Technologies, Santa Cruz conference room, Bldg 50, 5301 Stevens Creek Blvd, Santa Clara
RSVP: not required
Web & Map: www.mtt-scv.org/

Osama Shana'a (S'95, M'00, SM'02) received his B.Sc. degree in electrical engineering with high honor from University of Jordan, Amman, Jordan, in 1992. In 1994 he was awarded the Fulbright Scholarship to pursue an M.S.EE degree from Portland State University, which he received in 1996. He received his Ph.D. degree in electrical engineering from Stanford University in 2000. In the summer of 1995, he joined Radio Comm. Corp., Portland OR, where he worked on the design of a fully integrated RF transceiver for the ISM band applications. In the summer of 1997, he joined National Semiconductor, Santa Clara CA, where he lead a team to work on mixed signal megacell shareability. Since June 1998 he is with Maxim Integrated Products, Sunnyvale CA, where he has led many successful RF wireless designs for PCS, CDMA, WCDMA, WLAN chipsets as well as circuits for TV tuner applications. Dr. Shana'a is a member of the Eta Kappa Nu honor society, and a senior IEEE member.

Direct-Conversion architecture is currently the architecture of choice for 3G WCDMA handsets receiver. Many related design challenges are overcome through the proper use of Silicon process, circuit design techniques, and architecture implementation. The direct-conversion receiver architecture facilitates the complete integration of the radio section on chip, resulting in a lower cost and smaller radio solution. In this talk, we present an overview of the direct-conversion receiver IC architecture for 3G WCDMA FDD radio along with some key RF system issues and integrated circuit implementation challenges. These issues include DC-offsets, LO and interferer leakage, LO phase noise, I/Q channel mismatch, baseband channel filtering, and 2nd order distortion products in a Zero-IF receiver.

SCV Magnetics

TUESDAY OCTOBER 19

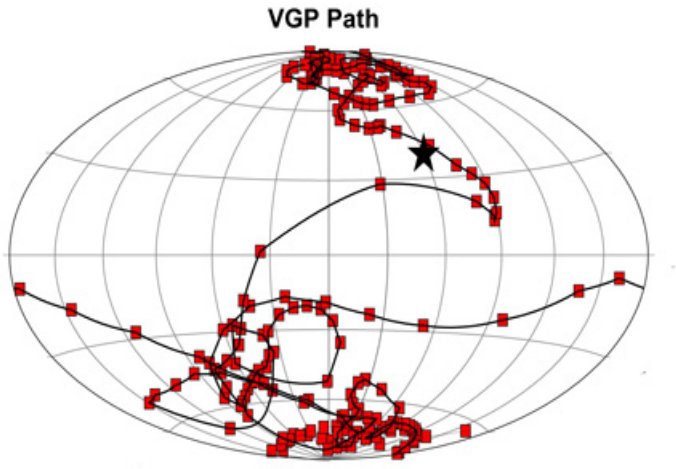
Is the Next Geomagnetic Reversal Imminent?

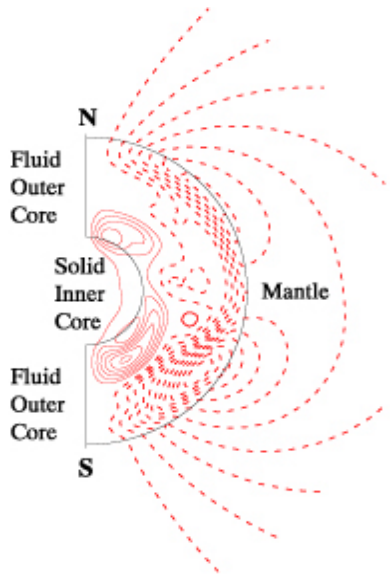
Speaker: Rob Coe, Earth Sciences Department and Institute of Geophysics and Planetary Physics, UC-Santa Cruz
Time: Coffee and conversation at 7:30 p.m. Presentation at 8:00
Place: Komag, 1710 Automation Parkway, San Jose
RSVP: not required
Web & Map: www.e-grid.net/docs/0410-scv-mag.pdf

Robert S. Coe holds a B.A. in Chemistry and Physics from Harvard College, and an MA and PhD in Geophysics from UC-Berkeley. He is a professor at UC Santa Cruz, and has served as chair of the Earth Sciences Department and as Associate Director, of the UCSC Institute of Tectonics. He was President of the Geomagnetism/Paleomagnetism Section, American Geophysical Union.

Dr. Coe's research interests include the Earth's geomagnetic field over geologic time (reversals, excursions, and intensity variation); Paleogeography (the assembling and subsequent deformation of Asia and the western U.S.); rock and mineral magnetism; and solid-solid phase transitions under nonhydrostatic stress.

The only evidence we have that the Earth's magnetic field has occasionally reversed polarity comes from paleomagnetism, the study of ancient magnetization carried by rocks. Reversals occur quickly on geological time scales, straining the resolution of natural magnetic recorders. During the transition the field appears to change direction rapidly, perhaps chaotically. What we can say with most certainty is that the field intensity drops by a factor of 3 to 10 as polarity reverses. Currently, the strength of the dipole field is decreasing at a rate that would reach zero in 1200 years. Evidence from fired archeological objects and historic lava flows shows that it has been decreasing monotonically for the past 1500-2,000 years, when it was 40-50 percent higher than today. In the past ten million years we have had about 50 reversals, which occur at irregular intervals that approximately fit a Poisson process. The last reversal was 780,000 years ago, so one might be tempted to say that a reversal is overdue. Indeed, some scientists have speculated that the current, accelerating decrease in field strength signals the approach to the next reversal. In this talk I will explain why, from the perspective of paleomagnetism, this speculation not likely true. I will explain how we study reversals recorded in the rock record and also present some results from Glatzmaier and Roberts geodynamo simulations.





Snapshot During an Aborted Reversal

Broken lines = Reversed magnetic polarity
Solid lines = Normal magnetic polarity

(Longitudinally-averaged poloidal magnetic field)

SCV Consultants' Network

TUESDAY OCTOBER 19

What an Engineer Needs to Know about Business

Speaker: Dave Conrath, Dean, College of Business, San Jose State University
Time: 7:00 PM Informal Networking, 7:15 Formal Networking, 7:30 PM Meeting Starts
Place: Sheraton Hotel, 1100 North Matilda Ave, Sunnyvale
RSVP: not required. SEATING IS LIMITED, so arrive early
Web: www.ieee-sv-consult.org/200410.htm

Our speaker is Dean **Dave Conrath** of the College of Business of San Jose State University. Dave brings with him both a cross disciplinary and an international perspective. While he has been the dean of two business schools (the DeGroote School of Business at McMaster University, and San Jose State), the majority of his career has been spent in a Faculty of Engineering (University of Waterloo). This is partly because his research interests lie at the interface of high technology (communication and computer) and human behavior and organizational structure. The international aspect comes from having lived in over 30 places in four countries on three continents.

Dave started his academic career at the University of California, moving from there to a position at the Wharton School, University of Pennsylvania. His other permanent positions have been at the schools mentioned in the preceding paragraph. He also has had extensive teaching and research relationships with the Université d'Aix-Marseille III in France and Nanyang Technological University in Singapore. He has published more than 100 refereed papers in academic journals and conference proceedings, as well as several books and monographs. And he consulted widely with such varied organizations as: the Commission of the European Communities (the "Common Market"), Motorola, France's P.T.& T., the governments of Canada and the Province of Ontario, A.T. & T., Nortel and the Rome Air Development Center.

We've all heard the expression: "build a better mousetrap and the world will beat a path to your door." But what is the reality? What's missing here?

Engineering and business are often an uneasy mix, and all too frequently there is a gap in understanding between these two camps. The cost of not bridging that gap can be great, and a number of examples will be detailed to emphasize this point.

Suggestions will be made on how to build an appropriate bridge. These will cover both organizational and personal levels, noting that there are a variety of ways the bridge can be built and that the issue posed does not have a simple answer.

WEDNESDAY OCTOBER 20

Cochlear Implants for Profound Hearing Loss – Signal Processing Considerations

Speaker: Dr. Bernhard Seeber, University of Technology Munich
Time and Place: Dinner (no-host) 6:15pm in the Stanford Hospital Cafeteria, Meeting at 7:30-8:30pm in room M114 of the Medical School
RSVP: none required
Web & Map: www.ewh.ieee.org/r6/scv/embs/

Bernhard Seeber obtained his diploma (MA) in Electrical Engineering and Information Technology from the University of Technology Munich, Germany in 1999. His diploma thesis focused on the masking effect in Psychoacoustics. In 1997 he worked with Rich Cox and Jont Allen at AT&T Labs Research (former Bell Labs) on the simulation of masking and loudness using a numerical model of the cochlea. From 1995 to 2002 he led his own company for sales and consulting in musical electronics and computer technology. In 2003 he received his Ph.D. in acoustics and psychoacoustics from the University of Technology Munich. He developed a new method for auditory localization studies. Using this method he showed that localization is possible with bilateral cochlear implants and for patients with a cochlear implant in one ear and a hearing aid in the other.

Dr. Seeber received several awards and grants for his work including a three year research funding from the Deutsche Forschungsgemeinschaft, two poster awards at the meetings of the German Acoustical Society in 2001 and 2003, and a young scientists conference attendance award from the International Commission for Acoustics in 2004.

In recent years cochlear implants developed into the most successful sensory prosthesis. Cochlear implants replace the function of the inner ear, the cochlea, by direct electrical stimulation of the auditory nerve with a signal derived from the acoustical information. Early cochlear implants transformed the sound signal into an analog electrical signal for stimulation at one electrode. Recent models process the acoustical information infrequency bands and stimulate at multiple electrodes using current pulses.

A brief overview of the auditory system will be given in the beginning of the talk. In the main part the talk will focus on signal processing in cochlear implants from early models to current multichannel implants and its impact on speech perception and sound quality. Acoustical demonstrations of cochlear implant simulations will illustrate this development. Current approaches and problems for an improvement of the perceptual quality of cochlear implants will be highlighted. If time permits the view will be extended to the processing and perception of binaural, directional information with cochlear implants.

WEDNESDAY OCTOBER 20

Technical Issues and Practical Applications of Transient Voltage Surge Suppression (TVSS)

Speaker: Richard E. Draper, P.E. Danaher Power Solutions
Time: Dinner 6:00 PM, Presentation 7:00 PM
Place: Ramada Inn, 1217 Wildwood Ave (Fwy 101 frontage road, between Lawrence Expressway and Great America Parkway), Sunnyvale
Cost: $22.00 IEEE members, $25.00 nonmembers, and $10.00 students
RSVP: Randal Kaufman, (650) 464-5170, rkaufman@powersmiths.com
Web: www.e-grid.net/docs/0410-scv-pesias.pdf

Our speaker is **Richard Draper** who graduated from North Carolina State University with a BSEE. As an electrical design engineer he worked for Newport News Shipbuilding and Dry Dock Company and CRS Sirrine Engineers, a consulting firm in Greenville, South Carolina. In 1993 he founded Ideas In Motion, a firm providing computer animation for the video industry and forensic profession. He has also worked for Current Technology, Inc. and Powersmiths Corporation as Manager of Applications Engineering and Training. Currently, Mr. Draper resides in Richmond, Virginia providing applications support to Danaher Power Solutions, Inc. in the areas of TVSS, digital static transfer switches, UPS's, and custom PDU's.

Protection from transients and high surges is vital to any major facility. Benefits include prevention of production or data loss, reductions in service and maintenance costs, extended equipment life and increased reliability. Join us for a review of TVSS applications for electrical surge suppression. The following topics will be covered.

Transient Voltage Surges in Electrical Distribution Systems
- a. Basic Definitions & How Surges Enter the Electrical System
- b. Protecting Sensitive Loads From Surges

The Importance of TVSS Standards and Testing
- a. Standards Overview
- b. ANSI/IEEE C62, NEMA LS1, UL1449 2nd Edition, NEC 2002
- c. Independent Testing of TVSS

TVSS Design Considerations
- a. Overcurrent Protection for TVSS
- b. Lead Length
- c. Internal vs. External to Switchgear

Monitoring and Field Testing
- a. Basic Monitoring Features in TVSS
- b. Startup Testing
  - • Validation of Voltage and Configuration
  - • Validation of Xo Bond
  - • Proper Installation
- c. Periodic Retesting

SCV Solid State Circuits

THURSDAY OCTOBER 21

Power-Performance Optimization Methods for Digital Circuits

Speaker:	Radu Zlatanovici, Ph.D. candidate, UC-Berkeley
Time:	6:30 PM refreshments, 7 PM Presentation
Place:	Cadence Building 5, 2655 Seely Ave, San Jose (map on website)
Cost:	none (donation for pizza)
RSVP:	call 408 894-2646 (leave a message) or by email to ssc_scv_rsvp@yahoogroups.com
Web:	www.ewh.ieee.org/r6/scv/ssc/

Most of today's designs are power-limited, yet performance is what ultimately sells products. Thus, it is interesting from a design standpoint to know how power and performance trade each other for digital circuits. The traditional way of designing digital circuits is to optimize for the best performance. Such an approach is not always appropriate in deep submicron technologies because targeting the ultimate performance usually results in prohibitive power consumption. It is therefore worthwhile to investigate how to reduce the power of a circuit without reducing its performance and, if still exceeding the power budget, how to further reduce the power with minimum performance penalty. In other words, it is worthwhile to investigate the optimal power - performance tradeoff curves of the circuits in order to make the best design decisions. Generating such optimal power-performance tradeoffs is a very broad problem due to the different definitions of "performance" at the different levels of the design. For a microprocessor, "performance" can mean "benchmark scores" at application level, "instructions per second" at architecture level, "cycle time" at micro-architecture (pipeline) level and "delay" at (combinational) circuit level. This talk discusses a methodology to generate power - performance tradeoffs at circuit and micro-architecture level. The design problem is formulated as an optimization problem, which is then solved using a mathematical optimizer. At circuit level the tool optimizes combinational circuits in the energy per transition - delay space. It computes the minimum achievable delay under maximum energy and correct operation constraints, by sizing the gates in the circuit. As an example, the tool is used to investigate energy-delay tradeoffs for 64-bit carry-lookahead adders, a very frequent critical path block and hotspot in high performance microprocessors. Conclusions are drawn about the optimal adder design in a given technology. The impact of additional design variables such as supply and threshold voltages is also discussed. At the next level of abstraction, (micro-architecture level) the tool optimizes pipelined circuits in the energy - cycle time space. It computes the minimum achievable cycle time under maximum energy and timing closure constraints. This version of the tool is still under development and it will be demonstrated on an IEEE-compliant Floating Point Unit (FPU). The presented optimization framework allows the designer to treat circuits' power and performance not as two separate notions, but as the two sides of the same coin. The flow can then be used to explore the connection between the two sides, the optimal power - performance tradeoff curve.

Radu Zlatanovici received his B.S and M.S. degrees from Politehnica University Bucharest, Romania in 1999 and 2000 respectively. In 2000 he joined the University of California at Berkeley where he received an M.S. degree in 2002. He is currently working towards his PhD degree at the same university. In 1997 and 1998 he was a summer undergraduate researcher at the Institute of Microelectronic Systems of the Darmstadt University of Technology, Darmstad, Germany working on hierarchical macromodeling of analog circuits. He worked as an analog circuit designer at Semiconix Design, Bucharest, Romania from 1997 to 1999. He was on the faculty of Politehnica University Bucharest from 1999 to 2000. In 2002 and 2003 he interned at IBM T.J. Watson Research Center, Yorktown Heights, NY working on power - performance tradeoffs for pipelined digital circuits. He was a recipient of the Romanian Department of Education Excellence Fellowship in 1997-1999 and of the MobilRom Excellence Fellowship in 1998. He won the first prize at the Romanian National Design Contest for Analog Circuits in 1997,1998 and 1999. His current research interests include high-speed and low-power arithmetic circuits, design optimization in the power - performance space and the impact of novel devices such as FinFETs on the design of digital circuits.

TUESDAY OCTOBER 26

Overview of IEEE Standard 1100-1999 –

Recommended Practice for Powering and Grounding Electronic Equipment (Emerald Book)

Speaker: Robert Schuerger, P.E., Senior Associate, EYP Mission Critical Facilities, Inc.
Time: 5:30 pm (Attitude Adjustment), 6:00 pm (Meeting), 7:00 pm (Dinner)
Place: Sinbad's Restaurant, Pier 2 Embarcadero St., San Francisco
Cost: $25 (at door)
RSVP: preregister by email to qualify for drawing. Call Sonny Siu, 415-901.4318 (leave a message) or by email to ssiu@eypmcf.com

This presentation will be an overview of the book, explaining how it is organized and presenting highlights from each of the chapters. Special emphasis will be given to Chapters 4 Fundamentals," and Chapter 8 "Recommended design/installation practices," in order to provide systematic coverage of power quality as it relates to electronic equipment in electrical distribution systems. The latest edition of the Emerald Book is in the balloting process, and a discussion of what has been added, along with some of the material will be included.

Robert Schuerger is a registered Professional Engineer and has over twenty-five years of experience in power engineering, specializing in electrical testing and maintenance, power quality and on-site engineering support of critical facilities. He was one of the founding members and has twice served as president of the Arizona Power Quality Association, and is a Senior Member of the IEEE. He is the Chapter 4 Chairman of the Working Group to revise IEEE Standard 1100-1999 (Emerald Book) and Chairman of Chapters 5 and 6 for Working Group to revise IEEE Standard 902-1998 (Yellow Book).

SCV Women In Engineering

WEDNESDAY OCTOBER 27

Panel Discussion for Women Engineers:

How to Balance Career Goals and Time for a Family

Panelists: Neha Choksi, Maria de Graaf, Dr. Leslie Field, Roxsana Hadjizadeh, Charan Langton, Dr. Wendy Wong
Time: The discussion starts at 7:00PM. Join us at 6:30PM for social and refreshments
Cost: Free
Place: Dragon's Den of Cogswell Polytechnical College, 1175 Bordeaux Drive, Sunnyvale, CA
RSVP: daisy_cheng@ieee.org
Web link: http://www.ewh.ieee.org/r6/scv/wie/

Neha Choksi took almost two years off to be with her child full time but is now back part time in the consulting world. Her engineering background includes semiconductor device physics, sensor design, and nanoscale manufacturing. She has worked in several start-up environments, consulted for McKinsey and Company, and has worked as an independent contractor. Neha earned a MSEE from Stanford University and a B.S. from Vanderbilt University in electrical engineering and math. She volunteers for the Program Committee of the IEEE-SCV Women in Engineering.

Maria de Graaf is the president of Silicon Valley International.

Dr. Leslie Field started MEMS Insight, a technical consulting company in 2002. Prior to that, Leslie worked in Micro Electro-Mechanical Systems (MEMS) R&D at HP Labs/Agilent Labs for ten years, playing a key role in starting HP Labs' Micromechanics group. At Chevron Research Company, her work resulted in improved commercial refining methods for various petroleum-based products. Leslie obtained her PhD in electrical engineering from U.C. Berkeley's Sensor & Actuator Center in 1991. Leslie earned BS and MS degrees in Chemical Engineering from MIT.

Gain insight from successful women engineers on how to maintain one's technical skills and further contribute to the field without sacrificing the opportunity to have a family. Audience members will be invited to ask questions of the panelists and share their own ideas.

Roxsana Hadjizadeh has 21 years of experience in NPI/Manufacturing Engineering. During her career, she has worked with semiconductors, computer peripherals, network computers, and networking equipment for such companies as GENUS Inc., Network Computing Devices, and WinCom Systems. Most recently, she was the Director of Operations/Mfg Engineering/Quality at Quantum3D, Inc. Roxsana earned her BSEE and MSEE degrees from S. Illinois University, Carbondale. She is a Senior Member of the IEEE and was one of the original founders of IEEE-SCV Women in Engineering, now serving as the 2004 Chair. She is also currently looking for a job and may be contacted at roxsana@ieee.org.

Charan Langton is the manager of the analysis and simulation group at Space Systems Loral. She has more than 30 years of engineering experience both with large corporations and as an independent consultant. Charan earned a BSEE from Cal-Poly San Luis Obispo and now serves on the Industrial Advisory Board to Cal-Poly San Luis Obispo Engineering School, Aerospace Engineering Department. She holds MSEE and MBA degrees from the University of Southern California. Charan has also co-authored a book on how to teach children to read.

Dr. Wendy Wong is currently working for Intel as a senior system engineer. She graduated from Cornell in 1996 with a PhD in electrical engineering. Wendy is a former Program Chair of IEEE-SCV Women in Engineering.

SCV Reliability

WEDNESDAY OCTOBER 27

Reliability Horror Stories

Speaker: Jurek Zarzycki, Ops A La Carte, AND the audience!
Time: 6:30 PM for refreshments, 7:00 PM for presentation
Place: HP-Cupertino Oak Room, Bldg 48. Just North of Hwy 280 (Wolfe Rd Exit) at the corner of Pruneridge Ave. and Wolfe Rd.
Cost: none
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/rs/

If you liked the Exorcist (1, 2 or 3), you will **love** this presentation! Jurek Zarzycki will describe some of the truly ghoulish reliability horror stories he has experienced during his career at Apple and elsewhere. Then, it's audience participation time! Each participant gets 5 minutes to present their own horror stories. We will have the audience vote on the most horrific stories and award prizes. Bonus points for coming in costume. If you have a scary story you would like to share (names can be changed to protect the guilty), please RSVP by sending e-mail to **reliability@ieee.org** to make sure we have sufficient time for everyone. Drop-in participants are welcome.

Jurek Zarzycki has over 25 years of experience as a reliability engineer and quality engineer with various high tech companies, including Tektronix, Varian, Diasonics, Radionics and the last 17 years with Apple Computer. He has extensive experience in high technology products and overseas quality/reliability assurance. He was trained as a design engineer in the Nuclear Technical School (Poland) and is a certified Reliability Engineer (CRE) and Quality Engineer (CQE) by the American Society for Quality and is an instructor in the areas of reliability and quality engineering.

SCV Engineering Management

WEDNESDAY OCTOBER 27

Panel Presentation: Startups that Survived the Bust: The Silicon Valley Spirit

Presenters: Announced on the Website
Time: Introductions and panelists' premises and theories for discussion at 6:00pm, Dinner at 7:00pm, after-dinner presentations at 7:45pm
Place: PRIME HOTEL Sunnyvale (Former Wyndham) 1300 Chesapeake Terrace, Sunnyvale - off Lawrence Expressway/ Caribbean Drive at Hwy 237
Reservations: through Website, below
Cost: (with reservations by Friday before meeting) $25 (IEEE member), $30 (non member), $5 surcharge thereafter. (Cash or check at the door). Student IEEE members - $5.
For other information leave message with Rich Hendrickson at (408) 203-3462.
Web: www.ieee-scv-ems.org/

The SCV Engineering Management Society presents a before-and-after dinner panel presentation on engineering management in the fast, then slow, now picking-up-speed lane. Following topic introductions, then discussions and networking at a sit-down dinner, the panelists will provide their perspectives and field round-robin questions that revolve around your interests.

Silicon Valley startups blossomed during the boom of the late 1990's when the potential of broadband and wireless access seemed limitless and the internet was growing at a phenomenal rate. The New Economy was driven in internet time by the need for new hardware, new software, and new systems to gain advantage and agility in what seemed to be an ever growing market. Then the dot-com bubble burst and the New Economy imploded. A few companies survived. What was unique about the survivors that allowed them to rise from the ashes, prosper, and flourish? A panel of senior managers from technology companies that started up during the boom times of the late '90's and survived the bust will describe and discuss what makes their companies unique and their business models robust.

The EMS website features the final selection of speakers; or check the on-line IEEE GRID calendar for panelist information. Come October 27th and find out where you can fit into the evolution.

THURSDAY OCTOBER 28

The Nanotechnology Frontier: Applications of Nano to Materials and Packaging

Speaker: Dr. Anthony Laviano, Managing Director, NANOWorld
Time: Noon – Lunch served 11:45-12:15, presentation at 12:15
Cost: $15 for lunch ($20 at the door)
Place: Ramada Inn, 1217 Wildwood Ave (Fwy 101 frontage road, between Lawrence Expressway and Great America Parkway), Sunnyvale
RSVP: to John Jackson, Analog Devices john.jackson@analog.com
Web & Map: www.cpmt.org/scv

In today's world, "Packaging Engineering" is a discipline of designing IC and MEMS platforms and electronic circuits at the mircoscale. The integrated circuit is so well established and common that many of us have given it little thought -- until now, with the advent of Nanotechnology. My vision is to bring an attitude of engagement between the Engineer and Nanotechnology. Therefore, I shall define Nanotechnology, answering the question, "Is it real?" After exposing its benchmark, I compare the technology readiness level and introduce achievements to date. Then, more importantly, we will examine why only the Engineer can grow the Nanotechnology Frontier into an Industry.

Dr. Anthony F. Laviano is Managing Director and founder of NANOWorld, a nanotechnology education service, and founder of ADTEKT, an engineering management service for Advanced Technologies. He was formally a Program Manager for Advanced Technical Programs and a member of the Patent Committee for Raytheon Space and Airborne Systems and established the Nano Engineering and Science Technology Interest Group (NEST) and the Power Electronics Technology Interest Group (PET). His focus is Advanced Technologies and Products for ground, air and space, and dual-use applications, that is, identifying, organizing, and transitioning technology into military and commercial applications. Dr. Laviano is the past Chairman of the IEEE Power Electronics Society for Southern California, a member of IEEE Standards Association, the IEEE Los Angeles Council, the Academy of Management, the Los Angeles Regional Technology Alliance (LARTA) Nanotechnology Working Group, the Journal of Public Administration Editorial Board, the Northrop Rice Aviation Institute of Technology Advisory Board, and a former member of the National Faculty of Nova Southeastern University Graduate School of Business and Hughes General Motors Technology Staff. Dr. Laviano has lectured both in the United States and United Kingdom on the subject of "Growing Nano Engineers to Apply and Use Nanotechnology" and serves on the U.S. National Academy of Sciences, National Research Council Nanotechnology Committee.

WEDNESDAY NOVEMBER 10

Packaging Challenges in Micro-Optical Electromechanical Systems Components: the DMD™ as a Case Study

Speaker: Dr. Richard Gale, Texas Tech University
Time: Seated dinner at 6:30 ($25 if reserved before Nov 6; $30 after & at door; vegetarian available)
Place: Ramada Inn, 1217 Wildwood Ave (Fwy 101 frontage road, between Lawrence Expressway and Great America Parkway), Sunnyvale
RSVP: to Allen Earman, allen.m.earman@intel.com
Web & Map: www.cpmt.org/scv

It is commonly held that packaging for MEMS components can run to 60-80% of unit cost. This is due to a number of factors including "hard-to-handle" and "hard-to-hold" problems as well as generally low volumes. When optical performance is added to the mix cost, complexity, and reliability all move in unfavorable directions. The digital micromirror device (DMD™) made by Texas Instruments has become a successful product in spite of these challenges. An optical quality window must be incorporated into the package to allow light modulation. Since the display is an image of the face of the device, the package must be cosmetically pleasing as well as optically functional. In digital cinema applications as much as 80 Watts in the visible spectrum impacts the device and parts of the package so that thermal management is also critical. High definition video bandwidth at ever-increasing bit depths places extreme demands on impedance control and/or pin count. Finally, the mechanical contact which makes possible acceptable pixel uniformity requires surface chemistry control on the monolayer or nanometer scale. Some of these special requirements and attempts at their solutions are discussed in this presentation.

Prof. Richard Gale is in the Electrical and Computer Engineering department at Texas Tech University. He held the position of Distinguished Member, Technical Staff, and was responsible for coordinating the work of the New Applications Research and Development Group in the Technology Development section of Digital Imaging at Texas Instrument Incorporated until retirement in April, 2001. Dr. Gale holds the A.B. degree in Physics from the University of California at Berkeley (1976), and M.S. and Ph. D. degrees from Lehigh University (1979 and 1984, respectively). Dr. Gale joined the Central Research Laboratories at Texas Instruments in 1984 to apply his graduate work on electron traps in silicon dioxide to charged-coupled device imagers for space-borne applications. He moved from CCD's to more general photonics interests in 1985, in time to make several key contributions in the developing MEMS spatial light modulators at TI. He was a member of the team taking the Digital Micromirror Device (DMD™) from research into a corporate venture projects activity in 1991 after successfully managing parts of the initial customer interactions in projection displays. He contributed to the development of Corporate Venturing at Texas Instruments, and managed the demonstration/validation activity in the early stages of Digital Imaging at TI.

After successfully promoting the technology internally and externally through a period of explosive growth, he took a position in Production Engineering for the development of first generation portable projectors. His final position included responsibility for novel approaches and new technologies utilizing and enabling Digital Light Processing (tm) insertion points,

providing strategic direction in understanding competitive assessment and intelligence, and coordinating the DLP™ Products Coop programs and technical publication management. Dr. Gale is an author of more than a dozen technical publications, and holds patents in MEMS design, processing, packaging, control circuits, and system utilization concepts.

Dr. Gale is currently pursuing new career directions that will build on and expand his experience in microelectromechanical systems, novel data analysis techniques, information creation and distribution systems, and communications technologies. He accepted a tenured Professorship in the Electrical and Computer Engineering Department at Texas Tech University in Lubbock, TX, that began 1 June, 2002.

Avocational interests include observational astronomy, home theater design, and digital photography.

SCV Solid State Circuits

THURSDAY NOVEMBER 18

Oversampling A/D and D/A Converters

Speaker: Prof. Bruce Wooley, Stanford University, IEEE Fellow
Time: 6:30PM Social, 7:00PM Presentation (no cost)
Place: Cadence Design Systems, Bldg. 5, 2655 Seely Ave., San Jose
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/ssc/

CONFERENCE CALENDAR

Oct 4-7: **SECON'04: IEEE Int'l Conf on Sensor and Ad Hoc Communications and Networks**

Held at the Santa Clara Marriott, SECON addresses the new generation of inexpensive mobile devices, sensors and actuators, and a broad range of applications.

See our **GRID display page** for more details, or visit

www.e-grid.net/conf/secon.html

Oct 7-8: **LEOS Workshop: SBIR Grants for the Curious Engineer in Business**

The US government and other domestic agencies provide funding for projects and assistance for R&D to small businesses under the Small Business Innovative Research (SBIR) program. Funds from tens to hundreds of thousands of dollars are available for work on topics ranging from nanotechnology to astronomy.

This workshop is for engineers, entrepreneurs, and small-business executives who wish to learn how to "read between the lines" of government solicitations and how to win grants and contracts. This two-day Workshop will be held in Sunnyvale, at the National Semiconductor Credit Union meeting rooms.

More details: www.ieee.org/sbir/

Oct 16: **Congestion Management Workshop**

This course provides a detailed description of various aspects of congestion management in power system operations. A primer is followed by market design basics as envisioned by the FERC approach, then the California market is covered. Finally, there is an overview of current state-of-the-art software tools and technologies and software demonstrations.

8AM – 5PM at San Francisco State University.

Visit

www.ewh.ieee.org/r6/san_francisco/sfpes.htm

Oct 18-21: **Integrated Reliability Workshop focuses on Semiconductor Reliability**

IRW'04 provides a unique environment for envisioning, developing, and sharing reliability technology for present and future semiconductor applications. All Workshop activities take place in a relaxed and rustic setting – the Stanford Sierra Camp – that promotes an atmosphere of interactive learning.

See our **GRID display page** for more details, or visit

www.e-grid.net/conf/irw.html

Oct 25-29: **BroadNets 2004 covers Broadband Networking in San José**

The IEEE Communications Society's first International Conference on Broadband Networks will be held locally at the end of October, with its focus on broadband networking for the entire gamut of next-generation networks – all the way from access networks (xDSL, Cable, EPON, Broadband Wireless, multi-Gigabit uplinks), to regional and metropolitan networks to wide-area core networks.

Visit the website: **www.e-grid.net/conf/broadnets.html**

Oct 5: **IEEE Short Course: "Mandated Pb-Free Solder Assemblies: Exploring the Transition's Impact on Product Reliability" -** in Cupertino

As governments in Europe and Asia begin the phase-in of their "Removal of Hazardous Substances" regulations, electronics designers and manufacturers are in the final stages of changing from classic tin-lead solders to various compositions of Pb-free solders. The new solders present us with considerable uncertainty. Will our computers, wireless devices, and other products show considerably lower reliability over the next few years? What are the risks for which we must be planning?

The focus in this special one-day event is on the technical engineering impact of the transition. What do we know, what do we not know, and where are the remaining significant risks?

More information: **www.cpmt.org/scv/**

The **CONFERENCE CALENDAR** is a service to our IEEE Members. It outlines upcoming IEEE workshops and conferences in the Bay Area. Please submit items to the GRID Editor: editor@e-grid.net.

Conferences are also encouraged to purchase display space in the **GRID.pdf** and publicize their events on our website and in our **e-GRID** email notification service. For the Conference Publicity flyer, please download:

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