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OMNIBUS SPECIFICATION (Preliminary)

Contents:

1. Scope

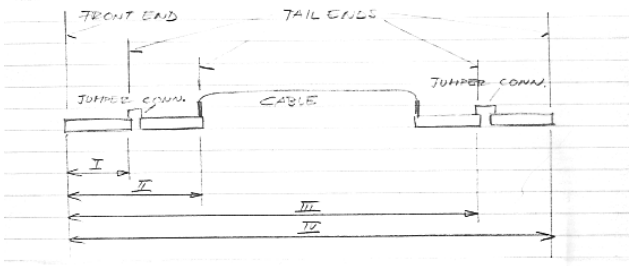
Chapter 9 of the "PDP8/E Small Computer Handbook 1971" provides a fairly extensive description of all the aspects of the OMNIBUS. The paragraphs "Bus Specifications, Loading Rules, and Electrical Considerations of Driving a Line" provide some basic information of the electrical characteristics of the OMNIBUS. However, a detailed description of these properties would be beyond the scope of the Small Computer Handbook.

It is the purpose of this specification to provide a detailed description of the electrical characteristic of the OMNIBUS. It is most important for designers dealing with the OMNIBUS to become familiar with all the aspects and peculiarities of the OMNIBUS.

2. General Electrical Characteristic

2.1 The Various Length of the OMNIBUS

Various system configurations call for four different lengths of the OMNIBUS as indicated by the sketch below. Most of the electrical characteristics of the bus change accordingly. Any standard piece of hardware shall be designed, so it will operate properly under worst case conditions in any length bus. Acceptance criterias of hardware have to be based on any length bus, too.



2.2 Mechanical and Electrical Properties

	Length (inch)	Prop. Delaytime Typ. (ns)	Capacitance to Gnd. Typ. (pF)
OMNIBUS I	10	6	70
" II	23	12	140
" III	71	24	530
" IV	84	30	600

Characteristic impedance Z_o: 100 ohm typ.

3. The Various Groups of Signal Lines

Different functions on an OMNIBUS line call for different electrical characteristics of drivers, receivers, terminators, etc. The electrical characteristic can be best described by breaking down the 96 signal lines into seven distinct groups (refer also to "Bus Load" schematic E-CS-M832Ø-Ø-1).

3.1 Group Definition

3.1.1 Group #1: Signal lines for open collector drivers.

List:

MDØØ ... MD11	INT RQST
MEM START	SKIP
LINK	LINK DATA
BRK IN PROG	IND 1
OVERFLOW	IND 2
LD ADD ENABLE	INTERNAL I/O
MA, MS LOAD CONT	NOT LAST XFER
BREAK DATA CONT	F SET
BREAK CYCLE	STOP
RES Ø	KEY CONTROL
RES 1	SW
CØ	IRØ
C1	IR1
C2	IR2
	CPMA DISABLE
	USER MODE

3.1.2 Group #2: Signal lines for open collector drivers and fast speed up during TP2 or TP4 respectively.

List:

MAØØ ... MA11	Speed up at TP4
EMAØ	
EMA1	
EMA2	
ROM ADDRESS	
MS IR DISABLE	
F	
D	
E	
MD DIR	Speed up at TP2

3.1.3 Group #3: Signal lines for open collector drivers and slow speed up during INT STROBE.

List:
- DATA ØØ ... DATA 11
- INT IN PROGRESS

3.1.4 Group #4: Memory timing & control signal lines.

List:
- RETURN
- SOURCE
- STROBE
- WRITE
- INHIBIT

3.1.5 Group #5: General timing signal lines terminated at one end.

List:
- TP1 ... TP4
- TS1 ... TS4
- INT STROBE
- I/O PAUSE (not a timing signal by definition, however the loading conditions are similar as for timing signals).

3.1.6 Group #6: General timing signal lines terminated at both ends.

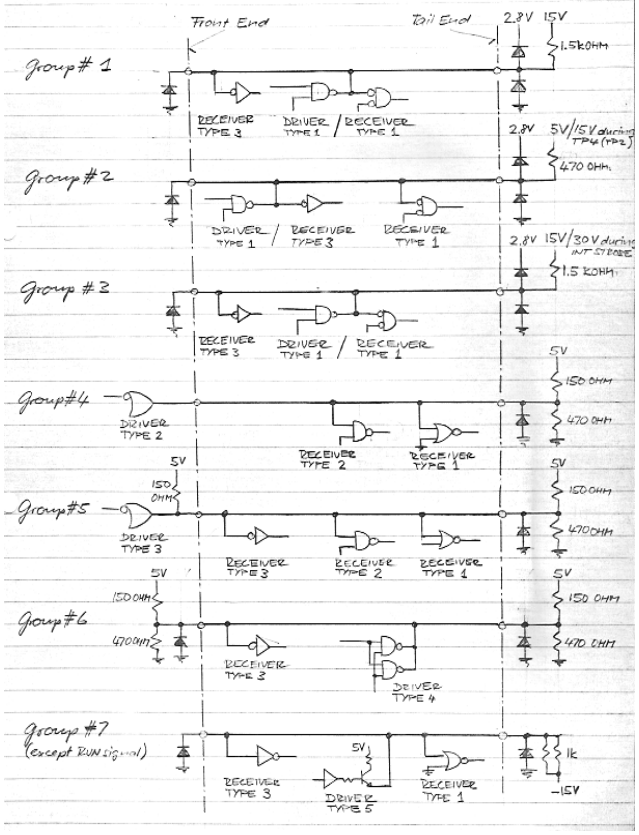
List:
- LINK LOAD
- BUS STROBE

3.1.7 Group #7: Miscellaneous

List:
- RUN (special treatment necessary because of power on/off peculiarities)
- POWER OK
- INITIALIZE
- LOAD ADDRESS

(low state has to be guaranteed with no power)

3.2 Line Characteristics



3.3 Terminators and Pull-Up Resistors

3.3.1 Section 3.2 reflects the hardware used for terminators and pull-up resistors of the various groups of lines. Each group has its own tailored set of clamp diodes terminator resistors, pull-up resistors according to driving capability, thresholds of receivers, proper line termination, time skew, speed of open collector driver lines, power consumption.

3.3.2 Front End: Termination hardware on the front end is located on any of the following three modules: Timing Generator M8330, Major Register Control M8310 or Major Register M8300. Most of the clamp diodes required are contained in IC gates. Note that all these boards have to be installed at the front end of the Omnibus (refer to Bus Priority List A-SP-PDP8/E-Ø-4).

3.3.3 Tail End: All the required termination hardware for the tail end is contained on the Bus Load board M8320. Note that this board has to be installed always in the last slot of the OMNIBUS for any given bus length or system configuration.

3.4 Drivers and Driving Capability

3.4.1 Driver Types:

Driver Type	Location on Omnibus	Group Used	Circuit Used	Notes
1	Anywhere	1	DEC 8881 DEC 97401 DEC 8235	
		2	DEC 8881	
		3	DEC 8881 DEC 97401 DEC 8235	
2	Front end only	4	DEC 74H40 DEC 7440	
3	Front end only	5	DEC 74H40	
4	Anywhere	6	DEC 8881	2 Circuits in parallel
5	Anywhere	7	DEC 3009	Emitter follower pull-up

3.4.2 Driving Capability (Operating range 0°C to 55°C)

Circuit	Driving Capability / Low State	Leakage Respect. High State	Notes
DEC 8881	16 mA at 0.4V 50 mA at 0.8V	-25 uA at 3.5V	
DEC 97401	16 mA at 0.4V	-25 uA at 5.5V	
DEC 8235	16 mA at 0.4V	-25 uA at 3.5V	
DEC 7440	48 mA at 0.4V	-1.2 mA at 2.4V	
DEC 74H40	60mA at 0.4V	-1.5 mA at 2.4V	
DEC 3009		-40 mA at 3.5V	

3.5 Receivers and Loading Characteristic

3.5.1 Receiver Types

Receiver Type	Locations on OMNIBUS	Group Used	Circuit Used	Notes
1	Anywhere	1,3,5,7	DEC 314, 6314, 5314, 7314 DEC 380, 6380, 5380, 7380 DEC 384, 5384, 7384	
		2,4	DEC 314, 6314 DEC 380, 6380 DEC 384	
2	Anywhere	4,5	Any of the DEC 74XX or DEC 74HXX Series circuits with 2-input-minimum positive AND or NAND gate.	
3	Front end only	1,2,3,5 6,7	Any of the DEC 74XX, DEC 74HXX or DEC 74LXX series circuits.	This type is not standard, refer to 3.5.3 for more details.

Receiver Type 1: This type receiver, which is equivalent or similar to the UTILOGIC 300 series gates, is the only type receiver necessary for standard OMNIBUS interfacing. For economical and part procurement reasons up to four different circuits with the same logic function are in use. The proper selection of the circuit is reflected in the above table, and the specific deviations are shown in 3.5.2.

Receiver Type 2: This type receiver, which is equivalent to any standard TTL 74XX or 74HXX series 2-input-minimum positive AND or NAND gate, is used for timing signals in the memory, memory options and some other internal options. The use of this type receiver is not allowed in standard interfacing techniques unless so specified.

Receiver Type 3: This receiver type, which is equivalent to any standard TTL 74XX, 74HXX or 74LXX series circuit, is used in specific cases in the CPU and in certain internal options. The use of this type receiver is not allowed in standard interfacing techniques, since heavier loading and smaller noise margins require special consideration.

3.5.2 Loading Characteristic & Switching Speed
(Operating range 0°C to 55°C)

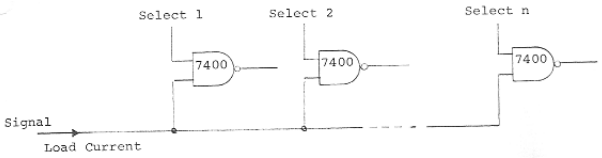
Circuit	Input Loading Characteristic		Propagation Delay (ns)* Input High Going		Input Low Going	
	Low State	High State	Min.	Max.	Min.	Max.
DEC 314	-25μA at 1.3V	160uA at 2.5V	10	35	10	45
DEC5314		160uA at 2.7V	0	35	0	45
DEC6314			10	35	10	45
DEC7314			0	36	0	18
DEC 380	-25μA at 1.3V	160uA at 2.5V	10	35	10	45
DEC5380		160uA at 2.7V	0	35	0	45
DEC6380			10	35	10	45
DEC7380			0	36	0	18
DEC 384	-25μA at 1.3V	160uA at 2.7V	10	45	10	35
DEC5384			0	45	0	35
DEC7384			0	26	0	20
DEC 74 ...	-1.6mA at 0.4V	40uA at 2.4V	0	15	0	29
DEC 74H...	-2.0mA at 0.4V	50uA at 2.4V	0	10	0	10
DEC 74L...	-0.18mA at 0.3V	10uA at 2.4V	0	60	0	60

*For the indicated propagation delay the capacitive load at the output is 15 pF on all circuits except the DEC 74HXX (25 pF) and the DEC 74LXX (50 pF).

3.5.3 Load Relief Technique

The essence of this technique is that the option, device or field select network provides the "hold off" current for a receiver to relieve bus loading. This technique is commonly used in OMNIBUS interfacing.

Example 1

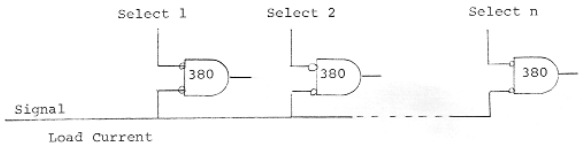


Assumption: The circuits have multi-emitter inputs.
Only one SELECT line is enabled at one time.

Resulting Load Current: SIGNAL LOW → -1.6 mA at 0.4V
└nominal load per gate input

SIGNAL HIGH → n * 40 uA at 2.4V
└nominal leakage per gate input
└number of gates

Example 2:



Assumption: The circuits have multi-emitter follower inputs.
Only one SELECT line is enabled at one time.

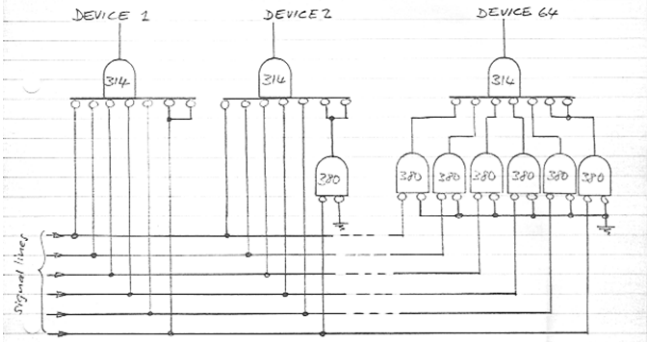
Resulting Load Current: SIGNAL HIGH → 160 µA at 2.7V
└ nominal load per gate input

SIGNAL LOW → n * (-25 µA) at 1.3V
└ nominal leakage per gate input
└ number of gates

3.5.4 Load Share Technique

This technique is a consequence of certain decoding networks (IOT Decoding), and it is based on the same principle as the Load Relief Technique.

Example:



Load Currents:

Assumption: The circuits have multi-emitter follower inputs.
There is only one decoder per device number.

Resulting Load Current for each of the signal lines:

HIGH STATE → 64* 160 uA * 1/6 * 1/2 + 32 * 160 uA = 5.97 nA at 3.5V
└ nominal load per input
└ max. number of inverters per line
└ signifies inverters for half of the decoder inputs
└ 1/number of inputs per decoder
└ nominal load per input
└ max. number of decoders per line

LOW STATE → 64* (-25 µA) at 1.3V
└ nominal leakage per gate input
└ max. number of decoders per line

3.6 Noise Margins

The following table shows the guaranteed DC noise margins of all the used combinations of drivers and receivers for the operating range 0°C to 55°C.

Driver Type \ Receiver Type	Logic State	1	2	3
1	High Low	0.8V 1.0V	——	1.5V 0.4V
2	High Low	0.8V 1.0V	1.5V 0.4V	——
3	High Low	1.3V 1.0V	2.0V 0.4V	2.0V 0.4V
4	High Low	——	——	1.5V 0.2V
5	High Low	0.8V 2.1V	——	1.5V 1.5V

4. Timing Considerations

4.1 Rise and Fall Times

The rise and fall times are a function of the length of the OMNIBUS and the loading. The rise time of all Open Collector signal lines is particularly dependent on this property.

Definition of Rise Time:

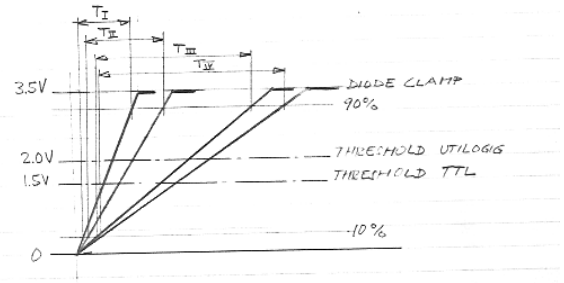


Table:

Group	Typical Rise Time for Various Length OMNIBUS				Notes
	T_I(ns)	T_{II}(ns)	T_{III}(ns)	T_{IV}(ns)	
1	30	50	150	180	
2	10	20	50	60	Fast speed up
3	15	25	75	90	Slow speed up

4.2 Propagation Delay

The propagation delay is a function of the length of the OMNIBUS and the loading. Typical delay times are listed in 2.2. The OMNIBUS PRIORITY LIST (A-SP-PDP8/E-0-4) defines the proper module assignments on the bus in order to avoid conflicts or unnecessary losses of time margins due to "Round Trip" delays. Unless an option fits into one of the listed categories on the Priority List, a careful timing analysis is required and the list has to get updated accordingly.

The maximum time skew between any of the OMNIBUS lines due to different line characteristics is 20 ns for the maximum length OMNIBUS provided none of the loading rules are violated.

Crosstalk

5.1 Crosstalk on OMNIBUS

Crosstalk is an inherent problem to the OMNIBUS. Given the electrostatic and magnetic coupling between edge runs and connector pins and the typical rise and fall times of state of the art circuitry, a significant amount of crosstalk becomes a fact of life.

Solutions which would eliminate the source of such problems are not feasible under the circumstances. Typically the crosstalk is worst for signal lines which are surrounded by a number of simultaneously switching lines. In order to circumvent this problem a number of techniques have been systematically applied in the design of the PDP8/E system.

5.2 Techniques to Avoid Crosstalk Problems

5.2.1 Optimum Noise Margins

The driver-receiver combination with the optimum noise margins are used where ever it is possible (see paragraph 3.6).

5.2.2 Integration

Signal lines carrying register information during the whole machine cycle (MA lines, etc.) are buffered by receivers with a specified minimum propagation delay time. The integrating effect of such gates filters out some of the very fast noise spikes.

5.2.3 Edge Triggered Clocking

Information loaded from the OMNIBUS to any type register is done by means of edge triggering. One reason is to prevent flip-flops from being vulnerable to noise during the duration of clock pulses. Secondly, on bidirectional lines logic conflicts could occur. Typical example:

In an output transfer with Clear the AC, supposedly asserted DATA lines can change state during the clock pulse (TP3), causing wrong information being loaded into non-edge triggered registers.

5.2.4 Skewing

The clocking in the system is done at times where bus lines, adders, logic trees, etc., have settled.

5.2.5 Conditional Enabling

In some cases the enabling of receivers is restricted to certain periods of the machine cycle or to certain events in order to reduce vulnerability to noise.

Example: STROBE and INHIBIT are gated with FIELD and WRITE in a memory system. The MD lines in peripherals are gated with I/O PAUSE.