Chapter Meetings and Events

SCV-CE - 7/26 | **Wireless at Home: Home Infotainment Networking** - impact of internet sharing, entertainment … [more]

SCV-IM - 8/3 | **Contamination Analysis using Surface Analytical Tools** - what is possible, with practical examples ... [more]

SJSU - 8/9 | **DSP System Design** and **Wireless Transmitters** - 4-day classes with labs ... [more]

SCV-EDS - 8/9 | **Organic Photovoltaics: Low-cost, Stable, Non-toxic Solar Cells using Organic Pigments** - the potential to substantially reduce the cost of solar electricity ... [more]

LSS - 8/12 | **BioImage Data Mining, 3D Molecular Structures, BioSPICE** and **Controlling Complexity** - inexpensive 1-day workshops in bio-sciences, held at Stanford ... [more]

SJSU - 8/16 | **FPGA DSP System Design** and **High-Speed Data Networks** - 4-day classes with labs ... [more]

SCV-K-12 - 8/23 | **Noon Planning Meeting: K-12 Age Group Outreach/Programs** - at SVTI in San Jose: more details: ... [more]

SCV-IM - 9/7 | **Introduction to the Stanford Nanofabrication Facility, with Research Examples** - an NSF Center with a variety of semiconductor processing equipment open to external use ... [more]

SCV-CPMT - 9/14 | **Kirkendall Voids in Lead-Free Solder Joints: A Reliability Issue** - effects on the impact and shock strength of solder joints ... [more]

Half-Day Tutorials (Monday Aug 8):

At Computational Systems Bioinformatics at Stanford

– Demonstration Projects in Clinical Informatics – Genome Tiling Microarrays and Gene Interaction Networks – Novel Visualization and Analysis Methods in BioImaging – Computational Methods in MS-based Proteomics – Introduction to the Semantic Web for Bioinformatics – Structure Based Methods for Identifying Protein Function – Pattern Discovery in Sequences and Structures – Statistical Approaches to Analyzing Biological Networks [more]

Half-Day Tutorials (Monday Sept 12):

At Int'l Semiconductor Manufacturing Symposium, San Jose

– Conjoint Design for Manufacturing (DFM) and Advanced Process Control (APC) Strategies for Yield at 65nm and Beyond

– Impact on Mfng of Introducing New Materials in IC Production [more]

Upcoming Conferences in the Bay Area

Aug. 8-11: **Computational Systems Bioinformatics**, Held at Stanford University; cutting edge research
Discount through August 3 [more]

Aug. 15-17: **16th Annual Magnetic Recording Conference**, Held at Stanford University
Early-bird discount through July 18th [more]

Sept 12-15: **Int'l Symposium on Semiconductor Manufacturing** – San Jose Fairmont
– Workshops, Sessions, keynotes, panel [more]

Sept 22-23: **Antenna Systems** and **Short-Range Wireless Conferences**, Held at Santa Clara Marriott
Early-bird discount through August 19th [more]

Professional Skills Courses from EMS, CPMT, ETA:

Transitioning from Individual Contributor to Manager
August 4 at Cypress Semiconductor, San Jose [more]

High Impact Coaching
August 16 at Sybase, Inc, Dublin [more]

Communication & Conflict Management Using MBTI
August 17 at LSI Logic, Milpitas [more]

IEEE GRID

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August 2005 • *Volume 52 • Number 8*

IEEE-SFBAC
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IEEE **GRID** is the monthly newsmagazine of the San Francisco Bay Area Council of the Institute of Electrical and Electronics Engineers, Inc. As a medium for both news and opinion, the editorial objectives of IEEE **GRID** are to inform readers in a timely and objective manner of newsworthy IEEE activities taking place in and around the Bay Area; to publish the official calendar of events; to report on IEEE activities of a national and international scope; and to serve as a forum for comment on areas of concern to the engineering community by publishing contributed articles, invited editorials and letters to the editor.

IEEE GRID is published as the **GRID** Online Edition residing at www.e-GRID.net, and in a handly printable **GRID.pdf** edition, and also as the **e-GRID** sent by email twice each month to more than 24,000 Bay Area members and other professionals.

Editor: Paul Wesling
IEEE **GRID**
12250 Saraglen Dr.
Saratoga CA 95070
Tel: 408 331-0114 / 510 500-0106 /
415 367-7323

Fax: 408 904-6997
Email: editor@e-grid.net
www.e-GRID.net

NOTE: This PDF version of the IEEE GRID – the **GRID.pdf** – is a monthly publication and is issued a few days before the first of the month. It is not updated after that. Please refer to the Online edition and Interactive Calendar for the latest information: **www.e-GRID.net**

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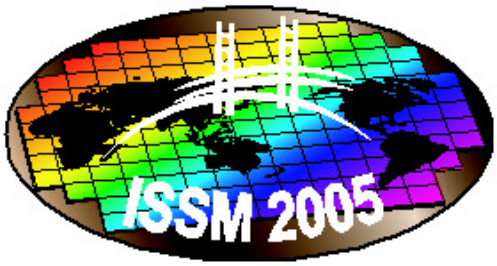
ISSM'05 International Symposium on Semiconductor Manufacturing

- **Fairmont Hotel, San Jose, CA USA**
- **Workshops: Monday, September 12**
- **Sessions: Tuesday – Thursday, September 13-15**



The 14th International Symposium on Semiconductor Manufacturing (ISSM) will be held Tuesday, September 13 through Thursday, September 15 at the San Jose Fairmont Hotel. ISSM is the largest world-wide forum specifically designed for semiconductor device manufacturers and suppliers.

This year's event covers timely and important topics: **– Factory Design – Manufacturing Strategy and Structure – Ultra Clean Technology – Process and Metrology Equipment – Manufacturing Control and Execution – Process Materials Optimization – Environment, Safety & Health – Robust Engineering – Advanced Backend Processing – Process Control and Monitoring – Yield Enhancement – Interactive Poster Session – and more**

Keynote presenters for 2005 include:

- **Peter Chang, Vice Chairman, UMC**
- **Gilles Delfassy, Senior VP of Wireless, TI**
- **Brian Halla, Chairman/CEO, National Semi**
- **Tetsuro Higashi, Chairman/CEO, Tokyo Electron**
- **W.S. Lee, Senior VP of SRAM Flash PA, Samsung**
- **Mike Polcari, Pres/CEO, International Sematech**

Panel: Semiconductors & Semi-Equipment – The Next Opportunity
…debating important issues in our industry.

Two educational workshops will precede the conference on Monday, September 12:

- **Conjoint Design for Manufacturing (DFM) and Advanced Process Control (APC) Strategies for Yield at 65nm and Beyond** (morning)
- **Impact on Manufacturing of Introducing New Materials in IC Production** (afternoon)

Created more than a decade ago by leading corporate executives, ISSM places an emphasis on sharing industrial experiences, technical solutions and opinions on the advancement of manufacturing science. ISSM has developed into one of the most respected and well-attended conferences in the industry. Now celebrating its fourteenth anniversary, ISSM has a stellar conference planned for 2005.

IEEE CPMT IEEE COMPONENTS, PACKAGING AND MANUFACTURING TECHNOLOGY SOCIETY EDS semi

As an international conference, ISSM seeks the best talent from around the world, this year from 77 companies, universities and technical consortia representing 15 countries. Conference presenters include manufacturing professionals, engineers and managers from semiconductor, equipment and materials companies, as well as academic experts from universities and research organizations. Thus, attendees are exposed to the latest technical information.

Recognizing that manufacturing expertise is a cornerstone to corporate success, ISSM places a high priority on relevance, significance and applicability to wafer fabrication. Additionally, plenary presentations provide opportunities for presenting broad visions and outlining key challenges facing the industry.

General information, online conference registration and hotel information is available on the ISSM web site:

www.issm.com

Earlybird Registration through August 1
(save $85 compared to on-site fee)

For assistance, contact Drue Hulmer at ISSM, c/o Maritz Travel Co, 1777 Botelho Dr., Suite 100, Walnut Creek, CA 94596 USA
Phone: 925-287-5221, e-mail **issm2005@maritz.com**

There are numerous parking lots in the area, most with a daily rate of $16. Parking in most public lots and on the street is free after 6:00 pm.

ISSM is sponsored by the IEEE (Electron Devices Society and Components, Packaging and Manufacturing Technology Society), the Society of Applied Physics of Japan (JSAP), and Semiconductor Equipment & Materials International (SEMI).

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The premiere conference focusing on the latest advancements in Antenna Systems and Technology & Short-range Wireless Standards and Technology

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Program (PDF) **Website** CLICK!

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Santa Clara Marriott Hotel

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Keynote Talks:

Small Size Active Controllable Antennas for Mobile Phones,
Anders Thornell-Pers, Centurion Wireless Technologies

Subscriber Based Smart Antenna For Wireless Devices: From Concept to System Integration And Beyond,
Dr. Bing Chiang, Technical Staff Member, InterDigital Corp

RFID Technology: Promises and Challenges
Salil Pradhan, Chief Technology Officer, H-P RFID Prgm

Panel Discussion:
Wireless Technology Market Development & Direction

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IEEE

16th Annual Magnetic Recording Conference

"Heads and Systems"

August 15-17, 2005

Held at Stanford University in Palo Alto
at the Hewlett Teaching Center Auditorium and Stone Pine Plaza

With utmost pleasure we announce this year's 16th annual TMRC. The main topics for the conference are Heads and Systems. This includes Read heads, Write heads, Perpendicular recording heads and systems, Recording systems, Advanced coding/detection, and Reliability/Mechanics.

With areal density growing at roughly 40% per year, key technologies to be presented at this conference include: new generation of advanced GMR, Tunnel MR, CPP GMR, Perpendicular recording heads and systems, novel coding/detection schemes, and head reliability and mechanics – all technologies that will be playing key roles in the near future.

The oral sessions will be held at the Hewlett Teaching Center Auditorium, and Stone Pine Plaza is to be used for Posters and Bierstube. I am sure you will find time to stroll through the pleasant Stanford campus.

Harry Gill, Hitachi Global Storage Technologies
Conference Chairman, TMRC 2005

Details:

- All Oral Sessions: Hewlett Teaching Center Auditorium (Continental Breakfast each day)
- Poster/Bierstube sessions: Stone Pine Plaza
- TMRC Banquet, 6:00-9:00 PM, Clark Center LinX Café
- Banquet Speaker: Dr. Mark Kryder, CTO, Seagate Technologies, "Magnetic Recording at the Crossroads"

PROGRAM

6 sessions with 36 papers, in the following areas:

- Read Heads - Write Heads
- Perpendicular Recording - Recording Systems
- Advanced Coding, Detection, and ECC
- Reliability and Mechanics

Invited speakers from the following companies and universities will present leading work in the magnetic recording area: Alps, Anelva, Fujitsu, Headway, Hitachi, Hutchinson, Matsushita, Maxtor, SAE, Seagate, Sony, TDK, Toshiba, UC Berkeley, CMU, UCSD/CMRR, Harvard

Plus Poster Sessions

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Institute for Information Storage Technology (**IIST**)
Santa Clara University

Center for Micromagnetics & Information Technologies (**MINT**) – University of Minnesota

Center for Materials for Information Technology (**MINT**)
University of Alabama

Center for Research on Information Storage Materials (**CRISM**) – Stanford University

Computer Mechanics Laboratory (**CML**)
University of California, Berkeley

Registration:

Low fees (includes CD-ROM):

- IEEE Member: $325
- Non-Member: $375
- Full-time Student/Life member: $95
- Tuesday evening reception/banquet: $50/person

Parking for Monday – Wednesday:

Free on-campus parking is located at the Galvez Field lot at the corner of Galvez Street and Campus Drive East. The lot is within walking distance of the conference site. From Galvez Street walk to Serra Mall, turn right and walk past the Oval until you arrive to the Hewlett Teaching Center. Disabled parking passes are honored everywhere on campus. Please refer to the maps at the end of the TMRC booklet.

REGISTER TODAY!

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More information on the TMRC website:

tmrc.nanointernational.org

CSB2005 brings you cutting-edge research on biological discovery and innovation through multidisciplinary presentations that can change the world of biology, medicine and drug discovery – and by changing this world, change the lives of the people waiting for cures. **CSB2005** provides a broad spectrum of peer-reviewed, bioinformatics-related topics covering the breadth and depth of this dynamically evolving field. Our topic submission procedures, keynote speakers, paper and poster presentations, tutorials and social events have all been designed to cater to bioinformatics' eclectic mix of disciplines. However, attendance is limited so please register early.

KEYNOTE SPEAKERS:

Russ Altman, MD, PhD
Professor of Genetics, Bioengineering, Medicine, Computer Science, Stanford University

Sydney Brenner, PhD
Distinguished Professor of Biological Studies, The Salk Institute, and 2002 Nobel Prize in Medicine and Physiology

Jacob T. Schwartz, PhD
Professor of Computer Science and Genetics, New York University Courant Institute

INVITED SPEAKERS:

Michael Ashburner, PhD, ScD
Prof of Biology, University of Cambridge; Professorial Fellow, Churchill College; Visiting Group Leader, European Bioinformatics Institute

Larry Goldstein, PhD
Professor of Cellular and Molecular Medicine, UCSD School of Medicine; Investigator, Howard Hughes Medical Institute

Ron Kikinis, MD
Director of the Surgical Planning Laboratory, Department of Radiology, Brigham and Women's Hospital and Harvard Medical School

Isaac Kohane, MD, PhD
Associate Professor of Pediatrics and Medicine, Harvard Medical School; Director, Children's Hospital Informatics Program

Srikanta Kumar, PhD
Program Manager, DARPA; Senior Technical Advisor, Information Technology Lab, National Institute of Standards and Technology (NIST)

Daniel Rokhsar, PhD
Professor of Molecular Cell Biology, Physics, UC Berkeley; Program Head, Computational Genomics, JGI

Arthur Toga, PhD
Professor of Neurology, UCLA School of Medicine; Director, Laboratory of Neuro Imaging; The Center for Computational Biology

Bioinformatics - scientific and engineering disciplines bringing new biological discoveries to fields as varied as human health, agriculture, the environment, energy and biotechnology. Find out more at **CSB2005**

Who should attend:

Bioinformaticists, Biologists, Computer Scientists, IT Professionals, and Engineers who want to quickly learn about the evolving field of bioinformatics.

Location:

Held on the Stanford University campus, **CSB2005** is easily accessible to professionals living in the SF Bay Area and Silicon Valley.

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For more Conference details including session titles, technical presentations, and on-line registration, please visit:

conferences.computer.org/bioinformatics

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Tutorials Offered on Monday, August 8
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Introduction to Factor Graphs and the Sum-Product Algorithm:
Genome Tiling Microarrays and Gene Interaction Networks
Novel Visualization and Analysis Methods in BioImaging
RNA-interference: The Short and Long of It
Computational Methods in MS-based Proteomics
AFTERNOON TUTORIALS
Introduction to the Semantic Web for Bioinformatics
Structure Based Methods for Identifying Protein Function
Pattern Discovery in Sequences and Structures
Understanding the Biological Data Deluge through Phylogenetics
Statistical Approaches to Analyzing Biological Networks

Listing of tutorial descriptions and instructors at

conferences.computer.org/bioinformatics

Friday Workshops – See next page ➔

The Life Sciences Society will be sponsoring **four parallel workshops** to be held on Friday, August 12 at Stanford University, as satellite events of the **CSB2005** Conference.

BioImage Data Mining and Informatics
Chaired by Hanchuan Peng, Lawrence Berkeley National Lab, UC Berkeley
Sponsored by the Life Sciences Society

Controlling Complexity
Chaired by Mike Hinchey, NASA Goddard Space Flight Center
Sponsored by the Life Sciences Society in conjunction with the IEEE Technical Committee on Complexity in Computing

Exploring 3D Molecular Structures Using NCBI Tools
Chaired by Eric Sayers, NCBI
Presented by the National Center for Biotechnology Information (NCBI) and sponsored by the Life Sciences Society

BioSPICE and Use Cases (half-day)
Presented by Quantum Intelligence, Inc.
Sponsored by the Life Sciences Society and BioSPICE Community

Lunch is included

CSB Conference registration is not required to sign up for a Workshop. Learn first-hand about this new engineering field!

WORKSHOP REGISTRATION includes snacks and lunch on Friday, August 12.

WORKSHOP FEES (US dollars)	ADVANCE	ON-SITE
LSS Member	$100.00	$130.00
Non-member*	$160.00	$190.00

* Fee Includes membership In LSS for One Year

For additional information and to register for these Friday Workshops, please see:

www.lifesciencessociety.org

The goal of the **Life Sciences Society** (LSS) is to foster collaboration among the various research disciplines that have a strong emphasis on the study of LIFE: biology, computer science, physics, engineering: electrical, chemical and mechanical, medicine, mathematics, pharmacology, microarray chip designs, drug discovery, genetic therapies, food production, stem cell analysis, high performance computing, and more.

Show your support for creating the **Life Sciences Society** within IEEE. Sign our petition now:

www.lifesciencessociety.org

IEEE Professional Skills Courses

SCV Chapters, Engineering Management & Components, Packaging and Manufacturing Technology Societies

Communication and Conflict Management Using MBTI

- Date/Time: Wed August 17, 8:30 AM - 4:30 PM
- Instructor: Linda Price
- Location: LSI Logic, Milpitas
- Fee: $350 for IEEE Members; $425 non-members

The Myers-Briggs Type Inventory (**MBTI**) is the most widely used instrument in the world to gain a deeper understanding of self, others and interpersonal relationships. It provides insights on the four basic "people patterns" that hold the key to leadership styles, effective communication, conflict, team building and productivity.

- Discover your Myers-Briggs Type Indicator
- Gain insights of your own communication strengths
- Understand four basic "people patterns"
- Discover your preferred communication and conflict style
- Practice how to communicate and influence each type
- Recognize barriers to effective communication
- Listen for problem statement, content and intention
- Learn how to use questions that gain quality information
- Separate facts from emotions
- Speak with clarity and commitment

Transitioning from Individual Contributor to Manager

- Date/Time: Thursday, August 4, 8:30AM-4:30PM
- Instructor: Roxanna Dunn
- Location: Cypress Semiconductor, San Jose
- Fee: $350 for IEEE Members; $425 non-members

"Excellent! The instructor's experiences have clearly demonstrated direction and path I would like to experiment. This class was very clear and concise"

High Impact Coaching

- Date/Time: Tuesday, August 16, 8:30AM-4:30PM
- Instructor: Dr. Andrew Oravets
- Location: Sybase, Inc, Dublin
- Fee: $350 for IEEE Members; $425 non-members

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2 Choices the week of August 9-12:

Digital Signal Processing -- 4-day class with labs:

DSP System Design and Implementation

Overview: Today's technology provides DSP processors that can be easily used to design very sophisticated products for instrumentation, control systems, communications, and wireless systems. This course presents DSP system design and implementation using programmable signal processors. Hands-on laboratory exercises are used to present the design and implementation aspects, using hardware and software tools for system implementation. The 5 laboratory sessions follow the lectures, where participants will apply system design concepts by designing, implementing, debugging and evaluating DSP schemes.

Wireless -- 4-day class with labs:

Wireless Transmitters

Overview: There are a number of transmitter architectures developed to satisfy the linearity requirements of modulation techniques employed in short- and long-range communication applications. This exceptional course introduces the modulation techniques and wireless standards, and compares the RF properties and performance of the CMOS, SiGe and GaAs technologies. The laboratory sessions of the course involve using the MATLAB/VerilogA simulators for behavioral characterization of transmitters by generating baseband signals of constant envelope, varying envelope communication systems, and applying transmitter nonlinearities. Throughout the lab projects, one will be able to understand and characterize the mask, the bandwidth and the peak to average ratio of communication signals and measure the distortion and spectral regrowth caused by transmitters.

Come to San Jose State!

Easy access: class starts before most students arrive on campus, so parking in the 7th Street garage is a snap!
Cost: $995 per course (includes student notebook, lunches and refreshments, CDs with class notes and problem solutions for certain classes)

Review the full course Flyer:

www.e-grid.net/docs/sjsu0508.pdf

for course overviews, prerequisites, instructor profiles, registration, map

3 Choices the week of August 16-19:

Digital System Design -- 4-day class with labs:

Embedded Systems and Embedded FPGAs

Overview: This short course is designed to introduce the fundamentals of embedded systems, and embedded FPGA design methodology. The objectives are to give an overview of the technology, the fundamentals and advanced issues, and hand-on experience with embedded FPGAs. The Laboratory modules provide hands-on experience with configuring the processor core, developing IP with VHDL, writing driver, system integration and test routines. Students will be exposed to a learning experience balanced between fundamental and advanced issues, theoretical concepts to hand-on experiments that will help them progress from novice to expert within a short time.

Digital System Design -- 4-day class with labs:

FPGA DSP System Design

Overview: This course provides an in-depth and state-of-the-art coverage of the design and FPGA-based implementation of high-performance DSP systems. After presenting FPGA architectures and design tools by Xilinx and Altera, several hands-on design labs on DSP, digital communications and video/imaging will be covered, including FFT, FIR filters, error detection/correction circuits, modem, color space converter, and DWT (Discrete Wavelet Transform). Contents: Basic DSP/Communication theory, FPGA architecture/design tools, HDL (VHDL and Verilog), DSP-specific arithmetic circuits, hardware design of digital filters, FFT circuits, error detection & correction circuits, encryption/decryption circuits, and video/imaging circuits.

Networking Engineering -- 4-day class with labs:

High-Speed Data Networks

Overview: This course covers architectures, delay modeling, and the latest innovations in broadband computer-communication networks – detailed studies on design and analysis of high-speed switches and routers, design of input/output interfaces for fast routers with quality-of-service provisions, design of multicast switches and networks, delay modeling, bandwidth allocations and congestion control methods for broadband networks, voice compression for higher data rates, voice over IP, and the latest techniques in wireless communication systems. The course starts with a brief overview of high-speed networks and architectures and continues with the design of switching systems and routers and router interfaces with quality-of-service provisioning. The course then addresses delay analysis and congestion control techniques, and then targets some of the most demanded topics such as the design of multicast high-speed networks, voice over IP, and wireless high-speed networks. The labs are hands-on experiments in Computer networking.

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- Boise Cascade
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- Alaska Power Authority

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Lecturer in Electrical Engineering

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Open Position: The Department invites applications for a one year faculty position in the area of **communications**; an emphasis on wireless is desirable but not necessary.

Duties: The person selected for this position would teach the equivalent of **two to three courses per academic quarter**, including both undergraduate and graduate courses in communications and other fundamental electrical engineering topics. Other duties include advising students and supervising senior design projects. Some teaching experience is desirable. For new PhD applicants, teaching assistantship experience is valuable.

Qualifications: Candidates should have a successful track record in teaching electrical engineering at the undergraduate and graduate levels or as a teaching assistant. Candidates should have earned a master's degree or doctorate in electrical engineering.

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Santa Clara, CA 95053-0560

Inquiries: For additional information please contact Benjamin Greer, the search coordinator:

Email: **bgreer@scu.edu** Phone: 408-554-5313 Fax: 408-554-5474

For additional information about the department please refer to our web site:

www.scu.edu/engineering/ee

The Department will begin considering applications immediately and continue until the position is filled. Santa Clara University is an equal opportunity affirmative action employer, and welcomes applications from women, persons of color, and members of other historically under-represented US ethnic groups.

Cogswell Polytechnical College
Sunnyvale, CA

Cogswell Polytechnical College

The Roy B. Anderson Endowed Chair in Electrical Engineering

Cogswell Polytechnical College invites applications for an endowed full-time faculty position, the Roy B. Anderson Chair in Electrical Engineering. A candidate for this position will lead the development of the electrical engineering program to implement the fusion of art and engineering. He/She will have the desire and knowledge necessary to create devices and systems to support innovation in the Digital Arts.

The ideal candidate will possess a doctorate (Ph.D., Sc.D., or equivalent) in Electrical Engineering by the beginning of the appointment period and have experience in teaching at the undergraduate level and in relevant industry. Interested individuals should submit a current curriculum vitae, a description of significant background, and three letters of recommendation of professional or academic nature.

Small, but highly focused, Cogswell offers programs leading to B.A. and B.S. degrees in Digital Art and Animation, Digital Motion Picture, Digital Arts Engineering, Digital Audio Technology, Electrical Engineering and Software Engineering.

Deadline open until filled. All applications should be directed to:

Roy B. Anderson Chair in Electrical Engineering,

EEVacancy@cogswell.edu or

Cogswell Polytechnical College, 1175 Bordeaux Drive, Sunnyvale, California 94089

SCV Consumer Electronics

TUESDAY JULY 26

Wireless at Home: Home Infotainment Networking

Speaker: Mike Stauffer, Director of Business Development, Atheros
Time: 6:30 PM pizza and networking; 7:00 presentation
Cost: $5 for IEEE Members, $10 for others
Place: Oak room (Building 48) at H-P, 19447 Pruneridge Avenue, Cupertino
RSVP: Please reserve by email, to scv.ce@ieee.org
Web: www.ieee.org/scvce

This presentation will describe how home networks are evolving from simply sharing Internet access and printers into comprehensive home infotainment networks that enable consumers to consume Any Content Anytime and Anywhere, with No New Wires. After introducing the overallconcept of home infotainment networking and several possible networking solutions, the presentation will focus on wireless networking solutions, primarily 802.11 solutions. The discussion will describe key requirements for home infotainment networking and how the various 802.11 technologies meet these requirements. Emerging technologies such 802.11n will be included.

Mike Stauffer is responsible for developing the home entertainment networking market for wireless products. He has over 30 years electronics industry experience in multiple functional disciplines and markets, ranging from semiconductors to systems in telecommunications, digital video and medical systems. Previous experience includes Founder, VP & General Manager of Hyundai Digital Video Systems with worldwide responsibility for digital settop box products and the first supplier to BSkyB; VP of Client Technology at iBlast, a broadcast networking company involving 250 US TV stations; Director of Business Development at Compression Labs, involved with developing the DirectTV broadcast system, settop boxes and videophones; Director of Marketing at Zoran; founder of several companies in the TV display business; various marketing, engineering & consulting positions with Intel, AMD, DSP Group, Searle Ultrasound, Syntex Medical Systems. Mike was an early participant in the JPEG, MPEG and DVB standards efforts. Mike has a BSEE/CS from MIT, an MSEE from Stanford and has attended the Stanford Business School Executive Education Program.

SCV Instrumentation & Measurement

WEDNESDAY AUGUST 3

Contamination Analysis using Surface Analytical Tools

Speaker: Gary Mount, Cascade Scientific Labs Inc.
Time: 7:30 PM
Cost: none
Place: Cogswell College Room 197,
1175 Bordeaux Dr, Sunnyvale
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/ims/

Surface analytical tools will be described and their capabilities outlined. The focus will be on contamination analysis, showing what is possible and providing practical examples. The discipline of surface science possesses many analytical tools that allow us to examine the surface of solids for contamination. We can identify elements, chemical bonding, concentration, and depth distribution. We can examine atomic layer contamination, thicker layers, and particles. This presentation will give an overview of what is possible, providing practical examples.

SCV Electron Devices

TUESDAY AUGUST 9

Organic Photovoltaics: Low-cost, Stable, Non-toxic Solar Cells using Organic Pigments

Speaker: Dr. Peter Peumans - Stanford University
Time: Pizza social at 6:00 PM;
Presentation at 6:15 PM
Cost: none
Place: National Semiconductor Corp. Building 31
Large Auditorium, 955 Kifer Road,
Sunnyvale
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/eds/

Peter Peumans received his BS and MS in Electrical Engineering from the Katholieke Universiteit Leuven (Belgium) and IMEC (Heverlee, Belgium) in 1998. He received his Ph.D in 2004 from Princeton University (Princeton, NJ) where he worked with Steve Forrest. Since 2004 he has been a professor at Stanford working in the area of organic and molecular electronics. His current interests are in using new materials to make better devices and systems: Physics of organic materials, metallic optical antennas, organic photovoltaic cells, light-emitting diodes and memories, protein scaffolds for terascale electronics, self-assembled and self-organizing circuit architectures.

Thin-film organic solar cells have attracted attention over the last decade because of their potential to substantially reduce the cost of solar electricity by lowering the cost of the substrate, materials, processing and installation. In addition, organic materials allow very thin and flexible cells to be designed, leading to entirely new device concepts that may revolutionize the way we harvest solar energy, such as roll-up solar cells and solar textile fiber. The power conversion efficiency of organic solar cells has increased steadily since the demonstration of the donor-acceptor and bulk heterojunction architectures to the current state of the art of ~5%, but remains far below that achieved in amorphous (~12%) and crystalline silicon (~24%) cells. In this talk, I will analyze the efficiency limits of organic solar cells and compare the current state-of-the-art with these limits. It will be shown that the separation of geminate electron-hole pairs at the donor-acceptor junction is a dominant loss factor. The efficiency of this process depends strongly on the ratio of the electron and hole mobility. Our analysis provides precise guidelines for increasing the efficiency of bulk heterojunction photovoltaic cells. To further improve the power conversion efficiency, we are developing multijunction architectures that allow several cells to be stacked in a series connection. These devices rely on metal nanoclusters as effective recombination layers between adjacent cells. The optimization and fabrication of multijunction organic solar cells with wide spectral coverage will be discussed.

SCV Instrumentation & Measurement

WEDNESDAY SEPTEMBER 7

Introduction to the Stanford Nanofabrication Facility, with Research Examples

Speaker: Paul Rissman, PhD, Director of Research Operations, Stanford Nanofabrication Facility
Time: 7:30 PM networking, 8:00 PM presentation
Cost: none
Place: Cogswell College Room 197, 1175 Bordeaux Dr, Sunnyvale
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/ims/

The Stanford Nanofabrication Facility is part of the NSF's National Nanotechnology Infrastructure Network. It is a research and development facility with a wide variety of semiconductor processing equipment that is open to external use. In a typical month, there are 200 users of the facility comprised of 120 Stanford graduate students, 20 students and faculty from other universities, and 60 industrial users, primarily from start-up companies. Projects in the lab come from the study of MEMS/NEMS, bio-MEMS/NEMS, sensors/actuators, nanotubes/ nanowires, semiconductor materials and device research, magnetic technology, photonic devices and many other fields.

Paul Rissman is the Director of Research Operations of the Stanford Nanofabrication Facility at Stanford University in Palo Alto. His undergraduate and graduate education was in Electrical and Computer Engineering at the University of Wisconsin in Madison. Paul worked 26 years in the semiconductor industry, including 2 years at Amdahl Corporation, 20 years at Hewlett Packard, and 4 years at LSI Logic, serving in various management positions for the last 19 years. He has 26 publications, 4 patents granted, 2 patents filed, and 2 patents disclosed in the fields of semiconductor processing, electron beam lithography, superconducting junction technology and other fields.

WEDNESDAY SEPTEMBER 14

Kirkendall Voids in Lead-Free Solder Joints: A Reliability Issue

Speaker: Zequn Mei, Cisco
Time: Seated dinner at 6:30 PM; presentation at 7:30 PM
Cost: $25 if reserved by Sept. 11; $30 at the door; presentation-only is free
Place: Ramada Inn, 1217 Wildwood Ave (Fwy 101 frontage road, between Lawrence Expy and Great America Pkwy), Sunnyvale
RSVP: Please reserve and pay in advance using our PayPal on-line system or email Janis Karklins
Web: www.cpmt.org/scv/

Zequn Mei received his Ph.D. of Materials Science and Engineering from University of California at Berkeley. He is currently working at Cisco Systems, in the Manufacturing Technology Goup, on interconnect reliability.

Previous studies demonstrate extensive Kirkendall voids at the interface of a solder joint to a copper substrate, and their significant effects on the impact and shock strength of the solder joints. This talk focuses on two issues: the condition for the void formation; and the effect of voids on solder joint reliability. Samples of electronic assemblies of different packages aged or thermal-cycled were cross-sectioned by either FIB or sputtering etching. The results show that voids at the Cu/solder interface formed extensively in some cases, but not so much in others. So far, we are not clear exactly what factors control the void formation; it seems that the Cu plating process and the small concentration of Ni in either the solder or the substrate influences the void density and distribution. Shock strength at 400G of BGA packages aged for 20 days at 125°C did not degrade; the failure occurred by either delamination at the fiber/resin interface underneath the non-solder-mask-defined Cu pads, or inside the solder where they were close to the solder-mask-defined Cu pads. We also curve-fitted the result of voids growth vs time at different temperatures with the equation of A = C t 0.5 exp (-Q/RT), to use it for prediction of the voided area at the product's service condition.

CONFERENCE CALENDAR

The **CONFERENCE CALENDAR** is a service to our IEEE Members. It outlines upcoming IEEE workshops and conferences in the Bay Area. Please submit items to the GRID Editor: editor@e-grid.net.

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www.e-grid.net/docs/conf-flyer.pdf

August 8-11: IEEE Computational Systems Bioinformatics Conference

- August 8: Tutorials - August 9-11: Sessions
- At Stanford University (plenty of free parking)

CSB2005 brings you cutting-edge research on biological discovery and innovation through multidisciplinary presentations that can change the world of biology, medicine and drug discovery – and by changing this world, change the lives of the people waiting for cures. **CSB2005** provides a broad spectrum of peer-reviewed, bioinformatics-related topics covering the breadth and depth of this dynamically evolving field.

See Page 7 for more details

16th Annual Magnetic Recording Conference

"Heads and Systems"

August 15-17, 2005

Held at Stanford University in Palo Alto

See **Page 6** for more details

September 13-15: International Symposium on Semiconductor Manufacturing

- San Jose Fairmont Hotel
- Workshops: Monday, September 12
- Sessions: Tuesday – Thursday

The 14th ISSM will be held at the San Jose Fairmont Hotel. ISSM is the largest world-wide forum specifically designed for semiconductor device manufacturers and suppliers.

See Page 4 for more details

Sept 22-23: Antenna Systems and Short-Range Wireless Conferences

Held this year at the Santa Clara Marriott, these co-located events bring together the foremost experts on antenna systems and short-range wireless standards & technology.

Early-bird discount through August 19th

See Page 5 for more details