
## Chapter Meetings

*SCV-CNSV - 1/10 & 1/24*: **Entrepreneurs SIG** - this SIG is part of the Consultants' Network of Silicon Valley... **[more]**

*SCV-EDS - 1/11:* **Extremely Thin Fully Depleted SOI (ETSOI) Devices** - a choice for 45nm technology nodes... **[more]**

*SCV-PACE - 1/11:* **The Job Market in the Valley and its Career Implications** - transitory and structural forces that change the job-search strategy ... **[more]**

*SCV-CPMT/LEOS - 1/12*: **Optical Fiber Coatings: The State-of-the-Art and the Application of a New Nano-material** - an attractive substitute for existing optical fiber coatings ... **[more]**

*SCV-Com - 1/13*: **Broadband Wireless Technologies and Standards** - European broadband radio access networks and WiMax broadband wireless metropolitan area networks ... **[more]**

*SCV-MTT - 1/13:* **Film Bulk Acoustic Resonators (FBAR**) - development history and role in future radio architectures ... **[more]**

*SCV-Mag - 1/18:* **Moore's Law and Magnetic Recording Areal Density - A Processing Perspective** - growth of magnetic recording density from the perspective of thin film processing ... **[more]**

*SCV-PSES - 1/18:* **Gateway to a New Thinking in Energy Management - Ultracapacitors** - ultracapacitor technology, current applications and future opportunities ... **[more]**

*SCV-CNSV - 1/18:* **Peering into the Network Industry Future** - the causes for the downturn, dynamics of the network industry, and future possibilities ... **[more]**

*SCV-EMB - 1/19*: **The Diagnostic Potential of Airway Gas Analysis Using Cavity Ringdown Spectroscopy** - description of a novel spectrometer-based health monitoring system ... **[more]**

*SCV-PES/IAS - 1/19:* **Circuit Breaker Protection** - covering a number of topics related to low-voltage circuit breakers ... **[more]**

*SCV-SSC - 1/20:* **Design Considerations for Low-Power WCDMA Direct-Conversion RF Receivers** - higher integration, higher sensitivity, lower die area and lower power ... **[more]**

*OEB-IAS - 1/20:* **Hybrid Electric Vehicles -- Design and Environmental Impact** - key technologies behind electric-drive vehicle design: advanced batteries, traction, fuel cells... **[more]**

*SCV-CE - 1/25*: **The Content of Storage** - digital storage device requirements for key markets, with a storage hierarchy ... **[more]**

*SCV-REL - 1/26:* **Developments at the Int'l Symposium for Testing and Failure Analysis (ISTFA)** - a panel discussion of selected papers from ISTFA ... **[more]**

*SCV-CPMT - 1/27:* **Trends in Packaging Technology - The International Packaging Roadmap Update** - cost, thermal & electrical performance, size, pin count, reliability... **[more]**

## Upcoming Conferences

22-27 January: **Photonics West**
San Jose Convention Center … **[more]**

27 Feb – 4 March: **Microlithography Symposium**
San Jose Convention Center … **[more]**

6-10 March: **Embedded Systems Conference**
Moscone Convention Center, San Francisco … **[more]**

21-23 March: **Symp on Quality Electronic Design**
Double Tree Hotel, San Jose … **[more]**

## Upcoming Courses in the Bay Area

**Reliability Engineering**
6 week course, beginning January 11 … **[more]**

*At San Jose State, week of Jan. 18th:*
**- DSP System Design and Implementations**
**- FPGA DSP System Design**
**- VHDL for Synthesis and Verification**
**- Device Physics and VLSI Technology**
**- Sensor Network Technology**
Theory and labs in current technologies **[more]**

*1-3 February:* **Intelligent Control & Soft Computing -- Neural Networks, Fuzzy Logic, Genetic Algorithms**
three-day class from top experts, at NASA Research Park - how to design and apply fuzzy logic and neural networks techniques **[more]**

## February Meetings

*SCV-Com - 2/9:* **Open Wireless Architecture (OWA) for Next Generation Wireless and Mobile Communications** - integration of different wireless access technologies in a common flexible and expandable platform ... **[more]**

*SCV-Mag - 2/15:* **Spin Torque and Nanorings** - description of two new topics in magnetic nanostructures from inception to realization to potential applications ... **[more]**

*SCV-SSC - 2/17:* **SiGe Heterojunction Bipolar Technology and Applications** - HBT's can be easily integrated into a standard CMOS flow for full-fledged manufacturing ... **[more]**

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**Marketplace** **page 3**
**IEEE & Council News** **page 29**
**Conference Calendar** **page 30**

# IEEE GRID

***Your Networking Partner®***

January *2005 • Volume 52 • Number 1*





IEEE **GRID** is the monthly newsmagazine of the San Francisco Bay Area Council of the Institute of Electrical and Electronics Engineers, Inc. As a medium for both news and opinion, the editorial objectives of IEEE **GRID** are to inform readers in a timely and objective manner of newsworthy IEEE activities taking place in and around the Bay Area; to publish the official calendar of events; to report on IEEE activities of a national and international scope; and to serve as a forum for comment on areas of concern to the engineering community by publishing contributed articles, invited editorials and letters to the editor.

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Editor: Paul Wesling
IEEE **GRID**
12250 Saraglen Dr.
Saratoga CA 95070
Tel: 408 331-0114 / 510 500-0106 /
415 367-7323

Fax: 408 904-6997
Email: editor@e-grid.net
**www.e-GRID.net**

## *From the editor . . .*

As we start a new calendar year, we install new officers in all of our Chapters as well as in our Sections. Next month we'll publish a listing of all the "new blood" – those tireless volunteers who help all of us keep up with the leading edge of our technology by organizing Chapter meetings, putting together pertinent tutorials and symposia, and bringing us conferences in our specialties.

Have you ever wondered how these important people go about choosing the topics that you see at the evening meetings? How they round up these great speakers? Why they seem to know all the "movers and shakers" in your specialty? Believe it or not, they started out just like you! They probably came to a few IEEE meetings, met some of the then-important people (in their early days), and spoke up to suggest another topic or a better way of doing something for the Chapter. They found themselves as "junior members" of the Chapter executive committee, contributing ideas and helping out. The networking contributed to their knowledge of the important technologists in your field – they eventually felt comfortable calling other technologists to stop by the Bay Area to give a talk to us on something that interested them.

In a few years, YOU could be one of these influential specialists in your field. Stop one of your new Chapter officers and ask how YOU can help.

*Paul Wesling* **editor@e-grid.net**

NOTE: This PDF version of the IEEE GRID – the **GRID.pdf** – is a monthly publication and is issued a few days before the first of the month. It is not updated after that. Please refer to the Online edition and Interactive Calendar for the latest information: **www.e-GRID.net**

Photonics WEST

The International Society for Optical Engineering

# • Biomedical Optics • Optoelectronics • Lasers and Applications • MOEMS-MEMS

## 22 - 27 January 2005

## San Jose Convention Center

CLICK! spie.org/events/pwest

## Multiple Conference Tracks: (partial listing)

### Biomedical Optics

• **Photonic Therapeutics and Diagnostics:** Applications to Tumor Treatment, Urology, Dermatology, Plastic Surgery, Soldering Tissue, Cardiovascular, Neurosurgery, Brain Imaging

• **Clinical Technologies and Systems:** Optical Coherence Tomography, Clinical Diagnostics, Spectral Imaging

• **Tissue Optics and Engineering:** Optical Interactions with Tissue and Cells, Imaging and Sensing, Energy Delivery

• **Biomedical Spectroscopy, Microscopy, and Imaging:** Optical Diagnostics and Sensing, Biomolecules and Cells, Multiphoton and 3-D Microscopy

• **Nano/Biophotonics:** Plasmonics, Microarrays, Combinatorial Techniques, Genetically Engineered Probes, High-Throughput Screening, Applications

### Integrated Optoelectronic Devices

• **Optoelectronic Materials and Devices:** Physics/Simulation, Organic Photonic and Nanostructure Materials, Photodetectors

• **Photonic Integration:** Devices, Materials, Technologies, Optoelectronic ICs, Photonics Packaging

• **Nanotechnologies in Photonics:** Quantum Sensing, Photonic Crystal Materials, Nanophotonic Devices, Quantum Dots, Nanoparticles, Nanoclusters

• **Displays and Holography:** Projection Displays, Liquid Crystal Technologies, Practical Holography

### Lasers & Applications in Science & Technology

• **Laser Source Engineering:** Solid State Lasers, Laser Resonators, Beam Control, Fiber Lasers

• **Laser Micro-/Nanoengineering & Applications:** Micro-Packaging, Optoelectronic Manufacturing, Synthesis and Photonics of Nanoscale Materials, Ultrafast Lasers

**Plus dozens of other tracks – see the website for details**

**Product Spotlight Demos:** Multispectral 3CCD Color Digital Cameras • Ti:Sapphire Laser Systems • Wavefront Sensing • MEMS/MOEMS Encapsulation • Yellow Solid State Lasers • Optical Filters • plus more

**Complimentary WiFi access for attendees**

**Preplan your visit with MyExhibitionPlanner, on the website**

## Short Courses (Separate registration allowed)

Choose from 68 courses and workshops on hot topics:

**Basic Optics:** Optical System Design • Fourier Optics and Diffraction • Gratings, Monochromators, and Spectrometers • Modern Optical Testing • Diode Lasers • Geometrical Optics • Basic Optics for Non-Optics Personnel

**Biomedical, Biophotonics, Microbiochips:** Biocompatible Materials • Planar Waveguide Biochemical Sensors • Biochip Fundamentals and Fabrication • Biophotonics • Microfluidics

**Optical Components and Systems:** Optical System Design • Optical Alignment Techniques • Thin Film Optical Coatings • Plastic Optical Systems • Aspheric Optics • Geometrical Optics

**Semiconductor Lasers, LEDs, Illumination:** Solid-State Lighting • Testing and Reliability • VCSELs • Diode Laser Selection • LED Optical Properties • Quantum Dot Laser Diodes

**Lasers and Nonlinear Optics:** Laser Diode-Pumped Solid-State Lasers • Fiber Laser Sources • Femtosecond Laser Techniques • Nonlinear Optics • Laser Product Certification

**Plus 40 others** – see the Website for listing/descriptions

**Course capacity is limited -- register now to ensure your participation!**

Students Save 50% on Courses  Group discounts available

## Free admission to Two Exhibitions

**Biomedical Optics Exhibition:** Focused on lasers, fibers, and optics in medicine, the BiOS exhibition showcases the latest commercial applications of biomedical optics, instrumentation, component MEMs, bio-MEMs and more.

**Saturday 1-5 and Sunday 10-4**

**Photonics West** is North America's largest commercial exhibition on optics, lasers, biomedical optics, optoelectronic components, and imaging technologies, with 800 exhibitors.

**Tuesday and Wednesday 10-5, Thursday 10-4**

**Preregister – or come to the Convention Center and register on-site for your free pass**

## Register by January 7th to get the $100 preregistration discount!

**For Symposium and registration information, please access the Photonics West website:**

CLICK! spie.org/events/pwest

*The Largest System Design Event in North America*

# *EMBEDDED SYSTEMS CONFERENCE*

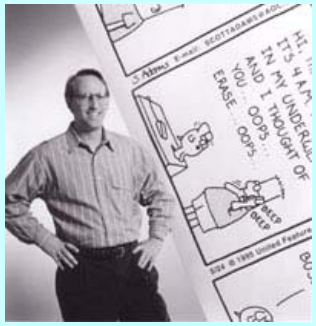
## March 6 – 10, 2005
## Moscone Convention Center
## San Francisco

CMP United Business Media

EmbeddedSystems Conference San Francisco

## Visit www.esconline.com/sf/ CLICK!

The Embedded Systems Conference offers an exciting line-up of special events. All of our special events are free to registered attendees and range from keynote addresses to networking opportunities and receptions, to panel discussions all designed to enrich your event experience.



### Keynote Address:
**Cartoonist Scott Adams:**
**From Cubicles to Comics**
**Tues March 8, noon - 1:00 PM**

### Design Seminar Keynote:
**Software Defined Radio — Business, Market, and Social Ramifications**
**Stephen M. Blust and Mark Cummings, SDR Forum**
**Wed March 9, 2-3 PM**

### Panel Discussions
**The Future of Processors for Signal Processing Applications**
Monday, March 7; 6–7 PM

**After the Storm: How the Industry has Changed Forever**
Wednesday, March 9; 1 – 2 PM

**Engineering Humanity: Managing the Chaos**
Thursday, March 10; 10:00am - 11:00am

**Plus Other Panel Discussions:**
- Moving Beyond 3G: Where Do We Go From Here?
- The Transformation of the TV
- Silicon Support at Layer 7: XML, SOAP, and Vertical Protocols
- The Future of Wireless Networking

## Technical Program

***Sunday full-day tutorials***
• User Interface Design • Migrating from a Legacy RTOS to Embedded Linux • Scaling System Design • Embedded Linux Jumpstart • Embedded C Programming • Introduction to Real-Time Operating Systems • Real-Time UML

***Monday full-day tutorials***
• Real-Time Kernels • System Architecting and Tradeoffs • Managing Embedded Projects • Real-Time Design Guidelines and Rules of Thumb • Embedded GNU Jumpstart • Crafting Embedded Systems in C++ • Architectural Design of Device Drivers • TCP/IP Networking

$645 for one full day; $995 for BOTH days

**Plus 132 three-hour and 90-minute Technical Classes** on Tuesday through Friday– see the Advance Program for listing/descriptions and times for each topic.

**Register now to ensure your participation!**
**www.esconline.com/sf/program**

**Seven full- or multi-day DESIGN SEMINARS:**
- **Analog and Power** (Monday – 2 tracks)
- **DSP Performance** (Monday – 2 tracks)
- **Easy Paths to Silicon** (Mon & Tues, 2 tracks)
- **Consumer Systems** (Tues & Wed, 2 tracks)
- **3G Cellular Systems** (Tues & Wed, 2 tracks)
- **Wireless Networking** (Wed & Thurs, 2 tracks)
- **Network Systems** (Wed & Thurs, 2 tracks)

*... and the new*
**Microprocessor Summit** (Monday) – new-product introductions in AM; three tracks on shipping products in PM

## Visit the Exhibits *(free admission)*

The Embedded Systems exhibits floor features leading companies showcasing cutting-edge hardware, software, tools, and the full spectrum of system components! You will learn relevant new skills, meet and talk with vendors, network with peers, and develop new strategic partnerships – all under one roof, at one time, with both daytime and evening hours:

**Tues 1-8pm – Wed 10am-7pm – Thurs 9am-2pm**

**Visit www.esconline.com/sf/exhibits** CLICK!

### Flexible Registration Packages
- **1-day, 2-day, 3-day, full 5-day, or the ePass value**
- **Free Exhibits Pass (includes Keynotes and Panels)**
- **Choose exactly what suits your needs and schedule**
- **Group rates – bring your team (save 15% and more)**

**Register by January 11th for early-bird rates!**

**Visit www.esconline.com/sf/** for full details

Ride BART or MUNI to the Powell Street station

# Microlithography 2005

SPIE The International Society for Optical Engineering

## 27 February – 4 March 2005
## San Jose Convention Center
## www.spie.org/events/ml05

**Conferences – Courses – Exhibits**

## Six Conference Tracks:

### Emerging Lithographic Technologies
EUV Systems/Optics/Materials - Advanced Mask Characterization – Nanoimprint - Maskless Lithography - Electron Projection Lithography - Novel Lithography Systems

### Metrology, Inspection, and Process Control
OPC/RET - Overlay, Registration Errors - SEM/Scatterometry for Critical Dimension Metrology - CD Measurement and Reference Systems/Comparisons - Overlay Tool and Mark Development - Line Edge Roughness - Integrated Metrology/Design - Line Edge Slimming - Mask-Related Defect Analysis - CD Uniformity Control

### Advances in Resist Technology & Processing
Immersion - 193nm/157nm Materials - ARC/Bilayer - EUV/E-beam - Novel Materials/Applications/Processing - Pattern Collapse/Defectivity - Resist Processing – Simulation - Line-Edge Roughness - ARC/EUV

### Optical Microlithography
Polarization and High NA - Immersion Lithography - Low K1 Process Control & Performance - Image Quality & Characterization - Image and Process Modeling - Mask Polarization Effects - Advanced Lithographic Materials - Advanced Exposure Systems and Components

### Data Analysis & Modeling for Process Control
Advanced Process Control - Data Modeling for Control - CD Uniformity Control - Advanced Process Control - Methods for Data Analysis and Automation

### Design and Process Integration for Microelectronics Manufacturing
Design, Automation and Characterization - Design Optimization and RET - Analysis and Modeling - Design for Yield - OPC and RET

## Plenary Presentations: (full details in Advance Program)

**Full-chip CD analysis and design optimization for 90-nm node and below**, Christopher Spence, AMD

**The flat panel display paradigm: Successful implementation of Microelectronic Processes on Gigantic Wafers**, Zvi Yaniv, CEO, Applied Nanotech

**Lithographic Technologies that Haven't (yet) Made it: Lessons Learned**, Fabian Pease, Stanford U.

## Panel Discussions:
Can NGL Crest the 32nm Summit: Where is the window of opportunity for emerging lithography? • Seamless integration of metrology and design for development and validation of OPC and RET • DfM Innovation Sources: Venture-backed companies, public corporations and academia

## Short Courses (Separate registration allowed)

Take advantage of these courses and workshops taught by leaders in the field – bring yourself up-to-date on the hottest technologies or get the background basics you need. You can register for Short Courses without attending the full Symposium.

***Sunday full-day courses***

Intro to Microlithography: Theory, Materials, & Processing • 193-nm Lithography • Lithography Control and Characterization • Lithographic Optimization: A Theoretical Approach

***Sunday half-day courses***

Introduction to Electron-Beam Lithography • Basics of Optical Imaging in Microlithography: Hands-on • Nano-Scale Patterning with Imprint Lithography • Instruments and Methodologies for Accurate Metrology • Pushing the Limits: Optical Enhancement, Polarization, and Immersion Lithography • 157-nm DUV Lithography • Optical Lithography Modeling • Intellectual Assets for Micro/Nanolithography

***Full-day courses during the week***

Applying Optical Proximity Correction and DfM • Plasma Etching and Reactive Ion Etching • Resists for Deep UV Lithography • Data Management: Understanding Chip-finishing, Tapeout, and Data Preparation

**Plus 13 others** – see the Advance Program for listing/descriptions

**Course capacity is limited -- register now to ensure your participation!**

Students Save 50% on Courses  Group discounts available

## Free admission to the Exhibits

The SPIE Microlithography Exhibition brings together all aspects of IC design, fabrication, processing, and manufacturing. You'll see the latest tools, instruments, components, and devices in lithographic technologies, along with expert representatives from over 130 companies.

**Exhibits are open 10-5 Tuesday and 10-4 Wednesday**

**Preregister – or come to the Convention Center and register on-site, for your free pass**

**Exhibit your product/service**  **Review list of exhibitors**

Tel: Sue Siegfried, 510-728-2105  **Download Advance Program**

## Register by February 15 to get the $100 preregistration discount!

**For Symposium and registration information, please download the Advance Program:**

## www.spie.org/events/ml05


# International Symposium on Quality Electronic Design

## "Design for Quality in the Era of Uncertainty"

## March 21-23, 2005 Double Tree Hotel San Jose

ISQED 2005 is a premier Design and Design Automation conference, held in technical sponsorship of the IEEE's Electron Devices and Components, Packaging & Manufacturing Technology Societies (EDS and CPMT), and in cooperation with IEEE CAS Society and ACM/sigDA. ISQED is the pioneer and leading conference dealing with design for manufacturability and quality issues, front to back. It spans three days, Monday through Wednesday, in three parallel tracks, hosting nearly 100 technical presentations, six keynote speakers, two panel discussions, workshops/tutorials and other informal meetings. Conference proceedings are published by the IEEE Computer Society, and the CD-ROM is published by ACM.

### Conference Audience:

- Designers of Integrated Circuits & Integrated Systems (IP, SoC, SiP)
- Researchers, Developers, and Users of EDA/TCAD Tools and Design Methodologies
- Process/Device Technologists and Semiconductor Manufacturing Specialists

### TUTORIALS (all day Monday):

- Design of sub-90nm CMOS Circuits and Design Methodologies
- Package-Chip Co-Design – Strategies and Challenges

### Panels:

- IP Creation and Use: What roadblocks are ahead?
- Nanoelectronics: Evolution or Revolution?

### Luncheon Talk:

"IP Quality: A Design, not a Verification Problem"
Michael Keating, Synopsys Inc.

### Technical Sessions:

• Tools and Flows for Quality • High Level Power/Noise Reduction Techniques • Leakage and Dynamic Power Issues • Test Application and Cost Reduction • DFM and Physical Layout • Performance and Reliability Analysis for Yield Optimization • Functional Verification and Test Generation • Power Delivery and Distribution • Quality System Level Design and Synthesis • DFM for Circuit Design • Leakage and Reliability Management • Analog Test and BIST • Design Methods and Tools in DSM • Design Techniques for Leakage Reduction • Variability Issues in Nanoscale Circuits • Issues in Noise and Timing • Design Approaches for System in Package (SiP) • DSM Interconnect Issues • Advances in Floor Planning • Issues in On-Chip Communication and Analog/RF Designs • Robust Design under Parameter Variations

**See the full Advance Program and Tutorial Descriptions (21 pages, 225kB PDF):**

**Download Now**

**Visit the ISQED website for more information and to register:**

**www.isqed.org**

**Early Registration through March 14th – save $100**

OPS ALACARTE™

Reliability Engineering Services
HALT and Classical Techniques
"Reliability Integration" SM

# RELIABILITY ENGINEERING COURSE

Reliability is a key attribute of the successful and profitable product. Understanding the disciplines and metrics and applying them during design, validation, test, and production yields big rewards. Yet, too few companies have engineering professionals who are skilled in the discipline of reliability.

If you are a **design, test, reliability, or production engineer** and need a good, in-depth course in hardware reliability engineering, this class can benefit you substantially. Key Topics:

-- Reliability Management
-- Probability and Statistics
-- Modeling and Prediction
-- Reliability Testing
-- Data Collection & Corrective Action Systems
-- Reliability Tools in Design and Development
-- Maintainability and Availability
-- Product Safety and Liability

OPS ALACARTE has offered the Reliability Engineering Course for several years. Students have found it very valuable in preparing for the Certified Reliability Engineer exam. *Becoming certified as a Reliability Engineer (CRE) can be valuable to your employer and your career. The success rate in passing is several times higher for students who have taken the course compared to those who have not.*

## *Course Starts January 11th, 2005*

| | |
|---|---|
| Instructor: | Jurek Zarzycki, CRE, CQE |
| Schedule: | Eight consecutive Tuesdays 6 - 10 PM from January 11th through March 1st, 2005 |
| Location: | Santa Clara, CA |
| Course Fee: | $995 including materials (Text Book and Solutions Book will be distributed the first night). A 25% discount is extended to anyone who is currently unemployed. |
| Registration: | This course fills up quickly and seating is limited. To register, please email to: relclass@opsalacarte.com or call (408) 472-3889 |

*Career-Advancement Short Courses with Labs*

## January Technology Series

- **Theoretical Aspects**
- **Hands-on Experience**
- **For working professionals**
- **Preparation for Tomorrow**
- **Excellent value; practical; timely topics**
- **5 Choices, all in the week of January 18, 2005**

San José State University

Department of Electrical Engineering

COLLEGE OF ENGINEERING

gateway to Silicon Valley

**Review the full course Flyer:**
**www.e-grid.net/docs/sjsu.pdf**
for course overviews, prerequisites, instructor profiles, registration, map

*Digital Signal Processing -- 4-day class with labs:*

### DSP System Design and Implementation

**Overview**: Today's technology provides DSP processors that can be easily used to design very sophisticated products for instrumentation, control systems, communications, and wireless systems. This course presents DSP system design and implementation using programmable signal processors. Hands-on laboratory exercises are used to present the design and implementation aspects, using hardware and software tools for system implementation. The 5 laboratory sessions follow the lectures, where participants will apply system design concepts by designing, implementing, debugging and evaluating DSP schemes.

*Digital System Design -- 4-day class with labs:*

### FPGA DSP System Design

**Overview**: This course provides an in-depth and state-of-the-art coverage of the design and FPGA-based implementation of high-performance DSP systems. After presenting FPGA architectures and design tools by Xilinx and Altera, several hands-on design labs on DSP, digital communications and video/imaging will be covered, including FFT, FIR filters, error detection/correction circuits, modem, color space converter, and DWT (Discrete Wavelet Transform). Contents: Basic DSP/Communication theory, FPGA architecture/design tools, HDL (VHDL and Verilog), DSP-specific arithmetic circuits, hardware design of digital filters, FFT circuits, error detection & correction circuits, encryption/decryption circuits, and video/imaging circuits.

*Digital Design -- 4-day class with labs:*

### VHDL for Synthesis and Verification

**Overview**: An in-depth study of VHDL methodologies, coding styles and design techniques used to efficiently synthesize and test digital hardware (ASICs and FPGAs), then VHDL structures and simulation, and finally test-bench and verification. Synthesis topics focus on mapping digital hardware structures to vendor-independent VHDL code, with do's and don'ts of coding styles. Students will learn proven coding practices that result in smaller and faster design. The Laboratory runs Synopsys's Design Analyzer and Design Compiler and Xilinx's ISE for design, synthesis and verification of a non-trivial digital subsystem with bus and control signals. Students start with simple test benches and progressively increase the level of abstraction. Students will learn how to correctly model and abstract behavior and simplify testbenches with subprograms. The final result is a transaction based, system-level, self-checking test environment.

### Come to San Jose State!

**Easy access:** class starts before most students arrive on campus, so parking in the 7th Street garage is a snap!
**Cost:** $995 per course (includes student notebook, lunches and refreshments, CDs with class notes and problem solutions for certain classes)

*Microelectronic Device & Technology -- 4-day class:*

### Device Physics and VLSI Technology

**Overview**: This course presents an introduction to the basic concepts of microelectronic structures, from the PN junction to BJT and MOSFET devices. The physics of device performance is discussed in some detail. Modern device fabrication technology is covered, including fabrication principles for semiconductor devices, crystal growth, epitaxy, lithography, scaling, and etching. Critical technologies in IC fabrication are related to the performance of the resultant devices.

*Networking Engineering -- 3-day class:*

### Sensor Network Technology

**Overview**: A sensor network is a number of sensors such as chemical, biological or solar sensors that are networked together in a certain fashion to strengthen the power of sensing. Such a network can be wired or wireless, depending on where and how the sensors are used. The applications of sensor networks can be military or civilian. In the military field (the battlefield of the future for instance) a network of sensors enables soldiers to see around corners and to sense the threat of chemical and biological weapons long before they get close enough to cause harm. Sensor networks can also be put to legions of civilian uses, such as environmental monitoring, traffic control, and health care monitoring for the elderly that allows them more freedom to move about.

The course focus is on architectures, protocols, hardware aspects, and other related issues such as scalability, fault-tolerance, and security. The basic concept is to deploy a large number of low-cost and self-powered sensor nodes that acquire and process event data, then alert users to take necessary action. A base-station monitors and controls cluster networks and chooses a cluster head (gateway) for each cluster through which the cluster data is collectively routed to the base-station. Sensor networks are constructed with a stack of five layer protocol: physical layer, data link layer and MAC sub-layer, network layer, transport layer, and application layer.

*Three-day Short Course:*

## Intelligent Control & Soft Computing – Neural Networks, Fuzzy Logic, Genetic Algorithms

- Dates: February 1-3, 2005
- Location: NASA Research Park, Moffett Field
- Instructors: **Lotfi Zadeh**, Ph.D., UC-Berkeley; **Kevin Passino**, Ph.D., Ohio State Univ; **Hamid Berenji**, Ph.D., IIS Corp.

Traditional (hard) computing methods do not provide sufficient capabilities to develop and implement intelligent systems. Soft Computing is a subfield of artificial intelligence that is tolerant of imprecision, uncertainty, and partial truth. Soft Computing and Computational Intelligence methods have provided important practical tools for constructing intelligent systems.

This course has been presented at several NASA locations including NASA Marshall and NASA Glen as recently as June 2004. At the completion of this course you will have a full understanding of the benefits of intelligent control, neural networks, fuzzy logic inference, and genetic algorithms. You will have learned significant details about their successful applications and you will have developed the necessary knowledge to design and apply these techniques to your particular applications.

**Key Topics:** Learn how to design and apply fuzzy logic and neural networks techniques -- Understand the fundamental concepts -- Gain important knowledge about recent developments -- Obtain information about available software and hardware tools -- Explore a wide range of applications

**Who Should Attend?** Engineers, technical managers, project leaders, scientists, system analysts, and others interested in fuzzy logic, neural networks and intelligent systems.

> "The Soft Computing Days seminar was fantastic! Three of us attended as a group and each of us came back with the seeds of a major soft computing project. I was so taken with Lotfi Zadeh's talk, that I went back and completely redesigned a fuzzy logic expert system for tactical asset allocation. Thanks for a great conference!"

**Cost:** $975 (includes class notes and refreshments)

**Registration and more information:** On the class website: **www.iiscorp.com/courses/**

## SCV PACE

# TUESDAY January 11

## The Job Market in the Valley and its Career Implications

| | |
|---|---|
| Speaker: | Dilip Saraf |
| Time: | dinner 6PM; presentation 7PM |
| Cost: | $15 for dinner ($10 for IEEE Members); use PayPal on website; presentation is free |
| Place: | Cadence Building 5, 2655 Seely Ave, San Jose |
| RSVP: | email j.david@ieee.org |
| Web: | www.ewh.ieee.org/r6/scv/scv_pace.html |

After getting his B. Tech from IIT, Bombay and Master's in EE from Stanford, **Dilip Saraf** worked at various organizations, first as an individual contributor and then progressing to head an engineering organization at a $2B local high-tech company. Dilip left the corporate world after some 23 years, to start his own consulting company to help organizations manage technology and get products to market faster. During his 37-year career, Dilip has worked in various capacities and industries that span from specialty chemicals to automotive to biomedical. Dilip has followed three careers, transitioning from engineering in high-tech to marketing consulting in a variety to industries and then as a business and organization consultant. Being a career counselor and an author is his fourth.

During the last three years, Dilip's focus has been career transitions for people at all levels. He has worked with nearly 2000 Silicon Valley professionals and those looking for a change in their careers and jobs at levels ranging from CEOs to hospital orderlies. He has developed numerous seminars and workshops to complement his individual coaching for those making career transitions.

Dilip holds two patents, has two publications in the *Harvard Business Review*, has led a CEO roundtable for Chief Executives on Customer Loyalty and has published: *Seven Keys to a Dream Job: A Career Nirvana Playbook*! This book received the Editor's Choice Award from its publisher. His second book, *Reinvention Through Messaging: The Write Message for the Right Job*!, which also received the Editor's Choice Award, was released in November. His third book, *Pathways to Career Nirvana: An Ultimate Success Sourcebook*, on career management is due out in January 2005. Dilip has his degrees from IIT-Bombay and Stanford, is listed in Who's Who, and is a member of IEEE.

The job market for technology professionals permanently shifted in 2001. Many forces caused this shift, some transitory and some structural. The transitory forces are notably those of economic recession, mergers and acquisitions; the structural ones are those from off shoring, continued gains in productivity, and job consolidations. Nearly one million California high-tech workers have been displaced since 2001 and over half have left high-tech or the state.

Yet despite these seismic shifts, many in engineering and high-tech professions have not changed their mindsets on how to go about their job search, career management, and their professional outlook. Most continue their careers in the ways of the past and launch their job search hoping that the familiar paradigms will serve them in this shifted landscape. To protect your career, manage a transition, and change jobs in an effective way, a new mindset is needed. The following prescription is a proven recipe for success that resulted from working with nearly 2000 professionals from the Valley who were affected by the seismic forces of job shifts that started in early 2001:

1. A resume is about tomorrow and not yesterday. Unless there is a clear and differentiated message of value creation that benefits the employer in tomorrow's economy, the employer is not going to pursue your response favorably. Challenge: How do you create a forward-looking resume that is compelling and credible?
2. With fewer jobs than available supply of qualified candidates, and its continuing trend, especially in the technology areas, how do you differentiate yourself from the crowd? Antidote: Tapping into your genius and articulating that as a value-creating mechanism for tomorrow can be a substantial differentiator. Most do not know how to discover their genius and then articulate that in a message that they can own.

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## SCV Electron Devices

# TUESDAY January 11

## Extremely Thin Fully Depleted SOI (ETSOI) Devices

Speaker: Dr. Zoran Krivokapic, Advanced Micro Devices
Time: Pizza social at 6:00pm; Presentation at 6:15pm
Place: National Semiconductor Corp. Building 31 Large Auditorium, 955 Kifer Road, Sunnyvale
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/eds/

**Zoran Krivokapic** received M.Sc. in Solid State Physics and Dr. Sc. Degree in electrical engineering from University of Ljubljana, Slovenia. He has spent 22 years in the semiconductor industry. Since 1990 he has worked for Advanced Micro Devices on various topics: technology manufacturability, lithography, topography and equipment simulation, logic and memory device research. Currently, he works in the Strategic Technology Group on the 32nm logic technologies, studying the effects of local strain and statistical fluctuations on devices and circuits, and on the 32nm node advanced memory devices like silicon nanowires and metallic nanocrystals. He has been involved with the Semiconductor Research Consortium for many years, interacting with university research on FEP processes and advanced devices. He authored more than 40 papers and holds 88 U.S. patents.

Fully depleted devices represent a choice for 45nm and beyond technology nodes. While their excellent short-channel control is widely accepted in the semiconductor community, some perceived problems are impeding large-scale experimental work. In this talk, the main processing issues for ETSOI devices will be addressed: control of silicon channel thickness, selective epitaxial growth on a very thin silicon layer, fully silicided gates, and control of the gate work function. Straining techniques to improve performance of ETSOI devices will be addressed. Due to the very thin extension regions, dopant fluctuations are becoming a serious concern and their effects will be presented for single-gate, tri-gate, and FinFET devices. Results will also be shown on gate mis-alignment for tri-gate devices and its effect on manufacturability. The talk will conclude with fluctuation effects on simple circuits built with ETSOI technologies.

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3. With increasing need for businesses to become an agile force of economic power in a shifting landscape, it is no longer enough for employees to merely showcase their technical depth in a particular subject matter. What they must learn to do is to translate that skill into unambiguous business value that is timeless in its message. Antidote: How do you translate your skills into a compelling value proposition to make you a must-hire?
4. 4. Most present their accomplishments in a task/responsibilities format in their resume. What is now required is showcasing your stories of leadership in critical assignments that changed the company's competitive position. Regardless of the title of a professional it is now needed to write such stories and yet most don't or are unable to. Antidote: Using simple tools how do you craft such stories that convey your undeniable leadership force that can change a company's fortunes, regardless of your title in a company?
5. With the future uncertain, how do technology professionals must now manage their careers using specific tools and disciplines, so that their value is constantly enhanced?
6. How do you leverage your current job momentum and reinvent yourself to change in an entirely different industry, career, or field?

Come to this informative and insightful presentation on career management and bring your challenge to the discussion to make it real to you!

# WEDNESDAY January 12

## Optical Fiber Coatings: The State-of-the-Art and the Application of a New Nano-material

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Speaker: Dr. Ephraim Suhir
Time: Seated dinner at 6:30 ($25 if reserved before Jan 10; $30 after & at door; vegetarian available)
Place: Ramada Inn, 1217 Wildwood Ave (Fwy 101 frontage road, between Lawrence Expy and Great America Pkwy), Sunnyvale
RSVP: to Janis Karklins, Karklins@pacbell.net
Web & Map: www.cpmt.org/scv

**Dr. Ephraim Suhir** is a Fellow of the IEEE, the ASME, the APS (American Physical Society) and the SPE (Society of Plastics Engineers). He has authored more than 250 technical publications (papers, book chapters, books, patents), including monographs *Structural Analysis of Microelectronic and Fiber Optic Systems*, Van-Nostrand, 1991 and *Applied Probability for Engineers and Scientists*, McGraw-Hill, 1997. Dr. Suhir has received numerous distinguished service and professional awards, including the 2004 ASME Worcester Read Warner Medal for outstanding contributions to the permanent literature of engineering, 2001 IMAPS John A. Wagnon Technical Achievement Award, 2000 IEEE Outstanding Sustained Technical Contribution Award, 2000 SPE Fred O. Conley Award, and 1999 ASME and Pi-Tau-Sigma Charles Russ Richards Memorial Award for distinguished contributions to the areas of engineering encompassed by these professional societies and laying a foundation of a new discipline "Structural Analysis in Microelectronics and Photonics". Dr. Suhir is a member of the IEEE Technical Activities Board (TAB), and Distinguished Lecturer of the IEEE CPMT Society. He has presented numerous invited and keynote talks and taught many continuing education courses worldwide.

This review addresses the state-of-the-art of the mechanics of coated optical fibers. We discuss various mechanical problems in the analysis, design and reliability evaluations of polymer-coated or metallized optical fibers, including predictive modeling (mostly analytical), mechanical behavior of hermetic and non-hermetic coatings, adhesion and strippability problems, etc. The review is based primarily on the author's research conducted during his almost twenty-year tenure with Bell Laboratories, Basic Research, Murray Hill, New Jersey. The extension part concerns the application of a newly developed nanoparticle material (NPM) as an attractive substitute for the existing optical fiber coatings. The improvement over the existing knowledge-base is two-fold: 1) understanding of the role, objectives, challenges and approaches of structural mechanics in the design and reliability evaluations of coated optical fibers and fiber coatings; and 2) development (invention) of a new nano-particle material as an attractive substitute for the existing optical fiber coatings and, in some cases, of claddings as well. Some additional applications of the NPM are also addressed and briefly discussed.

# SCV Communications Society

# THURSDAY January 13

**Broadband Wireless Technologies and Standards:**

## Advanced Broadband Wireless Standards from ETSI and Cooperation with WiMAX

First Speaker: Dr. Bernd Friedrichs, Chairman of ETSI BRAN

## IEEE Standard 802.16 for Broadband Wireless Metropolitan Area Networks

Second Speaker: Dr. Roger B. Marks, Chair of IEEE 802.16 Working Group on Broadband Wireless Access

Time: 6:15 p.m. to 8:45pm
Place: Fairmont Hotel, San Jose
Cost: Free (possible small donation to partially cover refreshment cost)
Registration: Registration is needed to get (free) WCA conference VIP pass to attend the meeting (the registration form can be downloaded from www.comsocscv.org)
RSVP (required): rsvp@comsocscv.org
Web Sites: www.comsocscv.org and www.wcai.com

*First Speaker:*

The Technical Commitee BRAN (Broadband Radio Access Networks) is responsible for the development of all types of interoperable broadband wireless systems within ETSI (European Telecommunications Standardization Institute). Generally, ETSI standards are not restricted to base specifications but include also test specifications serving as basis for certification schemes to ensure interoperability over the air between equipment from different manufacturers.

The development of HiperMAN and HiperAccess systems is performed in close co-operation with IEEE 802.16 WirelessMAN to ensure the harmonization of the base standards; and the WiMAX forum, where recently a co-operation for the joint development of test specifications was agreed, in order to benefit from the combination of the expertise of the ETSI Protocol and Testing Competence Center (PTCC) and the promotional and certification strength of WiMAX.

The mutual benefits of these harmonization and co-operation activities are outlined. The presentation also addresses some regulatory requirements (frequency bands, transmit power, power flux densities, etc.) in order to maximize the throughput of PMP systems.

*Second Speaker:*

While the world's data transmission capacities are growing at an enormous rate, relatively few users have broadband access to them. Wired solutions, including fiber, cable modems, and digital subscriber lines, have limitations that prevent ubiquitous deployment. Broadband wireless access (BWA) is an alternative that offers quick build-out at a low cost. A key issue for the success of these systems is global standardization. Within the IEEE 802 LAN/MAN Standards Committee, the 802.16 Working Group on Broadband Wireless Access, with hundreds of participants worldwide, has recently completed the WirelessMAN air interface standard for fixed wireless metropolitan area networks. Supporting industry groups, such as the WiMAX Forum, have blossomed, and the Working Group is nearing completion of the P802.16e project to extend the standard to address mobile terminals as well. This talk provides an overview of the 802.16 technology, which is based on a QoS-oriented point-to-multipoint medium access control layer and both single-carrier and OFDM/OFDMA physical layers.

**Bernd Friedrichs** joined ETSI BRAN standardization in 1998, and since 2002 he has been Chairman of the ETSI BRAN project, comprising the Hiperlan/2, HiperAccess and HiperMan areas. In particular, he contributed to the architecture of HiperAccess systems, including optimization of spectral efficiency, design of the DLC layer and appropriate testing methods (together with ETSI PTCC). Bernd also supported the harmonization between BRAN HiperAccess and IEEE 902.16 Wireless MAN-SC as well as the co-operation

between ETSI and WiMax. Since 1980, he has been with Marconi Communications in Backnang, Germany (formerly known as AEG-Telefunken, ANT Telecommunications, Bosch Telecom), now working in the R&D department of wireless access systems, in particular on the system design of broadband wireless cellular systems. He is also a lecturer at the University of Karlsruhe and he has authored a textbook on coding and information theory. He is a member of ITG, IEEE and AMS. Bernd graduated in mathematics and information science from the Technical University of Braunschweig, Germany. He received a PhD in electrical engineering from the University of Erlangen-Nürnberg, Germany. He was appointed Honorary Professor at the University of Karlsruhe, Germany.

**Roger B. Marks** is with the National Institute of Standards and Technology (NIST) in Boulder, Colorado, USA. In 1998, he initiated the effort that led to the IEEE 802.16 Working Group on Broadband Wireless Access, chairing it since inception and serving as Technical Editor of several standards. He also serves actively on the IEEE 802 Executive Committee. Marks received his A.B. in Physics in 1980 from Princeton University and his Ph.D. in Applied Physics in 1988 from Yale University. Author of over 80 publications, his awards include the 2003 Individual Governmental Vision Award from the Wireless Communications Association and a 1995 IEEE Technical Field Award. He developed the IEEE Radio and Wireless Conference and chaired it from 1996 through 1999. A Fellow of the IEEE, he has served as an IEEE Distinguished Lecturer since 1999.

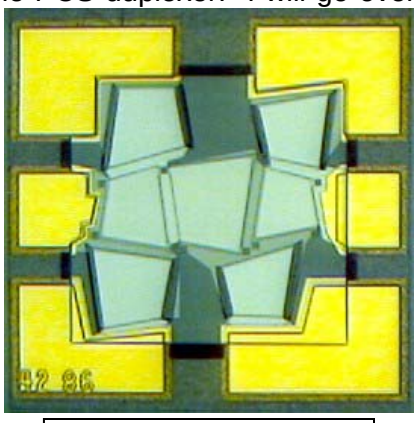
## SCV Microwave Theory & Techniques

# THURSDAY January 13

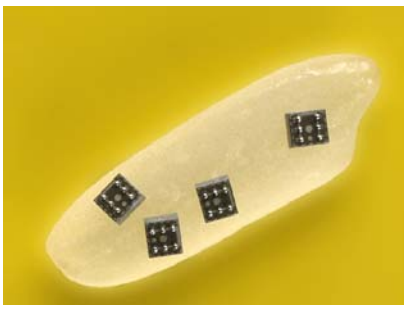
## Film Bulk Acoustic Resonators (FBARs)

Speaker: Dr. Richard Ruby, Agilent
Time: 6:30pm - Refreshments and Social Hour, 7pm - Presentation
Place: Agilent Technologies (Santa Cruz conf room), Bldg 50, 5301 Stevens Creek Blvd, Santa Clara
RSVP: none required
Web: www.mtt-scv.org/jan_mtg.html

This talk is about thin Film Bulk Acoustic Resonators, or FBARs. FBAR filters and resonators were first demonstrated in 1980 and after 8 or 9 years of research in this field, FBAR was abandoned. In 1993, a small effort was started at HP labs on FBAR resonators and filters. In 1999, Agilent published a working duplexer for the PCS CDMA band. Four years later, Agilent FBAR had made over 100M$ of revenue selling just the PCS duplexer. I will go over the physics of FBAR, and give a chronology of the development of FBAR inside HP and Agilent. Lastly, I will describe some of the "geopolitical" forces surrounding FBAR and its role in future radio architectures.



FBAR Receive Chip



FBAR GSM Filters on a grain of rice

**Rich Ruby** obtained his PhD from the University of California, Berkeley, in 1984 in the field of superconductivity. Rich then joined HP Labs and worked in the areas of e-beam lithography, X-ray lithography, advanced packaging and in 1989, superconductivity. In 1993, he began researching FBAR technology as a means for making high-Q, ultra-miniature filters for rf applications. In 1999, Rich joined Agilent (a spin-off of HP) and moved to the Wireless Semiconductor Division of Agilent as Director of Technology. Since 1993, Rich has focused on developing commercial applications for FBARs in the field of RF communications, particularly filters and duplexers for wireless handsets. In 2001, his innovations in FBAR technology lead to world-wide recognition including four industrial awards from the wireless industry, EDN Magazine's ***Innovation of the Year*** award, WIRELESS DESIGN & DEVELOPMENT Magazine's ***Technology of the Year*** award, ***Most Innovative Semiconductor Product of 2002 for Communication Applications*** from SEMICONDUCTOR INSIGHT, and Finalist for ***Product of the Year*** from Small Times Magazine (Nov. 2002) for the FBAR duplexer.

Rich has 39 patents and has given over 10 invited talks on FBAR. He was the 2001 recipient of the prestigious Barney Oliver Prize, a prize given out by Agilent Labs for "Technical contributions that demonstrate a level of creativity, innovation, technical depth, or business value that stands out from the norm, and led to a useful technical or scientific result". Rich was made a Fellow of Agilent Technologies in 2002.

## SCV Magnetics

# TUESDAY January 18

## Moore's Law and Magnetic Recording Areal Density - A Processing Perspective

Speaker: Dr. Robert E. Fontana, Jr., San Jose Research Center, Hitachi Global Storage Technologies
Time: Coffee and conversation at 7:30 PM, Presentation at 8:00 PM
Place: Komag, 1710 Automation Pkwy, San Jose
RSVP: none required
Web: www.e-grid.net/docs/0501-scv-mag.pdf

This talk examines the growth of magnetic recording storage density (disk drive capacity) from the perspective of thin film processing. Over the past 25 years, Moore's Law scaling has characterized the progress of the magnetic recording industry, with magnetic recording storage densities increasing by a factor of 10,000 to densities of 80 Gbit/in². Today, typical disk drive capacities are 40 GB with a cost of $2.00/GB. These economies of capacity and cost have been accomplished by the ability to fabricate thin film heads, the transducers that write and read magnetic transitions on a disk surface, at nano scale dimensions. The critical structures in the thin film heads are now 100 nm in length, 30 nm in thickness, and are now formed from 4 to 5 layers of thin magnetic and metallic films, each in the 1 nm to 10 nm thickness range. This talk describes the processes to form these sensor dimensions, shows that future areal density growth rates in the magnetic recording will be sustained be minimum feature processing and will be limited by the semiconductor lithography roadmap, and compares semiconductor and thin film head processing strategies for achieving smaller device sizes. The magnetic recording industry anticipates achieving 300 Gbit/in² magnetic recording densities in 5 years with minimum features of 40 nm.

**Dr. Robert E. Fontana, Jr.** is a Research Staff Member within the recording head processing function of the San Jose Research Center, Hitachi GST. He received his BS, MS and PhD degrees, all in Electrical Engineering, from the Massachusetts Institute of Technology in 1969, 1971, and 1975.

Dr. Fontana's technical activities have concentrated on developing and improving thin film processing techniques for fabricating magnetic device structures, first at Texas Instruments from 1975 to 1981 with magnetic bubbles, then from 1981 to 2002 at IBM with thin film heads, and now from 2003 at Hitachi GST with novel flux detecting sensors and nano structure fabrication with e-beam lithography. During his career Dr. Fontana has transferred research processing strategies for magnetic bubbles, magneto resistive thin film heads, spin valve giant magneto resistive thin film heads, and tunnel valve thin film heads to manufacturing applications.

Dr. Fontana has authored 37 papers on magnetic devices and processes and has 55 patents in thin film magnetic structures. He was named an IEEE Fellow in 1996 and received the IEEE Cledo Brunetti Award (excellence in the art of electronic miniaturization) in 2000 plus the IEEE Magnetics Society Achievement Award in 2005. Dr. Fontana was elected to the National Academy of Engineering (NAE) in 2002 for his contributions in magnetic device processing.

Dr. Fontana has served as President of the IEEE Magnetics Society (2001, 2002), as General Chair of the 1996 Magnetism and Magnetic Materials Conference, as General Chair of the 2004 Joint International Magnetics Conference and the Magnetism and Magnetic Materials Conference, and is serving as an NAE member on the National Research Council's (NRC) Board on Manufacturing and Engineering Design (2003-2005).

## SCV Product Safety Engineering

# TUESDAY January 18

### Gateway to a New Thinking in Energy Management - Ultracapacitors

Speaker: Bobby Maher, Maxwell Technologies
Time: Dinner from 6:00 - 6:30 PM (Free pizza and sodas), Presentation at 6:30 PM
Place: Applied Materials, Bowers Cafe, 3090 Bowers Ave, Santa Clara (map)
RSVP: Please respond to John McBain (johnmcbain@ieee.org) or Thomas Burke (Thomas.M.Burke@us.ul.com)
Web: www.ewh.ieee.org/r6/scv/pses/

Ultracapacitors are the heart of a high-power energy storage system that is finding its way into many applications as a battery replacement. The underlying technology is over 100 years old, but new discoveries in materials and processes have combined to bring the cost down. This presentation will look into the ultracapacitor technology, current applications and future opportunities. Find out what's "ultra" about ultracapacitors!

**Bobby Maher** has worked at Maxwell Technologies for 7 years, currently as Director of Technical Sales for the Boostcap product. He has a Bachelor of Science in Electrical Engineering from the University of California San Diego and also possesses an MBA. Before his employment at Maxwell Technologies, Bobby was employed as an engineer with Cubic Corp in San Diego.

## SCV Silicon Valley Consultants' Network

# TUESDAY January 18

### Peering into the Network Industry Future

Speaker: George Mattathil
Time: 7:00 PM Informal Networking; 7:15 Formal Networking; 7:30 PM Presentation
Place: New location - Girvan Inst. of Technology, 3940 Freedom Circle, Santa Clara
RSVP: not needed
Web: www.ieee-sv-consult.org/

**George Mattathil** (IEEE Senior Member) is a technologist, inventor and entrepreneur with US and international accomplishments in the telecom and data networking frontiers. Mr. Mattathil has researched strategic technology and industry trends and developed dependable high-impact insights into the future of communications infrastructure. His organizational experience includes multinational, medium and small businesses, and start-ups. He has published articles, columns and holds patents.

The Net is still the future! We are progressing through different stages of a technology-driven macroeconomic cycle, with the Internet as the key enabling technology. This macro-cycle is similar to the one in the early part of last century that was driven primarily by the automobile and the radio. The dot-com bubble marked a major turning point in this cycle. Some less noticed but equally important events have been taking place in the network industry. After a dramatic growth in the 1990s, the network industry has gone through a meltdown in the past few years. In the US alone, there was a loss over $2 trillion in market value, and over 500,000 jobs lost.

Join us to learn and discuss the causes for the downturn, dynamics of the network industry, and future possibilities.

## *SCV Power Engineering/Industry Applications*

# WEDNESDAY January 19

## Circuit Breaker Protection

Speaker: Dale Gilkey, Square-D Co.
Time: Dinner 6:00 PM, Presentation 7:00 PM
Place: Ramada Inn, 1217 Wildwood, Sunnyvale (408) 245-5330
Cost: $23 IEEE members, $25 nonmembers, $10 students
RSVP: Randal Kaufman, (650) 464-5170, rkaufman@powersmiths.com
Web: www.e-grid.net/docs/0501-scv-pesias.pdf

Our speaker will be **Dale Gilkey**, who is a Consulting Engineer Specialist for Square D Company in Northern California and Nevada. In this position he works closely with the Electrical Engineering community on project layouts, budgets, specifications, and training. Dale has been in the electrical industry for more than 25 years, beginning his career with Westinghouse Electric Corporation in 1978. There he worked in the engineering department of their switchboard/panelboard manufacturing facility for two years. Transferring to the San Francisco Bay area in 1980, he worked for Westinghouse in the Field Sales and Distribution Offices until 1990. He then worked for the local assembly builder, IEM, before joining Square D Company in 1992. Dale received his BS in Electrical Engineering at Manhattan College in New York City. There he was a member of IEEE and Eta Kappa Nu Association-the National Honor Society of Electrical Engineers.

Our subject this month is Circuit Breaker Protection. We will cover a number of topics related to Low Voltage Circuit Breakers. Here is an outline of the topics that will be covered:

Summary of Breaker Basics:
- Terminology/Definitions
- Types of Overloads

Thermal Magnetic versus Solid State (Electronic):
- Physical make up
- Coordination Curves
- Applications & Current Limiting Technology

ANSI Style Breakers versus UL Style Breakers:
- History & Equipment they are used in
- Long Short Time Withstand Ratings
- Applications

Circuit Breakers and Some NEC Code issues:
- Wire Selection
- 100% Rated Breakers
- Adjustable Trip Ratings
- Arc Fault Interrupters

Series Ratings:
- What are they?
- Where do you find Listings

Specifications:
- Gotcha's
- Proprietary Information
- Incorrect information

## SCV Engineering in Medicine and Biology

# WEDNESDAY January 19

## The Diagnostic Potential of Airway Gas Analysis Using Cavity Ringdown Spectroscopy

Speaker: Dr. Barbara Paldus, Picarro Inc.
Time: 6:15 PM - optional dinner at Stanford Hospital cafeteria; presentation at 7:30 PM
Place: Room M114 in the Stanford Hospital (see website for map)
RSVP: none required
Web: ewh.ieee.org/r6/scv/embs/pages/upcoming.html

**Barbara Paldus** is the CTO at Picarro and is responsible for technology strategy, research innovation, and business development. She leads the team that develops the company's breakthrough photonic technology. She has 14 awarded patents, 13 pending patent applications, and has published over 30 journal and conference papers, as well as two book chapters, on cavity ring-down spectroscopy (CRDS) and lasers. She has been recognized with 12 research and academic awards, most recently the Adolph Lomb Prize (2001) by the OSA. Barb received both her Ph.D. and M.S.E.E. degrees from Stanford University. She received her BS in electrical engineering and applied mathematics from the University of Waterloo, Canada.

Analysis of airway gases can potentially provide a sensitive real-time monitor of both lung and gastric functions, general physiological well-being, and of other conditions such as sedation or consciousness level while operating under anesthesia. Since different organisms metabolize substrates at different rates, often with isotopic and chiral discrimination, a species- and isotope-sensitive probe of airway gas could also be used as an early marker of bacterial or fungal infection.

Cavity Ringdown Spectroscopy (CRDS) is a novel ultra-trace gas sensing technology that is species specific, sensitive to isotopic substitution and intrinsically maintains high precision and absolute calibration. A laser is coupled into a stable optical cavity containing the gas (or liquid) to be analyzed, and is then decoupled rapidly. The decay time of the circulating power in the cavity – the "ring-down" time – is a very sensitive function of the losses within the cavity, and as such is an exceptionally good probe of absorption by the species in the cavity. Although the physical cavity length is on the order of a few tens of centimeters, effective path lengths of kilometers are routinely achieved. By continuously measuring ringdown times at the absorption peak and along the absorption feature baseline, absolute measurements may be made. The technique has the capability of monitoring biomarkers in quasi-real time at part-per-billion levels.

Barb will report on progress towards a compact, ruggedized cavity ringdown spectrometer to measure isotopes of carbon dioxide or trace amounts of ammonia and ethylene, all of which appear in the human breath. The spectrometer is currently fully contained in standard 19" rack mount enclosures and utilizes proven telecom-grade components for enhanced reliability. It is already in the field in industrial and research settings and has demonstrated a baseline noise level of $1X10^{-10}cm^{-1}/Hz^{1/2}$ over a wide range of ambient operating conditions, superior to all other competing optical spectroscopic techniques. Barb will also present results on typical instrument performance, including zero drift, precision, absolute accuracy, and linearity over the required operating concentration range for several industrial and medical applications.

# THURSDAY January 20

## A Technical Perspective on Hybrid Electric Vehicles -- Design, Technology, and Environmental Impact

Speaker: Mark Duvall, Electric Power Research Institute
Time: No-host social at 5:30 PM; Presentation at 6:15 PM; Dinner at 7:15 PM; Meeting continues at 8:00 PM
Place: Marie Callender's Restaurant - The Garden Room; 2090 Diamond Blvd, Concord, near the Concord Hilton Hotel. Call 925-827-4930 for directions.
Cost: Dinner is $22 for IEEE members, $25 for non-members
RSVP: Please make reservations by January 19, by contacting Gregg Boltz at gboltz@brwncald.com or telephone: (925) 210-2571
Web: www.ewh.ieee.org/r6/oeb/ias.html

The speaker is **Dr. Mark Duvall** of the Electric Power Research Institute. Mark has worked at EPRI for four years and is the Manager of Technology Development in Electric Transportation. In this position he is responsible for the technical development of all of EPRI's advanced transportation research programs, including battery electric, hybrid electric, and fuel cell vehicles for commercial, passenger, and transit applications.

Prior to joining EPRI, Mark held a research position at the University of California, Davis in the Hybrid Electric Vehicle Center.

Mark Duvall holds B.S and M.S. degrees in Mechanical Engineering from the University of California, Davis and a Ph.D. in Mechanical Engineering from Purdue University.

The automotive industry has entered a period of unprecedented technological development, driven by increasingly stringent emissions regulations, growing concerns about globally constrained petroleum supplies, and the looming prospect of limitations on vehicle carbon dioxide emissions. Most of this work is focused on the use of electric-drive systems to dramatically improve vehicle efficiencies and to ultimately promote sustainability and fuel diversity by enabling the use of energy carriers like electricity and hydrogen in the transportation sector.

The modern evolution of electric-drive vehicles began in the 1990s with the introduction of pure battery electric vehicles, like the General Motors EV1. The high-power electric drive technologies and other advanced components developed for these vehicles were applied to combustion engine hybrid electric vehicles, which entered the U.S. market in 1999 and show promising consumer appeal. Further technical advances could enable the development and market introduction of fuel cell hybrid electric and plug-in hybrid electric vehicles---applications which support long-term objectives to reduce the petroleum consumption and the carbon dioxide emissions of the transportation sector.

This talk will present some of the key technologies behind electric-drive vehicle design, including advanced battery systems, electric traction systems, fuel cell power devices, and hybrid-electric powertrain controls and energy management. The potential for these technologies to improve vehicle efficiency and performance, as well as their likely cost and commercialization challenges will also be discussed. Energy and environmental impacts will be discussed from a national and global perspective. The speaker will also share his experience with advanced vehicle design and the automotive development process --- including both advanced research objectives and the practical realities of collaborating with automotive manufacturers to introduce new technologies.

Questions and discussion on these and other transportation topics will be welcome throughout the evening.

## SCV Solid State Circuits

# THURSDAY January 20

## Design Considerations for Low-Power High-Sensitivity Integrated WCDMA Direct-Conversion RF Receivers

Speaker: Dr. Osama Shana'a, Maxim Integrated Products

Time: Refreshments at 6:30 PM (donation requested to partially cover food cost); presentation at 7:00 PM

Place: Cadence Building 5, 2655 Seely Ave, San Jose (map on website)

RSVP: by email to ssc_scv_rsvp@yahoogroups.com or call 408 894-2646.

Web: www.ewh.ieee.org/r6/scv/ssc/

**Osama Shana'a** received his B.Sc. degree in electrical engineering with high honors from the University of Jordan, Amman, Jordan, in 1992. In 1994 he was awarded the Fulbright Scholarship to pursue an M.S.EE degree from Portland State University, which he received in 1996. He received his Ph.D. degree in electrical engineering from Stanford University in 2000. In the summer of 1995, he joined Radio Comm. Corp., Portland OR, where he worked on the design of a fully integrated RF transceiver for ISM band applications. In the summer of 1997, he joined National Semiconductor, Santa Clara, where he led a team to work on mixed-signal megacell shareability. Since June 1998 he has been with Maxim Integrated Products, Sunnyvale, where he led many successful RF wireless designs for PCS, CDMA, WCDMA, and WLAN chipsets as well as circuits for TV tuner applications. Dr. Shana'a is a peer reviewer for many IEEE journals. He is also a member of the Eta Kappa Nu honor society, and is a senior IEEE member.

The market for wireless communications has seen a drastic change in the past few years. The era where performance comes at the expense of cost is almost over. Wireless product manufacturers are demanding high-performance RF ICs at continuously declining prices. This means higher levels of integration, higher sensitivity, smaller die area and – most importantly – lower power. In fact, most cell phone makers are now demanding superhetrodyne-like sensitivity and current consumption in any proposed RF solution, even if it saves them significantly on the bill of materials.

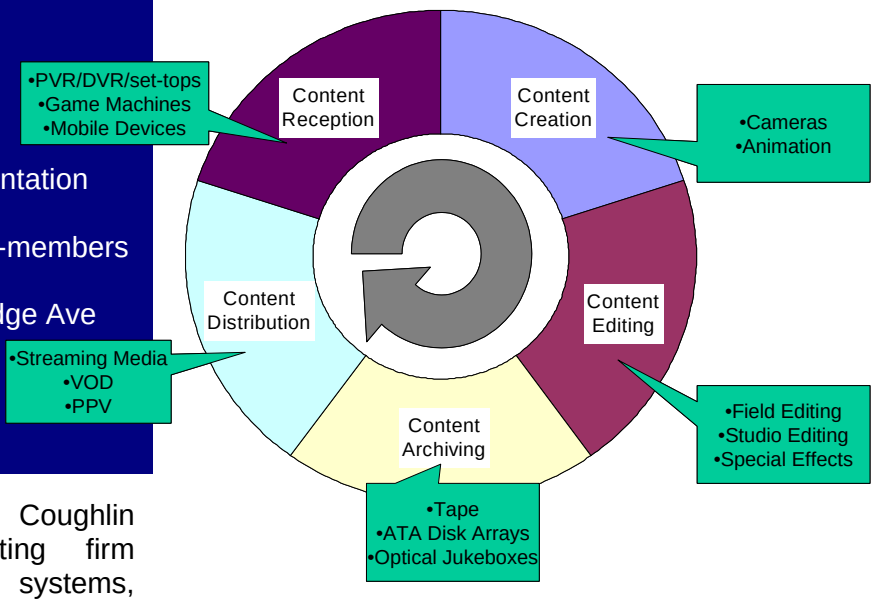
This talk will focus on design considerations for building high-performance direct conversion receivers with power consumption competitive to that of a superhet. Related design and architectural challenges will be addressed. An overview of direct-conversion receiver IC architecture for 3G WCDMA FDD radio will be presented along with some key RF system issues and integrated circuit implementation challenges. These issues include DC-offsets, LO and interferer leakage, LO phase noise, I/Q channel mismatch, baseband channel filtering, and 2nd order distortion products. The techniques will be demonstrated on a fully integrated WCDMA direct conversion receiver that achieves a 3dB NF with 30mA total current consumption.

# SCV Consumer Electronics

# TUESDAY January 25

## The Content of Storage

Speaker: Thomas M. Coughlin, President, Coughlin Associates
Time: Refreshments at 7:00 PM; presentation at 7:30 PM
Cost: $5 for members and $10 for non-members (at the door)
Place: Oak room at HP, 19447 Pruneridge Ave (Building 48), Cupertino
RSVP: by email to scv.ce@ieee.org
Web: www.ieee.org/scvce




**Thomas Coughlin** is President of Coughlin Associates, a data storage consulting firm specializing in data storage components, systems, and software used in consumer electronic, enterprise, and entertainment applications. He has over 24 years of industrial experience in data storage engineering, product development, program management, and market and technology assessment at such companies as 3M, Polaroid, Seagate Technology, Maxtor, Micropolis, Nashua Computer Products, Ampex and SyQuest. His consulting work has included clients such as Ampex, Raychem, Network Appliance, PriceWaterhouse Coopers, several start-ups, as well as Venture Capital and financial clients. Tom has over 50 articles, reports, and technical presentations to his credit and 6 granted patents.

Tom has been writing market and technology reports with Peripheral Research Corporation and Coughlin Associates for several years. His latest project is the 2005 Entertainment and Digital Media Storage Report Series committees, including overall Standards Chairman. He is a senior member of the IEEE (member for over 25 years), was publicity chairman of the 1992, 1996, 2002 and 2004 TMRC conferences and was co-chairman of the Santa Clara Valley IEEE PACE in 2004. He was also chair of the Santa Clara Valley IEEE Magnetics Society in 2002-2003.

Tom is the organizer of the annual Storage Visions Conference (www.storagevisions.com), which focuses on data storage and the digital content value chain. He is also a co-organizer with Farid Neema of the Network Storage Conference. He is a founding member of the Server Blade Trade Association and also a member of SNIA, IDEMA, ACM, APS, and AVS.

The capture, editing, archiving, distribution and reception of digital entertainment content is a huge driver for the growth of digital storage. Between 2004 and 2008 digital storage capacity for capture, editing, archiving, and distribution of digital entertainment content is expected to grow by about 290 times! Likewise the growth of digital consumer electronic "reception" devices utilizing significant digital storage for this digital content is expected to grow by at least 3 times over the same time period. The various markets for creating, archiving, distributing and using digital content constitute a "digital content value chain." The figure illustrates how each part of this value chain helps drive growth in all other parts of this value chain.

Different storage devices work best for particular applications and environments. This talk will discuss the digital storage device requirements for each of these markets including specifications and a storage hierarchy. It will also give a projection for these products vs. time. We will discuss the developing understanding of reliability requirements of disk drives for consumer applications. Critical to the growth of consumer electronic storage is an understanding of how the pricing pressure in the consumer electronics market will drive the integration of disk drives and other storage devices and their host products. Mobile storage with increasingly small storage devices will eventually lead to new interconnection technologies. The organization and recovery of digital storage content and the requirements of networking this content in the home will be discussed. Finally, the presentation will give projections for various form factor disk drives and other storage devices serving the digital content storage markets.

## SCV Reliability

# WEDNESDAY January 26

### Best of ISTFA: Developments at the Int'l Symposium for Testing and Failure Analysis

Speaker: Panel of attendees of ISTFA
Time: 6:30 PM - refreshments;
7:00 PM - presentation
Cost: none
Place: Oak room at HP, 19447 Pruneridge Avenue (Building 48), Cupertino
RSVP: none required
Web: www.e-grid.net/docs/0501-scv-rel.pdf

The International Symposium for Testing and Failure Analysis (ISTFA) provides a forum for the latest developments in wafer, chip, package, and board level test and failure analysis. The 29th ISTFA was held November 14-18, 2004, in Worcester (Boston). Information on ISTFA is available on the web at

**http://www.asminternational.org/ms/electronicdevicefailureanalysissociety/istfa/home.htm.**

The January Santa Clara Valley IEEE Reliability Society meeting will feature a panel discussion of selected papers from ISTFA. The panel is being organized by Art Rawers. We are looking for additional panel members, especially ISTFA attendees. If you are interested in helping select papers, being on the panel, leading a discussion, or contributing in another way, please e-mail us at **reliability@ieee.org**.

# THURSDAY January 27

## Long Term Trends in Packaging Technology - The International Packaging Roadmap Update

Speaker: Joe Adam, Skyworks Inc.
Time: Buffet lunch at 11:45 AM ($15 if reserved before Jan 24; $20 after & at door); vegetarian available
Place: Ramada Inn, 1217 Wildwood Ave (Fwy 101 frontage road, between Lawrence Expy and Great America Pkwy), Sunnyvale
RSVP: to John Jackson, Analog Devices, john.jackson@analog.com
Web & Map: www.cpmt.org/scv

Long-term industry trends in packaging and related research needs based on the new 2004 ITRS and NEMI Packaging Roadmaps will be reviewed. This includes key trends on package cost, thermal performance, electrical performance, size, pin count, reliability, and design. The most difficult technical challenges for the industry with emphasis on materials and infrastructure challenges will also be reviewed and the long-term market implications will be discussed. The speaker encourages audience interaction and will provide time for open discussion after the talk.

**Joe Adam** is Vice President for Strategic Marketing at Skyworks Inc. where he is responsible for RF product strategy and new business development. His primary area of interest is the evaluation, selection, and implementation of new technologies to maximize product revenue and reduce product cost. Prior to his present position he was the VP of Packaging and Test at Conexant where he was responsible for development of leading-edge manufacturing technologies for telecommunications products. He is the Co-chair for the ITRS and NEMI Packaging Roadmap Working Groups.

# WEDNESDAY February 9

## Open Wireless Architecture (OWA) for Next Generation Wireless and Mobile Communications

Speaker: Prof. Willie W. Lu, Stanford University.
Time: 6:00 p.m. (pizza & soda),
6:30 p.m. presentation
Cost: $1 donation to partially cover food cost
Place: National Semiconductor Credit Union, Bldg. 31, 955 Kifer Rd., Sunnyvale
RSVP(required): rsvp@comsocscv.org
Web: www.comsocscv.org

**Willie W. Lu** is a consulting professor at Stanford University, and a special advisor on emerging technologies and strategies to several China information and communications authorities including the Ministry of Information Industry. Prof. Lu was a member of the Technological Advisory Council of the U.S. Federal Communications Commission and a senior principal architect and vice president of Siemens and Infineon Technologies. He is also an internationally recognized senior expert in emerging wireless technologies and has been a senior technical advisor for 22 wireless communication authorities in more than 10 countries. He has guest edited about 50 special issues on emerging wireless communications in IEEE, IEICE, ACM, CIC and other major publications, and has had over 150 papers published in major professional publications. Prof. Lu is a member of the editorial board of IEEE **Spectrum** and has been technical chairman of numerous IEEE conferences including GLOBECOM'03, WCNC'02, and VTC'03, and wireless feature editor of IEEE **Communications** Magazine, IEEE **Transactions on Wireless Communications** (former J-SAC Wireless), and others. He is a frequent keynote and featured speaker at technical fora, and a prominent wireless pioneer on the worldwide basis. He is a member of IEEE, ACM, IEICE, CIC, CIE and Sigma Xi. Willie is also the founding chairman of the prestigious World Wireless Congress, Global Mobile Congress and Fourth Generation Mobile Forum (4GMF), and has been a distinguished Chinese wireless expert overseas by various Chinese authorities since 1996.

User expectations for wireless mobile communications are increasing with regard to a large variety of services and applications with different degrees of quality of service (QoS) related to delay, data rate and bit error requirements. Therefore, seamless service and applications via different access systems and technologies that maximize the use of available spectrum will be the driving forces for future developments.

Given the increasing demand for flexibility and individuality in society, the mean for the end-user might be assessed. Potentially, the value would be in the diversity of mobile applications, hidden from the complexity of the underlying communications schemes. This complexity would be absorbed into an intelligent personality management mechanism, which would learn and understand the needs of the user and control the behavior of their reconfigurable and open wireless terminals accordingly in terms of application behavior and access to support services.

This vision from the user perspective can be implemented by integration of these different evolving and emerging wireless access technologies in a common flexible and expandable platform to provide a multiplicity of possibilities for current and future services and applications to users in a single terminal. Systems of 4G mobile will mainly be characterized by a horizontal communication model, where different access technologies such as cellular, cordless, WLAN type systems, short range wireless connectivity and wired systems will be combined on a common platform to complement each other in an optimum way for different service requirements and radio environments – technically called "Converged Broadband Wireless Platform", or "Open Wireless Architecture" (OWA).

OWA will eventually become the global solution, integrating various wireless air-interfaces into one wireless open terminal where the same end equipment can flexibly work in the wireless access domain as well as in mobile cellular networks.

Based on the "Mission 2020 Plan in Wireless and Mobile Communications" in many countries, including the European Union and China, OWA has become the No.1 focused subject of research, development and strategy in the industry.

## SCV Magnetics

# TUESDAY February 15

## Spin Torque, and Nanorings

Speaker: Prof. C. L. Chien, 2005 IEEE Magnetics Society Distinguished Lecturer & Department of Physics & Astronomy, Johns Hopkins University
Time: Coffee and conversation at 7:30 PM, Presentation at 8:00
Place: Komag, 1710 Automation Pkwy, San Jose
RSVP: not required
Web: www.e-grid.net/docs/0502-scv-mag.pdf

**Chia-Ling Chien** received the B. S. degree in Physics from Tunghai University in Taiwan in 1965, and Ph. D. degree in Physics from Carnegie-Mellon University in 1972. He has been a faculty member in the Department of Physics and Astronomy at Johns Hopkins University since 1976, where he is the Jacob L. Hain Professor in Arts and Sciences. He currently directs the Material Research Science and Engineering Center on Nanostructured Materials at Johns Hopkins. His recent research focuses on magnetic nanostructures including magnetic granular solids, nanowires, multilayers, and arrays of rings and dots, and the exploration of GMR, exchange bias, half-metals, spin torque effects, Andreev reflection, and point-contact spectroscopy. He has written more than 330 journal articles and holds several patents. He is one of the ISI 1120 most cited physicists. He has served as Meeting Chair and Chair of the Advisory Committee of the Conference on Magnetism and Magnetic Materials. He has been awarded honorary professorships at Nanjing, Lanzhou, and Fudan universities in China. He has been a Fellow and the 2004 recipient of the David Adler Award of the American Physical Society.

The exploration of magnetic nanostructures in recent years has resulted in a string of discoveries such as interlayer coupling, giant magnetoresistance (GMR), exchange bias, and tunneling magnetoresistance. Some of these effects were utilized as read-heads in high-density magnetic recording and non-volatile magnetic storage only a few years after the original discovery. In this talk, I will describe two new topics in magnetic nanostructures from inception to realization to potential applications.

Since electrons have spin in addition to charge, a spin-polarized current carries angular momentum. For a large current density, the angular momentum can exert a substantial torque onto a receiving magnetic entity to excite spin waves or even to switch its magnetization. The spin torque effects are accomplished in the absence of an external magnetic field. The salient aspects of the spin torque effects in different contexts, such as switching and magnetic recording without a magnetic field, will be described.

Nanorings are small entities with special attributes of several magnetic states with unique switching characteristics. A magnetic nanoring can also support vortex state despite its very small size. The two chiralities of the vortex state can be exploited for magnetic recording purposes. Multilayered nanorings have also been proposed as vertical random access memory (VRAM) units. However, fabrication of nanorings using e-beam lithography has considerable limitations in the number of rings, ring size, and areal density. We have developed a new method with which a large number (109) of small (100 nm) rings can be fabricated with an areal density of 45 rings/$\mu m^2$. The magnetic and other characteristics of such arrays of nanorings will be described.

## SCV Solid State Circuits

# THURSDAY FEBRUARY 17

## SiGe Heterojunction Bipolar Technology and Applications

Speaker: Jayasimha Prasad, Maxim Integrated Products
Time: Refreshments at 6:30 PM (donation requested to partially cover food cost); presentation at 7:00 PM
Place: Cadence Building 5, 2655 Seely Ave, San Jose (map on website)
RSVP: by email to ssc_scv_rsvp@yahoogroups.com or call 408 894-2646.
Web: www.ewh.ieee.org/r6/scv/ssc/

**Prasad** obtained his Ph.D in Electrical Engineering from Oregon State University, Corvallis. For the past twenty years he has been engaged in developing high-speed GaAs and SiGe HBT technology. He was with Tektronix for 12 years developing GaAs-based HBT technology for high-speed oscilloscopes. As a Tektronix Fellow, he was the first in the world to demonstrate a 60GHz InGaP HBT IC technology with 28ps gate delay. During the past 9 years, he has been with National Semiconductor, Micrel Semiconductor and new Maxim Integrated Products where he has developed SiGe BiCMOS processes for wireless and fiber optic applications which have resulted in several products. Prior to the HBT work, Prasad developed E2PROM processes at National Semiconductor and contributed to VMOS processes at AMI Semiconductor. Prasad is a Distinguished Lecturer for the IEEE Electron Devices Society. He is a member of the IEEE technical committees on Compound Semiconductor Devices, Compact Modeling, and Education. He is also a member of the IEEE Technical Field Awards Committee. Prasad has served on the technical program committees for BCTM and IEDM.

In the past two decades, there has been a phenomenal growth in Silicon-Germanium (SiGe) Heterojunction Bipolar Transistor (HBT) technology. The devices have migrated from a mere laboratory curiosity to full-fledged manufacturing of highly dense integrated circuits. More and more commercial HBT circuits are being introduced into the market almost every day. The unity-gain cutoff frequency (fT) and the maximum oscillation frequency (fmax) have reached record highs. SiGe HBTs have demonstrated fT and fmax of 350GHz and 340GHz respectively. Current Mode Logic (CML) ring oscillator gate delays have hit a low of 3.3ps. What makes this technology even more interesting is that the HBT can be easily integrated into a standard CMOS flow, yielding a highly functional SiGe BiCMOS process capable of realizing analog, digital, RF and microwave circuits. These have become mainstream processes throughout the industry and they are also being offered by the well-known semiconductor foundries.

SiGe HBTs have found a presence in the least expensive consumer products, from cell phones to the most expensive gigabit communications systems. The improved performance of the devices has resulted in impressive circuit results. Dynamic frequency dividers operating at 110GHz and oscillators running at 98GHz have been reported. SiGe power amplifiers with an output power of 220 watts and power-added efficiency of 46% have been demonstrated. In high-speed communication circuits, 50Gb/s 4:1 MUX/DMUX, and 43Gb/s Clock and Data Recovery (CDR) have been shown with SiGe HBTs. This talk will focus on the physics, status of the technology, applications and future prospects of SiGe HBT technology.

# IEEE, REGION, and COUNCIL NEWS

## The IEEE Kirchhoff Award

Solicitations are made by the Kirchhoff Award Committee for nominations toward the IEEE Gustav Robert Kirchhoff Award as an IEEE Technical Field Award sponsored by the IEEE Circuits & Systems Society. The due date is January 31 of each year and the nomination form is available at www.ieee.org/portal/site/mainsite/menuitem.818c0c39e85ef176fb2275875bac26c8/index.jsp?&pName=corp_level1&path=about/awards/noms&file=kirchhoffnom.xml&xsl=generic.xsl *(whew!)*

More information about Kirchhoff can be found at www.ee.umd.edu/newcomb/Kirchhoff.html

## Proposed IEEE Life Sciences Society

Are you involved in the Life Sciences? Do you think that an awareness of LS is likely to be a part of your future and your career? If so, then we'd like you to fill out a survey being conducted by Vicky Markstein.

The proposed scope of a Life Sciences Society (LSS) is to address all areas of science that are involved with LIFE. The LSS's emphasis, however, is on the computational and engineering aspects of life sciences from both the research and the application side.

There are many organizations that have been formed in IEEE around the various components of LS – bioinformatics, molecular biology, genetics, medical informatics, all the 'omics', agriculture and food production, drug discovery, medical devices, and gene therapy to name a few – BUT at this time there is no one organization that covers the computational and engineering aspects of Life Sciences or addresses the needs of the interdisciplinary community, which is growing very fast.

The LS formation committee submitted a proposal to IEEE TAB to create a LS Society. With a large survey response, we hope to establish that there is a large community of Life Scientists that are potential IEEE members, a community that has not otherwise been attracted to our organization. At the same time, the LSS can provide a focal point for IEEE members who want to become involved with Life Science and the opportunity to do so in their own IEEE organization.

So, we invite you to fill out our survey form:

**www.csbcon.org**

Thanks!

## Fred MacKenzie, 82, of Palo Alto

**Fred MacKenzie**, a longtime Palo Alto resident and volunteer with an electronics trade convention, has died. He was 82. MacKenzie received his engineering degree at the Technical Institute of Northwestern University and moved to South California to begin his engineering career. In 1959, he moved his family to Palo Alto, working for the Stanford Research Institute until his retirement in 1987. He was a 40-year volunteer with the Western Electronics Show and Convention (WESCON), spending 28 years on the WESCON board and seven years as its chairman.

MacKenzie also chaired the IEEE's 20,000-member San Francisco Bay Area Council and received the IEEE Centennial Medal and the Don Larson Award for exceptional service to WESCON. He was an avid reader, traveler and photographer.

MacKenzie was born March 13, 1922, in Kansas City, Mo and died Nov.19 in Palo Alto. He is survived by his wife, Anne Marie Shields, his children, Richard MacKenzie of Elk Grove and Nancy Hamilton of Stockton, his step children, Leighton, Leslie and Jana Shields of Redondo Beach, two grandsons and three great -grandchildren.

In lieu of flowers, memorial contributions may be sent to the Lucile Packard Foundation for Children's Health, 770 Welch Road, Suite 350, Palo Alto, CA 94304.

# CONFERENCE CALENDAR

The **CONFERENCE CALENDAR** is a service to our IEEE Members. It outlines upcoming IEEE workshops and conferences in the Bay Area. Please submit items to the GRID Editor: editor@e-grid.net.

Conferences are also encouraged to purchase display space in the **GRID.pdf** and publicize their events on our website and in our **e-GRID** email notification service. For the Conference Publicity flyer, please download:

**www.e-grid.net/docs/conf-flyer.pdf**

January 3-6: **Consumer Communications and Networking Conference (CCNC) in Las Vegas**

The demand for networked consumer systems and devices is large – transparent networking for systems and devices for communications, entertainment, and information. Solutions include wireless, wireline, and power line networked communications environments, each with its own strengths and special challenges to overcome. In the not too distant future, we will see ad hoc networking augmented with sensors sharing networked knowledge that enables systems and devices to seamlessly interact with the Internet and wireless systems such as WiFi, 3G, and future 4G networks. A highlight this year is the topic of Digital Rights Management's Impact on Consumer Communications.

CCNC2005 is held this year at the Las Vegas Convention Center, immediately before the 2005 International CES trade show sponsored by the Consumer Electronics Association (CEA). CCNC is sponsored by the IEEE Communications Society (ComSoc). For more information: www.ieee-ccnc.org.

January 22-27: **Photonics West 2005**

**• Biomedical Optics • Optoelectronics**
**• Lasers and Applications • MOEMS-MEMS**

Photonics West has become North America's largest commercial exhibition on optics, lasers, biomedical optics, optoelectronic components, and imaging technologies. No other event covers the full range of applications and technologies. Light-powered technology is changing the world -- it's faster, cheaper, and better than the technologies that it is replacing. You don't want to miss this revolution. Located at the center of the world's hottest technology market, Silicon Valley, this event provides a unique opportunity to see new technologies with applications across a wide range of industries, production processes, and products.

With nearly 800 exhibitors, Photonics West offers a great opportunity to research vendors, establish new contacts, meet with current suppliers, and network with colleagues.

For more information and your free exhibits pass:

**spie.org/events/pwest**

February 27 – March 4: **Microlithography Symposium this year in San Jose**

SPIE's Microlithography Symposium brings practitioners of micro- and nano-lithography together in an exciting, informative, and interactive environment. It includes six Conferences tracks, 30 courses, and 130 exhibits.

Hear the latest about state-of-the-art applications and techniques, as well as emerging issues as you are presented with new challenges and alternative technologies. This variety in topic becomes all the more important as optical lithography, historically the dominant patterning technology, faces tough challenges in providing the patterning solutions for leading edge semiconductor manufacturing. Microlith'05 is held at the San Jose Convention Center.

For full information, please visit the website:

**www.spie.org/events/ml05**

March 6-10: **Embedded Systems Conference in San Francisco at Moscone Center**

The Embedded Systems Conference offers an exciting line-up of special events, 132 technical classes, 16 full day tutorials, 6 Design Seminars and over 350 exhibits. The Microprocessor Summit is a forum for major semiconductor companies to talk about their near-future plans and make new-product announcements. All of the special events are free to registered attendees and range from keynote addresses to networking opportunities and receptions, to panel discussions all designed to enrich your event experience. Discounts for teams registering together; free admission to the Exhibits. For more information:

**www.e-grid.net/conf/embed05.html**

March 21-23: **International Symposium on Quality Electronic Design at DoubleTree in San Jose**

With the theme "Design for Quality in the Era of Uncertainty," ISQED is the pioneer and leading conference dealing with design for manufacturability and quality issues, front to back. It spans three days, Monday through Wednesday, in three parallel tracks, hosting nearly 100 technical presentations, six keynote speakers, two panel discussions, workshops/tutorials and other informal meetings. The Advance Program can now be downloaded:

**www.isqed.org**