
## Chapter Meetings and Events

*June 1 – SCV LEOS* – **"Quantum Cryptography Using Autocompensating Fiber-Optic Interferometers"** – IBM work on quantum cryptography and on low-noise single-photon detectors. [more]

*June 8 – SCV ED* – **"Reliability of Low-k Dielectrics: The Importance of the Barrier Interface"** – reliability is determined by the barrier/dielectric interface - PEBO is a sealing concept. [more]

*June 9 – SCV CPMT* – **"High Density Interconnect on Flexible Substrates"** – the latest developments in high density flexible substrates for smaller form-factor packaging. [more]

*June 9 – SCV Comm* **– "Cyberspace Security Issues and Challenges"** – Web/Internet-based services must include solutions that provide security as a primary component. [more]

*June 10 – SF Comm* **– "Cyberspace Security Issues and Challenges"** – Web/Internet-based services must include solutions that provide security as a primary component. [more]

*June 11 – SCV PES/IAS* – **Summer Banquet**: Sumptuous dining and networking high above Silicon Valley [more]

*June 14 – SCV SP* – **"Fortran 95 - or Matlab meets C++"** – surprising modern language features in Fortran 90 & 95 [more]

*June 15 – SCV CNSV* – Annual Dinner: **"Positive Psychology: How To Achieve More by Separating the Science of Success from Self-Help Snake Oil"** – Come for networking, dinner, and an entertaining speaker on psychology, success and self-help [more]

*June 15 – SCV-Mag* – **"It's a Small World, But I Wouldn't Want to Paint It"** – the shift to small-form-factor disk drives. [more]

*June 16 – SCV EMB* – **"The Artificial Synapse Chip: Towards an Electronic Prosthetic Retina"** - Developing a neural interface to connect from a digital camera to individual retinal cells. [more]

*June 17 – SCV SSC* – **"MicroPower Precision Floating Gate Voltage Reference"** – A new low-power voltage reference design with high accuracy is targeted at portable systems. [more]

*June 17 – OEB IAS* – **"Bus Protection and Current Transformer Theory"** – Current theory leads to better understanding of bus faults and bus protection methods. [more]

*June 17 – OEB Comm* – **"IEEE 802.11n: Multi-Antenna Techniques for High Throughput WLANs"** – focus on smart antenna architectures for 100Mbps systems. [more]

*June 21 – SCV CAS* – **"Signal Integrity: Design, Test and Tolerance"** – SI for nanometer technology and SoC is a major challenge. [more]

*June 22 – SCV PSE*– **"Looking Forward, Looking Back"** – Profile of the Symposium this summer in Santa Clara and views about where Product Safety Engineering is going. [more]

*June 23 – SCV Rel* – **"Design and Analysis of Accelerated Reliability Tests"** - Alternatives for greatly accelerating tests and analyzing data are valuable for estimating product MTBF. [more]

*June 30 – SCV EMS* – **"The Dream – and Focusing to Make it Real"** & **"Making It - How To Go Into Business For Yourself"** - bootstrapping a new company in Silicon Valley, and making it with your own business startup. [more]

## Upcoming Conferences in the Bay Area

*July 14-16 – San Jose – IEMT'04*
IEEE Int'l **Electronics Manufacturing Technology (IEMT) Symposium** [more]
**IEMT Professional Dev't Courses** [more]

*August 9-13 – Santa Clara – EMC'04*
IEEE Int'l **Symposium on Electromagnetic Compatibility (EMC'04)** [more]
EMC'04 Workshops **(**Monday and Friday) [more]

*August 13-15 – Santa Clara – PSES'04*
IEEE First Annual **Symposium on Product Safety Engineering (PSES'04)** [more]

*August 16-19 on the Stanford University Campus:*
**IEEE Computational Systems Bioinformatics Conference** Tutorials: Monday, August 16 [more]

*August 23-27 – San Francisco – ICF'04*
Int'l **Conference on Ferrites** [more]

*Sept 1-5 – San Francisco – EMBC'04*
IEEE Int'l **Conference on Engineering in Medicine and Biology** [more]

*Sept 21-23 – Anaheim – WESCON'04*
**WESCON** and **NANOWORLD** [more]

## Tutorials, Short Courses in the Bay Area

*July 13 – San Jose – Professional Dev't Courses with IEMT'04*
Flip-Chip, Nano, Lead-Free, RF/MMIC, ... [more]

*August 9 & August 13 – Santa Clara – Tutorials with EMC'04*
Measurements, PCB Design, SI, 802.11, ... [more]

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***Other content***

# IEEE GRID

***Your Networking Partner®***

*June 2004 • Volume 51 • Number 6*





IEEE **GRID** is the monthly newsmagazine of the San Francisco Bay Area Council of the Institute of Electrical and Electronics Engineers, Inc. As a medium for both news and opinion, the editorial objectives of IEEE **GRID** are to inform readers in a timely and objective manner of newsworthy IEEE activities taking place in and around the Bay Area; to publish the official calendar of events; to report on IEEE activities of a national and international scope; and to serve as a forum for comment on areas of concern to the engineering community by publishing contributed articles, invited editorials and letters to the editor.

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## *From the editor . . .*

Summer is a time of new growth. The photo on the cover is one of my favorite "summer" places – the Eastern Sierra crest rising above Hot Creek. When snow clears from the passes, I'll be heading over there for backpacking and fishing.

And this is a time of both fond remembrance and of growth for the SF Bay Area Council and for the **GRID**. We bid farewell to Doug Davolt as he enters a second retirement after 24 years as our editor. And we move bravely forward in our shift to communicating with you using the new "tools" created by us engineers.

If you are not getting our "**e-GRID**" notification email, drop me a note and I'll get you set up. Both Members and non-members can now receive it twice a month, profiling our Chapter meetings and other events for the next 45 days.

A special "thank you" to the SCV chapter of the Computer Society, which this month donated $650 for acquiring new communications tools for the Council office. We'll add a hardware firewall, router, and VoIP box to our DSL modem, along with some new telephone equipment for Marilyn. The router has an 802.11g interface, so officers can use their WiFi-enabled laptops during meetings held in our conference room at 345 Forest Avenue.

*Paul Wesling* **editor@e-grid.net**

A hint on using the embeded links in this GRID: hover over the blue link; if you see a "+", then right-click and select "Open in Browser". Otherwise, simply click the link to move to that page.

NOTE: The PDF version of the IEEE GRID – the **GRID.pdf** – is a monthly publication and is issued a few days before the first of the month. It is not updated after that. Please refer to the Online edition and interactive calendar for the latest information: **www.e-GRID.net**

COMPUTATIONAL SYSTEMS BIOINFORMATICS

# Bioinformatics Conference

Stanford, CA • August 16–19, 2004

CSB2004

**CSB2004** is sure to be one of the key bioinformatics events in 2004, providing a broad spectrum of peer-reviewed, bioinformatics-related topics covering the breadth and depth of this dynamically evolving field. Our topic submission procedures, keynote speakers, paper and poster presentations, tutorials and social events have all been designed to cater to bioinformatics' eclectic mix of disciplines. **CSB2004** also has the lowest registration fees of any conference of its kind in the US, making it possible for everyone to attend. However, attendance is limited so please register early.

**KEYNOTE SPEAKERS:**

**Philip Green, Ph.D.**
Professor, Genome Sciences & Adjunct Professor, Computer Science and Engineering, University of Washington, Seattle

**Benoit Mandelbrot, Ph.D.**
Sterling Professor of Mathematical Sciences, Yale University, IBM Fellow Emeritus, IBM TJ Watson Research Center

**Gene Myers, Ph.D.**
Professor, Computer Science, University of California, Berkeley

**Ron Shamir, Ph.D.**
Professor, Computer Science Genetics Branch, Raymond and Beverly Sackler Chair in Bioinformatics, Tel Aviv University

**INVITED SPEAKERS:**

**Hamid Bolouri, Ph.D.**
Professor, Institute for Systems Biology

**Michael Eisen, Ph.D.**
Assistant Adjunct Professor of Genetics & Development, University of California, Berkeley, & Scientist, Life Sciences Division, Lawrence Berkeley Lab

**Jim Kent, Ph.D.**
Research Scientist, Baskin School of Engineering, University of California, Santa Cruz

**Paul S. Meltzer, M.D., Ph.D.**
Acting Chief and Senior Investigator, Genetics Branch, Head, Molecular Cytogenetics Section, National Human Genome Research Institute

**Sandy Shaw**
Vice President, Fractal Technology, Health Discovery Corp

**Stephen Wong, Ph.D., PE**
Director, HCNR Center for Bioinformatics, & Associate Professor, Department of Radiology, Harvard Medical School and Brigham & Women's Hospital

**Bioinformatics** - scientific and engineering disciplines bringing new biological discoveries to fields as varied as human health, agriculture, the environment, energy and biotechnology. Find out more at **CSB2004**

## Who should attend:

Bioinformaticists, Biologists, Computer Scientists, IT Professionals, and Engineers who want to quickly learn about the evolving field of bioinformatics.

## Location:

Held on the Stanford University campus, **CSB2004** is easily accessible to professionals living in the SF Bay Area and Silicon Valley.

***See our website for driving and parking directions.***

**Sponsored by the IEEE Computer Society with corporate support of the Hewlett-Packard Company**

***"I think the next century will be the century of complexity." ...Stephen Hawking***

For more Conference details including session titles, technical presentations, and on-line registration, please visit:

**www.e-grid.net/conf/csb.html**

**Tutorials Offered on Monday, August 16**

*(as low as $100 – includes one AM and one PM)*

MORNING SESSIONS
Introduction to Evolutionary and Functional Genomic Analysis
Tandem Mass Spectrometry in Proteomics
Use the Genome Browsers to Get the Most Out of Public Genomes
Computational Genetics: Haplotype Inference and Applications in Human Disease Gene Mapping
Intro. to Dynamic Programming & Its Applications to Bioinformatics

AFTERNOON SESSIONS
Bioinformatics: The Machine Learning Approach
Using dChip for Microarray and SNP Chip Data Analysis
Discovering Regulatory Networks from Gene Expression and Promoter Sequence
Computational Methods in Phylogenetics
From Sequence to Structure: Protein Structure Prediction

Listing of topics and instructors at

www.e-grid.net/conf/csb.html


# *World's EMC Experts Converge in Santa Clara this August*

**IEEE**
## INTERNATIONAL SYMPOSIUM ON ELECTROMAGNETIC COMPATIBILITY

**August 9-13, 2004 – Santa Clara, CA**
**Santa Clara Convention Center**

Join over 1,000 of the world's leading Electromagnetic Compatibility (EMC) engineers at the 2004 Symposium here in the Santa Clara Valley. For five full days, over August 9 to 13, EMC engineers will attend workshops and special sessions, hear technical papers presented by leaders in the industry, and view numerous experiments and demonstrations which are designed to put into practice the theory and applications learned in the technical sessions. In addition, over 200 exhibitors of EMC-related products and services will be on hand to present the latest technological advances in this industry. Engineers representing the diverse fields of telecom, automotive, and medical EMC will attend. The heart of Silicon Valley will also draw engineers working with printed circuit boards and integrated circuits. EMC design and test challenges are present across a wide range of industries.

The local Santa Clara Valley Chapter of the IEEE EMC Society organizes this symposium. Its steering committee members are from leading technology companies such as Cisco Systems, Hewlett Packard, Apple Computer, Lockheed Martin, and Underwriters Laboratories, among others. Chairman John Howard, a noted EMC Consultant, commented, "Not only will this year's symposium provide a great opportunity for engineers to attend cutting edge technical sessions, but it will also encourage the unique networking with fellow engineers that can only enhance one's career. No where else does this level of EMC technical expertise converge in one place at one time."


## SYMPOSIUM AT A GLANCE - Sessions

PCB Analysis and Design
Shielding - Signal Integrity
Coupling - Lightning Protection
Filters and Conducted Emissions
Automotive EMC - System EMC
Gasketing and Grounding
Cables and Connectors

Test Facilities, Instrumentation
Reverberation Chambers
Immunity Testing
Radio Systems Interference
Wireless Testing SAR

Measurement Techniques
Computer Modeling
Model Parameter Determination
CAD Modeling and Extraction
Modeling & Simulation Validation
Modeling for Signal Integrity

FCC and Digital Devices
Standards and Regulations

Plus Experiment Demonstrations,
Committee & Standards Meetings

**Introductory Level Workshops Offered**

- 20 workshops, plus a NARTE exam prep session and the NARTE EMC Engineer exams
- Included with full conference registration, or register for only the "workshop" day you want

Listing of topics at **www.e-grid.net/conf/emc.html**

For more information on the **Symposium**, a complete listing of **exhibitors**, and **registration forms**, please visit:

**www.e-grid.net/conf/emc.html**

Note: attendees can select from **full-day** or **full-week** registration options.

Limited **exhibit space** is still available; local exhibitors are welcome. Interested exhibitors should contact Sue Kingston at s.kingston@ieee.org for more information.

# Current Exhibitors for the 2004 EMC International Symposium

Use the registration form to receive **a free day pass** to the EMC'04 exhibits


**Exhibit Hours:**
**Tues & Wed August 10, 11 - 9:00am - 5:30pm**
**Thursday August 12th - 9:00am - 3:00pm**

**www.e-grid.net/conf/emc.html**

**(Print out and bring)**

| Exhibitors | Booth numbers |
|---|---|
| 3M Electronic Products Div. | 701 |
| 3M Electronics Markets Mtls Div. | 702 |
| A. H. Systems | 418 |
| Acemark/Cherry Clough Consulting | 705 |
| Advanced Test Equipment Rentals | 619 |
| Agilent Technologie | 824 |
| AK Stamping Co. | 710 |
| American Assoc for Lab Accreditation | 845 |
| American TCB | 944 |
| AMIC (Advanced Mtls & Integration) | 1045 |
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## SCV Lasers and Electro-Optics

# TUESDAY JUNE 1

### Quantum Cryptography Using Autocompensating Fiber-Optic Interferometers

Speaker: William Risk, Almaden Research Center, IBM
Time: Pizza Social at 7:00 PM, presentation at 8:00 PM
Place: National Semiconductor Credit Union Bldg 31, large auditorium, 955 Kifer Road, Sunnyvale
Reservations: RSVP@silicavalley.com
Web: www.silicavalley.com/

Quantum cryptography exploits fundamental principles of quantum mechanics to ensure that secure communication can be conducted over unsecured channels. Systems that use fiber-optic links operating at telecom wavelengths are now moving out of the laboratory and into practical use.

These implementations, based on interferometers that are tens of kilometers long, use Faraday mirrors to provide automatic and passive compensation for uncontrolled phase shifts caused by environmental influences. I will describe recent work at IBM to develop quantum cryptography systems based on this approach. I will also describe our current work on high-efficiency, low-noise single-photon detectors for telecom wavelengths.

William P. Risk joined the IBM Corporation in 1986 as a Research Staff Member at the Almaden Research Center in San Jose, CA after receiving his Ph.D. from Stanford University. His work at Almaden for several years was concerned with the development of compact blue-green lasers for high-density optical data storage. More recently, his technical contributions have been in the area of quantum cryptography and nanophotonics. He has authored or co-authored some 100 publications in technical journals and conference proceedings and holds fifteen patents. He is a co-author of the book **Compact Blue-Green Lasers**, published in 2003 by Cambridge University Press. Dr. Risk is a Fellow of the Optical Society of America and a member of the American Physical Society.

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## SCV Electron Devices

# TUESDAY JUNE 8

### Reliability of Low-k Dielectrics: The Importance of the Barrier Interface

Speaker: Dr. Gerald Beyer, IMEC Leuven, Belgium
Time: Pizza social at 6:00pm; Presentation at 6:15pm
Cost: Free
Place: National Semiconductor Corp. Building 31 Large Auditorium, 955 Kifer Road, Sunnyvale
RSVP: not required

The area of dielectric reliability in the Back-End-Of-Line (BEOL) process is really only as old as copper in BEOL. Some test concepts could be taken from gate oxide reliability, but the introduction of (meso) porous low-k materials required a specific approach. Fast turn-around test vehicles were developed at IMEC and validated by rigorous reliability testing. One of the most important findings is that the reliability of the integrated (meso) porous dielectric is determined by the barrier/dielectric interface. Therefore, sealing the surface of the (meso) porous dielectric is mandatory for long lifetimes. Post Etch porogen Burn Out (PEBO) is such an enabling sealing concept for (meso) porous materials.

Dr. Gerald Beyer studied chemistry at the University of Leipzig and obtained a MSc in Materials Science at Thames Polytechnic and a PhD at Imperial College, London. He joined IMEC as a post-doctoral researcher 10 years ago, working on SIMS analysis of Si-based semiconductors. He then became a process engineer for PVD of barriers and conductors, battling constantly with the step coverage of the liners. Today Gerald Beyer is the manager of the Cu/low-k program at IMEC.

# SCV Components, Packaging, & Manufacturing Technology

# WEDNESDAY JUNE 9

## High Density Interconnect on Flexible Substrates

Speaker: C. Q. Cui, Compass Technology Co (Hong Kong)
Time: 6:30 – 7:30 PM seated Dinner (optional), 7:30 – 9:00 Presentation
Cost: Dinner $25 if before June 5, $30 after & at door; vegetarian available
Payment and Map: www.cpmt.org/scv/meetings/cpmt0406.html
Location: Ramada Inn, 1217 Wildwood Ave (Fwy 101 frontage road near Lawrence Expy)
Reservations: Required for dinner (preferred for talk)
RSVP: Allen Earman, allen.m.earman@intel.com
Web Site: www.cpmt.org/scv/

Substrates with higher density are being expected, driven by reductions in device size and the increase in pin-counts, and by the growing demand for smaller form-factor packages. In this talk, the latest developments in high density flexible substrates are covered. The comparison between flexible and rigid substrates will be addressed. The discussion will cover the development activities on trace pitch and via/land diameter, semi-additive bussless products, bumped flex, multi-layer build-up substrates and embedded passives, etc, for CSP, BGA, flip chip and 3-D packages for memory, ASIC, optical and RF devices for applications in mobile and telecommunications electronics.

Cui Cheng Qiang is Chief Technology Officer for Compass Technology Co. Ltd in Hong Kong. He has over 10 years of experience in microelectronics primarily focusing on materials and reliability in wafer fabrication and IC packaging. He was a Member, Technical Staff and group leader in the advanced packaging development department, Institute of Microelectronics (IME), Singapore from 1995-2000. He worked as a research scientist at National University of Singapore from 1991-1995. Dr. Cui received his Ph.D in Chemistry from the University of Essex, UK in 1991, and M.Eng and B.Eng in electrochemical engineering from Tianjin University in 1985 and 1983. He was the recipient of the prestigious Lee Kuan Yew Fellowship in 1992. He has published over 100 papers in international journals and conferences and holds over 10 patents in the USA and UK.



July 13-16:

### IEEE Int'l Electronics Manufacturing Technology (IEMT) Symposium

San Jose Marriott - in conjunction with SEMICON/West.

The IEEE's IEMT is an international forum on electronic/ photonic/MEMS components and systems manufacturing technology, a joint effort of SEMI and the IEEE CPMT Society. It brings to Silicon Valley a unique venue for engineers and scientists with technical papers on research, development, and applications of manufacturing technology for components, assemblies, and systems. Individual sessions will deal with reliability, green manufacturing, MEMS packaging, design for manufacturing, the effects of using low k materials, wafer level and stacked die packaging, and testing.

You will learn:
- Practical solutions to current production problems
- How to meet the process challenges of the 90nm node
- The latest trends in final manufacturing technology from recognized experts
- What is new in advanced packaging, reliability, materials, and design for test

Who should attend:
- Process, equipment and materials engineers in assembly, packaging and test
- Process and product development managers

See also the six **Professional Development Courses**.

More information:
**www.e-grid.net/conf/iemt.html**

## SCV Communications

## WEDNESDAY JUNE 9

## SF Communications

## THURSDAY JUNE 10

# Cyberspace Security Issues and Challenges

Speaker: **Dr. Manu Malek,** Professor of Computer Science, Stevens Institute of Technology, IEEE Fellow, and Communications Society Distinguished Lecturer

Time: 6:00 PM (pizza & soda), 6:30 PM presentation
Fee: $1 donation to partially cover food cost
Place: National Semiconductor Credit Union, Bldg. 31, 955 Kifer Rd., Sunnyvale
RSVP: required, to rsvp@comsocscv.org
Web: www.comsocscv.org

Time: Networking at 6:00 PM (pizza & soda), Lecture at 6:30
Fee: none (donations for pizza accepted)
Place: San Francisco State University
Map: www.sfsu.edu/~parking/text/tocampus.html
RSVP: to asim@ieee.org to get room number - seating might be limited

Cyberspace is used extensively for commerce. Businesses that accept transactions via the Internet can gain a competitive edge by reaching a worldwide customer base at a relatively low cost. But the Internet poses a unique set of security issues due to its openness and ubiquity. Customers will submit information via the Web/Internet only if they are confident that their private information, such as their credit card numbers, is secure. Therefore, today's Web/Internet-based services must include solutions that provide security as a primary component in their design and deployment.

This talk will provide an overview of cyberspace security vulnerabilities, attacks, and safeguards. Some attack techniques and the corresponding defenses against them will be described. The anatomy of a specific attack will be presented. Also some techniques based on data mining will be provided to detect and even predict attacks.



Manu Malek is Industry Professor of Computer Science and Director, Certificate in CyberSecurity Program, at Stevens Institute of Technology. Prior to joining Stevens, he was a Distinguished Member of the Technical Staff at Lucent Technologies Bell Laboratories. He has more than 20 years of experience in teaching, practicing, and research in communication networks design, optimization, operations, and management. He has held various academic positions in the US and overseas, as well as technical management positions with Bellcore (now Telcordia Technologies) and AT&T Bell Laboratories.

He is the author, co-author, or editor of seven books, co-holder of two patents, and the author or co-author of over fifty published technical papers and numerous technical reports in the areas of network design, computer communications, and network operations and management.

Dr. Malek is a fellow of the IEEE, an IEEE Communications Society Distinguished Lecturer, and the founder and Editor-in-Chief of the Journal of Network and Systems Management. He earned his PhD in EE/CS from the University of California, Berkeley.

# FRIDAY JUNE 11

## Santa Clara Valley IAS/PES Summer Banquet

Time: Drinks 6:30 PM, Dinner 7:00 PM.
Place: Silicon Valley Capital Club, 50 W. San Fernando, Suite 1700, San Jose
RSVP: Randal Kaufman, (650) 464-5170, rkaufman@powersmiths.com
Cost: $38.00 IEEE members, $43.00 nonmembers

You and a companion are cordially invited to the IAS/PES Summer Banquet. Please join us for a relaxing evening with industry professionals and a beautiful view of Silicon Valley.

Our menu will include:

- Baby Spinach and Endive Salad with Candied Pecans, Gorgonzola Cheese and Roasted Pear Dressing.
- Entree Choice of Grilled Gulf Prawns with Seared Breast of Chicken Provencal or Sundried Tomato Ravioli with Baby Arugula and Wild Mushrooms.
- Dessert will be Tiramisu

Please include your Entree Choice when you make your reservation. Parking is available in the garage under the Knight Ridder building and the Capital Club will validate your ticket. Drinks are available at the Capital Club Lounge. Please RSVP early, seating is limited.

## SCV Signal Processing

# MONDAY JUNE 14

### Fortran 95 – or Matlab meets C++

Speaker: Matthew Halfant, PhD, VP Advanced Technology, Genesis Microchip, Inc
Time: 6:30PM: fast food & drinks ($1 donation),
7:00: Announcements (Jobs etc),
7:05: presentation
Place: National Semiconductor Credit Union Building (Bldg 31), 955 Kifer Rd., Sunnyvale (Near Lawrence & Central Expressways);
RSVP: Not required
Web: www.ewh.ieee.org/r6/sps/

Some years ago I upgraded a Microsoft Fortran compiler from PowerStation 1 to PowerStation 4, hoping to gain the advantage of a true 32-bit memory model. Quite unexpectedly, the upgrade took me from Fortran 77 to something called Fortran 90, and this ultimately proved far more exciting than the "mere" transition from 16 to 32 bits.

Fortran 90, and its current successor Fortran 95, breaks with the rigid formatting conventions of earlier Fortran; it introduces dynamic memory allocation, derived data types ("structs"), operator overloading, and other modern language features. Of greatest value to me personally is the array notation, which is very similar to Matlab's: this allows a natural expression for array operations, which simplifies coding and simultaneously opens the door to high-performance execution on parallel hardware.

I've chosen this topic because many of my colleagues have had no inkling of this development -- at any mention of Fortran they simply visualize the classical dialect and are understandably puzzled at my enthusiasm. This is too good to be a well-kept secret, so I wish to offer an overview of modern Fortran and illustrate, with examples from my own work, how empowering it has been for me.

Dr. Matthew Halfant has had a wide range of professional experience. He was a Post Doctoral Fellow in the Mathematics Dept. of IBM's Thomas J. Watson Research Center, taught for three years at Evergreen State College, then returned to T.J. Watson as a Research Staff Member in Computer Science. Following that he took a position as Senior Scientist, then Director of Engineering, at Bedford Computer -- the company that developed WYSIWYG page composition for typesetting long before the era of desktop publishing.

After this he spent a few years as a Research Scientist with the AI Lab at M.I.T., developing Numerical Analysis libraries in Scheme. Following that he took a high-level technology position in the Digital Typeface Division of AGFA Compugraphic, before becoming Manager of Font Technology at Apple Computer, where he led the team that launched TrueType. To avoid being "typecast", his next role was that of Architect at cc:Mail (Lotus), in which he demonstrated the power of rapid prototyping in accelerating the design of a next-generation e-mail system.

In 1995 he left Lotus to become the first hired employee at startup VMLABS, which developed the award-winning NUON DVD player, based on its proprietary media processor. As VP of Software Development, he assembled the strongest team he'd ever had the pleasure of working with. The company was bought by Genesis Microchip in 2002, which is where Dr. Halfant may currently be found.

## SCV Consultants' Network of Silicon Valley

# TUESDAY JUNE 15

## Positive Psychology: How To Achieve More by Separating the Science of Success from Self-Help Snake Oil

Speaker: Dr. Stephen J. Kraus, PhD
(Next Level Sciences)
Time: Networking at 6:30 p.m., dinner at 7:00
Place: Wyndham Ramada Inn (new location), 1217 Wildwood Ave, Sunnyvale (between Lawrence and Great America, E. of 101)
RSVP: Seating limited to 40 max; preregister to **a.rahman@ieee.org** with Membership status, choice of chicken or vegetarian
Cost: With reservations by Friday June 11: $15 (CNSV), $20 (IEEE member), $25 (non member). $5 surcharge thereafter
Web: www.ieee-sv-consult.org/

"Positive psychology" is the scientific study of happy, successful, highly achieving people, and it's one of the fastest growing fields in psychology. Success scientist and Harvard Ph.D. Stephen Kraus utilizes this research to offer proven, practical tools for achieving more, while debunking self-help snake oil and unmasking self-improvement urban legends.

In this entertaining talk, Dr. Stephen J. Kraus will explore what cutting-edge scientific research has revealed about top leaders and managers, and how this research has exposed leadership myths, self-help snake oil and self-improvement urban legends. He will also describe the 5 key characteristics of highly successful individuals and organizations, along with proven ways to perform better at each step:



- **Vision:** The Science of Clarifying What You Really Want from Your Life and Your Business
- **Strategy:** The Science of Turning Lofty Ambitions into Consistent Action
- **Belief:** The Science of Minimizing FUD (Fear, Uncertainty and Doubt)
- **Persistence:** The Science of Drive and Determination
- **Learning:** The Science of Making Course Corrections in Life

Dr. Kraus is President of peak performance consultancy Next Level Sciences, which helps individuals and organizations take their performance to the next level with science-based tools. A management consultant and executive coach, Steve has been called a combination of Tony Robbins and Mr. Spock for his scientific approach to the psychology of success. He is author of *Psychological Foundations of Success: A Harvard-Trained Scientist Separates the Science of Success from Self-Help Snake Oil*.

You can read more about Dr. Kraus on his website and sign up for his free award-winning newsletter on the REAL Science of Success at http://www.RealScienceOfSuccess.com.

Come join us on June 15 to explore the science of self help, meet new friends, explore business connections and have a fun time!

# WEDNESDAY JUNE 16

## The Artificial Synapse Chip: Towards an Electronic Prosthetic Retina

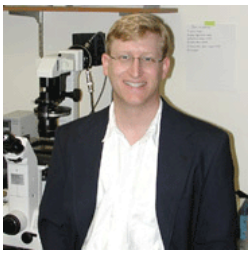
Speaker: Harvey A. Fishman, M.D., Ph.D, Stanford University School of Medicine
Dinner: 6:15 in the Stanford Hospital Cafeteria
Meeting: 7:30-8:30 in room M114 of the Medical School (see map link.)
RSVP: none (just stop by)
Map: www.med.stanford.edu/maps/sumc.html
Web: ieee.org/scv/embs

Age-related macular degeneration (AMD) is the most common form of severe and irreversible blindness in the U.S. Our research program consists of a highly interdisciplinary effort between physicians, engineers, and scientists to develop a neural interface that will connect the output from a digital camera to individual retinal cells in patients with AMD, thus bypassing injured cells.

Present prosthetic devices stimulate neurons electrically with limited spatial control and without cell type specificity. Our purpose is to explore whether neuronal growth from a specific retinal cell layer can be directed onto a chip where focal neurotransmitter or electrical stimulation would provide a more physiologic and neuron-specific transfer of information. To accomplish this, we are adapting BioMEMs technology to construct an artificial nerve connection that will be fashioned from flexible biomaterials and upon which the microcircuitry of retinal cells will be re-grown.

Specifically, neurites from retinal cells can be directed to the surface of a flexible, polymeric chip where micropatterns of growth factors cause the cells to grow toward focal stimulation sites. Cells and their neurites can be directed to grow to either (1) apertures that are connected to a microfluidics system that pulse neurotransmitters or (2) microelectrodes made from carbon nanotubes. Transmitter and electrical stimulation are shown to cause a calcium increase along the neurite and in the cell soma, indicating transmission of signal to the cell soma.

The ability to direct the growth of retinal-cell neurites and to stimulate them with a microfluidic neurotransmitter delivery system demonstrates the feasibility of a visual prosthesis interface based on direct neuronal stimulation with physiologically appropriate neurotransmitters. This neural interface represents a new paradigm in the field of electronic prosthetic retinas that are being developed worldwide. In addition to advancing the treatment of AMD, this method will have wide-reaching applications in spinal cord injuries and in the field of tissue engineering. These bioengineering technologies will help bring basic science discoveries into clinical realities and bridge the gap from bench to bedside.



**Harvey A. Fishman**, M.D., Ph.D., is Director of Ophthalmic Tissue Engineering and Retinal Prosthesis Laboratory, Department of Ophthalmology, Stanford University School of Medicine. Dr. Fishman received his Baccalaureate degree in Chemistry. He then earned a Ph.D. in Chemistry with an emphasis in Neuroscience from Stanford University working under the guidance of Professors Richard N. Zare and Richard H. Scheller. He then earned an M.D. degree from Stanford University. He completed a medical internship at St. Mary's Hospital in San Francisco and is currently a licensed Physician in the State of California. Dr. Fishman then returned to Stanford where he now holds dual positions as both the Director of Ophthalmic Tissue Engineering and Chief Ophthalmology Resident (July 2004) in the department of Ophthalmology.

Dr. Fishman's area of expertise is translational research that uses a multidisciplinary approach to develop novel therapies for blinding diseases in the eye – in particular, Age-Related Macular Degeneration. His research bridges the gaps between tissue engineering, surface science, nanofabrication, chemistry, neuroscience and retinal transplantation biology in Ophthalmology. His background in new technologies and medical science is diverse including bioMEMS, chip-based microfluidics and confocal and time-lapse microscopy, neuroscience/nerve cell regeneration and macular diseases in Ophthalmology. He has made contributions in the fields of microfluidics, laser-induced fluorescence detection, separation science, and biosensors.

*Aug. 16-19 on the Stanford University Campus:*
**IEEE Computational Systems Bioinformatics Conference** Tutorials: Monday, August 16

For more information, and to register online:

**www.e-grid.net/conf/csb.html**

## SCV/SF Magnetics

# TUESDAY JUNE 15

### It's a Small World, But I Wouldn't Want to Paint It

Speaker: Mark Green (President, TrendFOCUS)
Time: Coffee and conversation at 7:30 PM.
Presentation at 8:00
Place: Komag, 1710 Automation Parkway,
San Jose
RSVP: Not required
Web and Map: www.ewh.ieee.org/r6/scv/mag/

Mark Green is the president and founder of TrendFOCUS, a leading supplier of market intelligence for the data storage industry. Mr. Green brings extensive skill and data storage industry knowledge to TrendFOCUS, including nearly 20 years of researching the HDD and components markets. He is also president of the International Disk Drive Equipment and Materials Association (IDEMA).

The explosive unit growth experienced by the HDD industry was driven over the last 20 years largely by 3.5" drives. While that form factor will continue to be the backbone of the market for several years, emerging demand drivers will shift our industry's focus to small form factor drives. Notebook computers continue to shrink in size while demand will increase quickly due to changing user needs. This will bolster already-impressive growth rates in 2.5" and 1.8" HDDs. Handheld computing and entertainment devices, including MP3 players, portable DVRs, and multi-function mobile phones, are bursting on the scene with varied data storage requirements.

The HDD industry is responding to these huge opportunities. The supply ranks and array of available products will more than double in the next year, as established drive suppliers enter the <=1.0" HDD segments. Challenges abound, but the adaptive HDD community will find a way to not only fend off the flash threat but also to enjoy the "new era" profitably.

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## SCV Solid State Circuits

# THURSDAY JUNE 17

### MicroPower Precision Floating Gate Voltage Reference

Lecturer: Bhupendra K. Ahuja, Xicor, Inc., Milpitas
Time: Refreshments at 6:30 p.m.,
presentation at 7:00
Place: Cadence Design Systems, Bldg. 5,
2655 Seely Ave., San Jose
RSVP: ssc_scv_rsvp@yahoogroups.com

Precision Voltage references are an integral part of any data acquisition system. As opposed to using conventional Bandgap or Buried Zener techniques, Xicor engineers have come up with very high precision analog voltage references using Floating Gate Analog (FGA™) CMOS technology. By precisely setting a known charge onto an on-chip capacitor and buffering its output, a wide range of reference voltages can be programmed.

The presentation will provide details on the design techniques and process technology. FGA voltage references feature very high initial accuracy (0.2mV), very low temperature coefficient of ~1ppm/°C, excellent long term stability of less than 10ppm/1000hours, low noise, and excellent line and load regulation, at the lowest power consumption currently available (500nA typical). These voltage references enable advanced applications for precision industrial and portable systems operating at significantly higher accuracy and lower power levels than can be achieved with conventional technologies.

Bhupendra K. (BK) Ahuja received his BS-EE from the Indian Institute of Technology, Kanpur, India, in 1973 and his MS and PhD degrees in Electronics Engineering from Carleton University, Ottawa, Canada, in 1976, and 1978. He started his professional career at Bell Laboratories, Murray Hill, NJ working on the single-chip CMOS codec/filter IC design. From 1980 thru 1992 he worked at Intel Corporation as a Project Manager for advanced telecommunications products such as CODECs and MODEMs. Later he helped set up Circuit Design Methodology and also designed Clock Generation/ Distribution/Skew Control PLL circuits for the first-generation Pentium microprocessor.

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## OEB Industry Applications

# THURSDAY JUNE 17

## Bus Protection and Current Transformer Theory

Speaker: John Horak, Application Engineer, Basler Electric
Time: No-host social at 5:30 p.m.; Presentation at 6:15, Dinner at 7:15, presentation continues at 8:00 -9:00pm
Place: Marie Callender's Restaurant, The Garden Room, 2090 Diamond Blvd., Concord (near Concord Hilton Hotel) 925 827-4930 for directions.
Cost: (dinner) $22 for IEEE members; $25 for non-members
RSVP: (by noon, June 16th) Gregg Boltz, 925 210-2571 or gboltz@brwncald.com

The June 17th meeting of the IEEE Industry Applications Society, for the Oakland East Bay Area, will feature a talk by John Horak, Basler Electric, Inc. His topic is Bus Protection methods and will tie the subject into some extensive evaluation of current transformer theory and how CT operation affects the bus protection scheme.

Bus faults are uncommon, but when they occur they are very high profile events. Bus faults involve such issues as personnel safety, outage to an extensive collection of loads, may involve equipment damage that could prevent feeding these loads for an extended period or prevent generators from operating, and can cause system stability issues such as generators pulling out of step and islanding of sections of the power system. For these reasons and more, such as relay coordination concerns, a bus fault is frequently one of the highest speed tripping systems found in the protective relay business.

In an opposition to high speed, one needs a scheme that is secure against tripping for out of zone faults. One needs to be aware of some of the issues that can make systems mis-measure bus current. In order to understand the issues with CT performance in bus protection, the presentation will delve into how current transformers (CTs) work and how the CT performance affects the bus protection scheme. The presentation will begin with a detailed review of CT operation, covering the burden ratings of CTs, the ANSI C class definitions, some means of determining if a CT is prone to AC saturation during a fault, DC offset and how it arises, and CT saturation induced by DC offset current, and CT performance on high impedance differential systems during in-zone faults.

The presentation will discuss the various bus protection schemes, including various forms of high impedance bus protection using single and dual ratio CTs and the calculation of settings for such systems; low impedance current differential schemes using time overcurrent, including an analysis of the use of a with a stabilizing resistor and how this resistor is sized; interlocked feeder and bus relays; multiple restraint systems using a system similar to transformer differential relaying; and lastly, the basic overcurrent or partial differential overcurrent approach.

John Horak has been the Regional Application Engineer for Basler Electric for the California area for 7 years. Prior to joining Basler Electric John worked for Stone and Webster Engineering for 10 years, 6 of them on assignment at the System Protection offices of Public Service of Colorado. Prior to joining Stone and Webster John worked with Chevron and Houston Light and Power. John has and MSEE in Power System Studies and is a licensed professional engineer.

***SCV Solid State Circuits … continued***

After leaving Intel Dr. Ahuja worked at several smaller and startup companies (NeoMagic, Tripath and Genesis Microchip) in the Bay Area developing low-power, high-speed mixed analog chips for a PC Graphics controller, DVD decoders, an ADSL line driver, and the DVI interface for Flat Panels. From 1999 thru 2002 he worked at Exar Corp. as Sr. Director of Engineering, leading designs of Communications and Video IC products. Since 2003 he is working at Xicor, Inc. as Director of Design Engineering on high-precision analog CMOS products. Dr. Ahuja is a Senior Member of IEEE and has published numerous papers and received several patents in the area of analog IC designs.

# THURSDAY JUNE 17

## IEEE 802.11n: Multi-Antenna Techniques for High Throughput WLANs

Speaker: Dr. Sumeet Sandhu, Intel
Time: 6:30 – 7:00 PM Pizza,
7:00 – 8:30 PM Presentation
Location: Bishop Ranch 1, 6101 Bollinger Canyon Rd, San Ramon (just off I-680)
Map: www.comsoc.org/oeb/Directions.htm
Reservations: Please send a quick note by 6/16 to oeb@comsoc.org to allow us to order the pizzas
Contact: Malik Audeh - audeh@ieee.org or call (510) 305-6022
Web Site: www.comsoc.org/oeb/

Smart antennas are well-known as a means to increase the range of wireless networks. While the theoretical capacity gains provided by smart antenna systems are well understood, practical applications have lagged behind because of high costs of multiple RF chains. With increasing integration of RF circuits, costs are dropping and widespread adoption of advanced antenna technologies is imminent.

One product arena that has sparked great interest in smart antennas is the series of evolving WLAN standards such as IEEE 802.11b, 802.11a and 802.11g. In particular, IEEE Task Group 802.11n has been chartered to boost network throughput to 100 Mbps. This throughput is 4-5 times higher than the best throughputs currently available. The candidate technologies required to achieve this ambitious goal are channel bonding, burst aggregation, and MIMO (multiple input, multiple output) systems, i.e., systems with multiple antennas and multiple RF chains at both the AP and client.

We will focus on MIMO and other smart antenna architectures such as SIMO (single input, multiple output), and MISO (multiple input, single output), highlighting the differentiating feature of each architecture such as diversity gain, array gain and multiplexing gain. Multiplexing gain in particular boosts the maximum point-to-point throughput without consuming extra transmit power or signal bandwidth, and is unique to the MIMO architecture. We reveal channel measurements and simulation results substantiating the range and throughput gains realizable with practical SIMO and MIMO architectures.

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## SCV Circuits and Systems

# MONDAY JUNE 21

## Signal Integrity: Design, Test and Tolerance

Speaker: Dr. Xiaoliang Bai, Magma Design Automation
Time: 6:30 PM (networking, snacks) then talk at 7:00 PM
Place: Cadence Design Systems, Building 5. 2655 Seely Ave, San Jose
Reservations: not needed
Cost: none
Info/Web/Map: www.ewh.ieee.org/r6/scv/cas/

With emergence of nanometer technology, signal integrity is becoming a major challenge within the IC industry. With reduced noise margin and increased process variation, circuits become more vulnerable to environmental interference and manufacturing defects. In modern designs like SoCs, there are millions of noise-prone nodes needing to be analyzed, verified and tested.

In this talk, we will briefly present the following two topics:

1) A chip may fail to function due to design vulnerabilities, process variations or radiation effects. While it is expensive and difficult to achieve 100% accuracy in predicting compound noise effects, it is possible to efficiently analyze the aggregated noise impact on the overall robustness, identify the most vulnerable region of a design, and subsequently guide repairing/optimization techniques.

2) Noise effects are sensitive to operational parameters such as power supply voltage, frequency and temperature, demanding at-speed testing for AC failures. The Software-Based Self-Test (SBST) methodology, as an embedded test and validation solution, combines advantages of structural test and functional test. Not only can it test the circuit in a natural operational environment, it also can provide an opportunity for cost-effective self-test and self-repair for SoC designs.

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Dr. Xiaoliang Bai received his PhD degree in 2003 from the Department of Electrical and Computer Engineering, University of California, San Diego. He is currently a member of technical staff at Magma Design Automation, Inc. He has filed three U.S. Patent applications based on his research. His research interests include signal integrity analysis, design for test, timing analysis and circuit optimization.

### *OEB Communications … continued*

Dr. Sumeet Sandhu is a senior staff researcher in the Corporate Technology Group at Intel Corporation in Santa Clara. She holds a Ph.D. from Stanford University and a B.S and M.S from the Massachusetts Institute of Technology. Prior to Intel, she held positions at Iospan Wireless, Hughes Research Laboratories and Bell Laboratories. Her primary interests are space-time coding, stochastic signal processing and error control coding for point-to-point wireless systems, and distributed processing for cognitive networks.

We will continue our feature at the meeting of providing some networking time for those who want to stand and make a brief announcement. If you're looking for a new position, have a position to fill, want to let us know that your new start-up is ready for business or have a similar announcement, bring your resumes, job descriptions or company brochures and be prepared to make a pitch. Please keep your statements brief, so we'll have time for everyone. There will be time before and after the formal meeting for one-on-one discussions.

## SCV Product Safety Engineering

# TUESDAY JUNE 22

## Looking Forward, Looking Back

Speakers: Chapter officers
Time: 5:30 PM (networking, food and beverages) then panel at 7:00 PM
Place: Applied Materials' Bowers Café, 3090 Bowers Ave, Santa Clara
Map: www.scvemc.org/scv2003meetmap.gif
Reservations: not needed
Cost: none
RSVP: Requested (to plan for refreshments) to Julia Luke, jluke@ccsemc.com, or 408-463-0885, x112Web: ieee.org/scv/embs

This meeting is the last one before the first PSES-sponsored IEEE Symposium on Product Safety Engineering, which is being held this year in Santa Clara! The theme for the evening is "Looking Forward, Looking Back" and presentations will focus on three topics. First, an update on the Symposium – what will be happening, who will be there, with local Symposium Committee members available to answer your questions. Second, a brief history of the PSES (previously known as PSTC), back to its origins as the CSA Users' Group! Third, an interactive session on how you can have an important influence on the future of Product Safety Engineering, both locally and internationally, starting now!

Of course, there will be the usual sharing of local job openings, suggestions for future meeting topics, networking, and other useful information. Interested members of other local IEEE Society Chapters are encouraged to attend!

## *First Annual IEEE Symposium on Product Safety Engineering*

### in Santa Clara – August 13-15

While product safety has been addressed in various committees over the years, there has never been a professional society or symposium solely devoted to product safety engineering, as a discipline, until now. Attend the **first annual Product Safety Engineering Symposium** and be a part of this important new direction. It's here – locally – in Santa Clara.

This symposium addresses safety engineering for equipment and devices. It allows engineers, students and others with an interest in electrical product safety to discuss and disseminate technical information and to enhance their professional skills.

- Talk and discuss problems with vendors displaying the latest Regulatory Compliance products.
- Attend Technical Sessions, Workshops, Tutorials and Demonstrations specifically targeted to the electrical safety engineering professional.

*More information:*

**www.e-grid.net/conf/pses.html**

PSES
Product Safety Engineering Society

## *SCV Reliability*

# WEDNESDAY JUNE 23

## Design and Analysis of Accelerated Reliability Tests

Speaker: Larry George
Time: 6:30 PM – refreshments;
7:00 PM – presentation
Cost: Free (no RSVP required)
Place: HP-Cupertino Oak Room, Bldg 48. Just North of Hwy 280 (Wolfe Rd Exit) at the corner of Pruneridge Ave. and Wolfe Rd. Turn right on Pruneridge Ave and left into HP site. Follow signs to Building 48 Lobby / Oak Room.
Web link: www.ewh.ieee.org/r6/scv/rs/

This presentation describes piecewise linear failure rate functions and gives their reliability, infant mortality, and MTBF. The piecewise linear model resembles the left-hand end of the bathtub curve, which is all that is observed of reliable product demonstration tests, even accelerated ones. The piecewise linear failure rate represents infant mortality and provides enough information to estimate MTBF as well as age-specific reliability during useful lifetime even with limited test time and few failures. The presentation proposes acceleration alternatives, including one that accelerates tests greatly, continuously increasing acceleration. The presentation gives experimental designs and statistical analysis of test data, assuming the piecewise linear failure rate function and power law acceleration.

Send your test data to pstlarry@comcast.net, and he'll analyze it and present the resulting model parameters, reliability, and MTBF estimates, if he can, free of charge.

**Larry George** is a Certified Reliability Engineer and Fellow of the American Society for Quality. His education includes B.S. in Engineering, M.B.A., and M.S. and Ph.D. in industrial engineering and operations research with a minor in probability and statistics from the University of California at Berkeley. He taught for 11 years; worked for 11 years at Lawrence Livermore National Laboratory; and has worked in the real world for more than 20 years. His reliability experience comes from the communications, computers, electronics, medical, power, security, space, semiconductor, sensors, and transportation sectors.

He would like to thank those who inspired this presentation through their MTBF demonstration plans with too few samples, too short test times, zero failures, and LCLs on MTBF. Larry likes the challenge of learning everything useful from available data, without unwarranted assumptions.

# SCV Engineering Management

# WEDNESDAY JUNE 30

***The Case For Starting a Business for Yourself … and In Silicon Valley:***

**Forum: "The Dream – and Focusing to Make it Real"**

Speaker: Manu Pillai (Product Acceleration Inc.)
Time: 6:00 PM

**Presentation: "Making It - How To Go Into Business For Yourself"**

Speaker: Orin Laney (PhD Candidate, Touro U.)
Time: 7:45 PM

Time: Forum at 6:00pm, Dinner at 7:00pm, after dinner presentation at 7:45pm
Place: Wyndham Garden Hotel, 1300 Chesapeake Terrace, Sunnyvale - off Lawrence Expy/ Caribbean Drive at Hwy 237
Reservations: through website: www.ieee-scv-ems.org
Cost: (with reservations thru Friday June25): $25 (IEEE member), $30 (non member), $5 surcharge thereafter (cash or check at the door). Student IEEE members - $5.
Other information: leave message with Rich Hendrickson at (408) 203-3462

As a sequel to our outsourcing/offshoring theme of the last few months, this month the Santa Clara Valley Engineering Management Society discusses local operations at startups. The before-dinner forum is on bootstrapping a new company in Silicon Valley, highlighting the experiences of the company's founder. Following networking and a sit-down dinner, the after-dinner topic will be on making it with your own business startup.



***Before-Dinner Forum presentation* -**

## The Dream – and Focusing to Make it Real

After the tech bust, outsourcing and agonizing, it's time to use lessons learned and innovate ourselves out of this economy. The presentation will cover a year 2000 startup, its survival and its growth strategies. Topics will range from developing and refining go-to market ideas in product and services, to leveraging the engineering discipline, to initiating and managing sales, to building solid teams (outsourced/offshore and in-house/local) and focusing. We will discuss cash flow and fundraising options - with their risk-reward tradeoffs, including VC fundraising, government SBIR/ATP funds, and using your personal funding sources (and support systems needed for that). Marketing and advertising budget, in the areas of market intelligence, strategy development, channel selection and partner development will be discussed in the context of developing strategic partnerships. This will be a "gloves off" format, and attendees are encouraged to actively participate. At the end of this presentation, attendees should be able to start the process of assessing their risk tolerance, survival chances, and the fundamental value proposition … and perhaps go to the next level of building their own businesses.

Manu Pillai is CEO/Founder of Product Acceleration Inc. (PAI), started in 2000 with personal funds. PAI is based on his experiences in speeding up product design and delivery across hardware and software design, manufacturing and test. PAI has now grown into a focused Engineering Software and Services company, with its own EDA products for the FPGA implementation space, and services that include design process re-engineering as well as custom software development. PAI includes Fortune 250 clients as well as emerging startups, and continues to be funded primarily by internal growth, with assistance from specific individual investors (angel investors) as well as strategic corporate investors. Manu has a BE (EE) from University College, Dublin, Ireland, and an MBA from Santa Clara University. Prior to founding PAI, he worked with Mitsubishi Electric in India, UAE and Japan, followed and then with Solectron Corp., Fujitsu PC and Maxtor in Silicon Valley. PAI was recently

*(continued, next page …)*

featured by the San Jose Mercury News as an example of a small but growing company, and is hiring at a steady pace.

***After-Dinner presentation* -**

### Making It: How To Go Into Business For Yourself

After graduation, many engineers are surprised to discover that employers value them less for their academic prowess than for certain intangible qualities. The flip side of the coin is that employers are always surprised when the engineers who exemplify those intangible qualities are first to quit their "careers" to found new businesses. This is a talk on how to amaze your friends, surprise your enemies, and disconcert your spouse by starting a successful business of your own. In cooperation with the forum speaker, this talk will build on your new strategic knowledge and concentrate on the personal aspects and challenges required to transition from wage slave to a tough-as-nails captain of industry (and floor sweeper). Personal characteristics make a crucial difference in early stage success. Topics include preparation and risk taking, decision making, and how to test your readiness. For the skeptics among you, certain reasons not to go into business will be discussed and the relative merits of employment will be included for comparison. Several of the most important mistakes of new businesses will be developed at length.

Orin Laney became interested in electronics when he built his first crystal radio at age twelve. He was raised in the Washington DC area and received his BSEE from the University of Maryland under its Co-op Engineering Program. He later obtained his MBA from Brigham Young University and has used it to found numerous small businesses in the electronics field. Mr. Laney is currently pursuing his Ph.D BA at Touro University. A senior member of the IEEE and a member and former chair of the IEEE-USA Intellectual Property Committee, he is busier than ever, designing, researching, and making deals.

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## NEWS FROM AROUND THE BAY

### Santa Clara Valley CPMT Chapter Named "Chapter of the Year!"

Tom Tarter, chair of the Santa Clara Valley Components, Packaging and Manufacturing Technology (CPMT) Chapter, announced that the (international) CPMT Society has honored our Chapter as their "Chapter of the Year". This was based on an analysis of our activities during 2003 conducted by Ralph Russell, Chapter Development Strategic Director for the Society.

Tom has been asked to attend the CPMT Society Luncheon at the upcoming Electronic Components and Technology Conference (ECTC) in Las Vegas, on Thursday June 3rd, where he will receive a certificate and a new banner to display at our Chapter meetings.

The Society analyzes a number of factors for its 20+ Chapters worldwide, including conducting 4 technical meetings (we had more than 10), conducting one educational event (we do about 20 each year), upgrading two or more Members to Senior Member (we had 3), increasing membership (we recruited quite a few), and generating a nomination for IEEE Fellow (which we did). Tom will be at the June Chapter meeting (on June 9th) to tell you how it went.

**A recent Email to the Editor:**

There are interesting talks in the IEEE. I was wondering if there are any accommodations for individuals who are between jobs, i.e. the attendance fee (excluding dinner)? Steven

Dear Steven --

HMMMmmm - good question, and I have good news. There isn't an attendance fee for the meetings themselves -- they're free to all. The answer for the dinner itself is "No", but let me expand.

Each Chapter handles this a bit differently. I know that the CPMT Society Chapter subsidizes the dinner cost. Each dinner attendee pays about what it costs, but we do not charge the speaker or the two or three active Chapter OpCom volunteers who have to be there to run the meeting. So, this Chapter spends about $100 per meeting from its funds raised from classes. A number of other Chapters charge only a dollar or two for pizza or sandwiches.

But there is an alternative, for evening meetings: anyone can come AFTER dinner for the meeting itself, which is free. Coming about 15 minutes before the start-time of the talk gives a good opportunity for networking, which is a key benefit for someone currently unemployed, such as you.

As for the Professional Skills classes, or technical classes, a phone call to the organizer will usually get a 50% discount or some other accommodation.

We'll hope to see you at a June meeting (just after dinner!)

Best regards, Paul

## STATUS: Job Hunt for Local IEEE Members

On May 5, 2005 the SCV **PACE** (**P**rofessional **A**ctivities **C**ommittee for **E**ngineers) sent a letter to all Santa Clara Valley IEEE members describing the plight of some local unemployed engineers as well offering suggestions on how readers of the email could help by making job openings available and offering mid-career intern programs for older engineers trying to get into a new field. The letter was sent out by IEEE Headquarters under my name as local PACE co-chair. In fact the letter was the product of many individuals in the Santa Clara Valley **PACE** including Linda Fong, Nelson Zierbach, Ben Hu, Rufino Olay, and myself. Linda was the primary author.

The following day, May 6th, we had a local PACE meeting that was very well attended to discuss the results of the letter and talk about what we should do next. The response from the emailed letter was considerable. There were numerous job openings that were sent to us including intern position offers and temporary work. People also gave many editorial comments from various perspectives including those out of work for some time, those that felt that it was about time that IEEE started to say something about the situation of unemployed engineers and encouraging that much more be done, and a few entrepreneurs who said that they would like to hire local engineers but that the US regulatory and tax environment and the significant difference in expense of local vs. foreign engineers made this very difficult. It was quite clear that this was a very hot issue with strong opinions felt on all sides. We have created a location on the SCV IEEE web site where engineers can go to find these job openings – see **www.ewh.ieee.org/r6/scv/** (under NEWS). This local job listing is being offered free to companies with job, temporary work, and engineering intern openings, and over 75 jobs are now listed there.

Our local group is exploring ways to get this letter wider exposure including printing it in the Council's **GRID.pdf**. We are also discussing further steps to expose the current employment situation in the Valley, appeal to engineering managers to make positions known to us and available to our local engineers, and explore various other ways that we can work on improving the current situation and hopefully result in a net gain to the whole dynamic Silicon Valley culture. We welcome opportunities to work with other PACE groups and engineering groups to open discussion on the current situation and work to improve the employment situation for local engineers.

Tom Coughlin, SCV Chair, PACE (Professional Activities Committee for Engineers)
tom@tomcoughlin.com

IEEE Santa Clara Valley PACE Committee:
**www.ieee.org /scv/scv_pace.html**

**The email letter:**

Dear fellow IEEE members and employers,

We are sending you this letter in response to the current plight of many unemployed IEEE engineers in Silicon Valley. As you know, these past three years have been particularly difficult for those working in both hardware and software engineering fields. Engineers with strong professional integrity and years of experience are desperately looking for work. Here's what some affected engineers are saying:

"After years in Telecommunication, I was laid off. I actively pursued retraining and acquired certifications in DSP from Berkeley Extension and other accredited institutions. Unemployed American engineers like myself are told to retrain for new-technology jobs since many of the routine tech jobs are being sent offshore. However the inevitable rejection interview remarks I receive boil down to:

'You have a lot of good academic experience in DSP, but you don't have any commercial experience.'

A 3-to-6 month internship with a company would help me enormously in getting re-employed in the engineering profession."

*Nelson, IEEE member, former Telecom engineer*

"I have emailed my resume to hundreds of potential employers to no avail. While my experience matches well the job's requirements, very few hiring managers respond back. Every day is a struggle."

*Pic-Wen, IEEE member, former software manager*

**How you can help:**

1. Offer an industrial mid-career intern program. This gives a hiring manager an opportunity to find seasoned engineers to put in a few months of work on a project at a discount. Compare this to what it would take to bring in an engineer without prior industrial experience. Once retrained, a mid-career intern is able to rapidly function at a high level and thus is a very attractive permanent hire.

2. Post your job openings a-priori on our IEEE-Santa Clara Valley web site at **www.ieee.org/scv**. IEEE members looking for engineering work are open to part-time, internship or full-time employment. Please email your requests to our section webmaster: **scv_webmaster@ieee.org.**

IEEE members care enough about their careers and profession to join a professional engineering organization, attend local meetings in their fields, and subscribe to professional publications. There are no better employees for a company than IEEE members. Re-trained engineers bring a wealth of prior experience and mature judgment to their work. If you are a hiring manager, please give special consideration to resumes from your fellow IEEE members. Your help is invaluable in this time of great need!

## Consumer Electronics Chapter forms in Santa Clara Valley

The convergence of audio, video, imaging, computing, storage, communications and networking technologies found in today's CE products makes Silicon Valley area an excellent location for a Consumer Electronics Society Chapter. This area is extremely well represented by companies specializing in the variety of technologies that have already resulted in new products enriching our lives such as cell phone cameras, digital video/still cameras, recordable DVDs, digital video recorders, HDTV, MP3 players and game machines.

Borrowing from the IEEE Consumer Electronics Society's website (http://ewh.ieee.org/soc/ces/), members of the society are interested in the consumer related aspects of leisure, video and audio entertainment electronics; home information and communications systems; and interactive information and display systems. Products in these categories include video receivers, video signal generation, processing, and distribution equipment; projection TV; still and motion electronic cameras; HDTV and other advanced TV systems; personal computer hardware and software; home automation and security systems; telephones and accessories; electronic games and toys; digital audio systems; audio and video recording devices; home, mobile, and portable audio systems; cellular telephones and personal communications devices; music electronics; and home health care electronic devices.

The key goals of the CES SCV Chapter will be to:

- enable professional networking within the CE community in SCV area
- invite speakers and hold discussion panels on CE industry issues (see below)
- offer company sponsored events and seminars
- drive CE industry standards
- collaborate with other IEEE SV chapters

Here are examples of some hot topics of discussion once the chapter is established:

- Digital Rights Management
- New video codecs
- Wired and wireless home networking technologies
- Role of Media Centers/Servers
- Video on demand over broadband/cable/satellite
- What's the next hot platform for the living room

It is extremely encouraging to note that some 40 members in the Bay Area responded with their support within 24 hours of sending out the request for petitions to establish the chapter. These amazingly quick responses came from Members at such well known companies as Agere, ATI, Cisco, Intel, Microsoft, Samsung, and Sony. The breadth of interest in Consumer Electronics is evident from the roster of the 300 or so members of the CE Society in the Bay Area. These members come from highly visible companies that include Apple, ARM, Broadcom, Cadence, Conexant, Dolby, Fujitsu, Genesis, HP, Infineon, LSI Logic, Marvell, National Semiconductor, MIPS, Philips, Rambus, Seagate, SGI, Terayon, Toyota, and Xilinx among others.

For additional details, questions, or to contribute your time as an officer in the CES SCV Chapter, feel free to contact the Chair of the Society Abhi Dugar at abhidugar@ieee.org.

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Other new Chapters that have recently been formed:

**Education**
**Nanotechnology**

We'll try to publish information about each of these new Chapters in coming issues.

## OEB ComSoc Chapter, Berkeley Student Chapter Gather for West Oakland Middle School Project

On the morning of Saturday, May 8, 2004, members of the IEEE Oakland East Bay (OEB) ComSoc and the UC Berkeley student chapter got together at the Prescott-Joseph Community Center in West Oakland to celebrate the completion of the Bridging the Digital Divide (BDD) project with the DUSTY staff, volunteers, and students.

The project had its genesis over a year ago, when the OEB ComSoc chapter (www.comsoc.org/oeb/) as part of its Education and Community outreach decided to sponsor and fund a project that would enable EE students to complement their classroom learning with hands-on experience bringing computer and networking technology to underserved schools and community groups in the local area. The project was enthusiastically received by undergraduate students of the IEEE chapter at UC Berkeley (ieee.eecs.berkeley.edu/). After an extensive search among local school administrations and community groups, the BDD project team decided to work with DUSTY.

DUSTY (Digital Underground Story Telling for Youth - www.oaklanddusty.org/) is an after-school literacy and technology program in West Oakland for elementary and middle-school kids. Kids come to DUSTY generally from 3:00 until 6:00 PM. They have snacks; engage in activities geared toward exercising reading and writing skills, character and community building, creative expression, and technology skill development, and get help with homework. The central semester-long project at DUSTY is a “Digital Story”, a kind of movie-making process that begins with a written story and evolves into a multi-media video integrating various kinds of imagery, music, text and sound. The students work on computers to create their own Digital Stories, using Adobe PhotoShop, Adobe Premiere, and iMovie. At the end of each semester, the students' stories are shown at the Parkway Theatre in downtown Oakland.

DUSTY is a joint project developed by the Prescott-Joseph Center for Community Enhancement and the Graduate School of Education at the University of California, Berkeley and involves an entire community of people: professors, undergrads, grad students and alumni from UC Berkeley, Oakland community members, parents and kids.

The IEEE students, under the guidance of IEEE OEB ComSoc members, contributed to the DUSTY community by enhancing the networking in the video lab and upgrading video capturing and editing platforms. The networking improvements included replacement of hubs with managed switches, labeling and organization of network connections, partitioning into VLANs, and configuration of firewall security. The platform upgrades included additional local memory for editing performance and network storage for backup. The successful completion of the project provided a practical learning experience for the EE students and enhanced network performance for the DUSTY program.

The BDD project involved a number of groups coming together in a joint effort at both learning and community empowerment.

Submitted by Christopher Flores
Educational Liaison for the OEB ComSoc Chapter

Kedar Shah (UCB) explaining enhancements in DUSTY Lab.

IEEE and DUSTY groups (L-R): Christopher Flores (OEB), Prof Glynda Hull (DUSTY), David Lin, Vincent Liu, Devang Parekh, Rian Whittle, Vikram Savani, Jason Bayer (all UCB), Malik Audeh (OEB), Kedar Shah UCB), Philip Godoy (UCB), Suresh Bazaj (OEB), David Keenan (DUSTY), Prof Shyam Parekh (UCB).

# CONFERENCE CALENDAR

July 13-16: **IEEE International Electronics Manufacturing Technology Symposium in San Jose**

The IEEE's IEMT is an international forum on electronic/photonic/MEMS components and systems manufacturing technology, a joint effort of SEMI and the IEEE's CPMT Society. It brings to Silicon Valley a unique venue for engineers and scientists with technical papers on research, development, and applications of manufacturing technology for components, assemblies, and systems. Individual sessions will deal with reliability, green manufacturing, MEMS packaging, design for manufacturing, the effects of using low k materials, wafer level and stacked die packaging, and testing.
For registration information, an Advance Program and a listing of the Professional Development Courses:
www.e-grid.net/conf/iemt.html

Aug. 9-10: **Workshop on Memory Design and Testing will be in San Jose**

The workshop (MTDT'04) covers all aspects of memory design, process technologies and testability related topics, such as memory circuit designs, cell structures, fabrication processes, design architectures and related testing and verification methods for SRAM, DRAM, Flash and non-volatile memories, EPROM, EEPROM, embedded memories, logic-enhanced and FIFO memories, 3-D memories, and content addressable memories. For more information, contact Rochit Raysuman, 408 727 2222, r.rajsuman@advantest-ard.com

Aug 13-15: **IEEE Symposium on Product Safety Engineering Comes to Santa Clara**

This symposium addresses safety engineering for equipment and devices. It will allow engineers, students and others with an interest in electrical product safety to discuss and disseminate technical information and enhance their professional skills. Talk and discuss problems with vendors displaying the latest Regulatory Compliance products. Attend Technical Sessions, Workshops, Tutorials and Demonstrations specifically targeted to the electrical safety engineering professional.
For registration information, see the website:
**www.e-grid.net/conf/pses.html**

Aug. 16-19: **IEEE Computational Systems Bioinformatics comes to Stanford in August**

The IEEE Computational Systems Bioinformatics (CSB2004) meeting will be one of the important bioinformatics events in 2004 and will provide a broad spectrum across the bioinformatics field to ensure that this conference works for you. Our submission procedures, keynote speakers, paper and poster presentations, tutorials and social events have all been designed to cater to bioinformatics' eclectic mix of disciplines. CSB2004 has the lowest registration fees of any conference of its kind worldwide to make it possible for everyone to attend. And this year it is in our own "back yard."

The tutorials will be given on Monday, August 16, prior to the CSB2004 meeting. The purpose of the tutorial program is to provide participants with lectures and demos on either well-established or new "cutting-edge" topics relevant to the bioinformatics field. These offer participants the opportunity to learn about new areas of bioinformatics research, get an introduction to important established topics, and/or develop higher skill levels in areas for which they are already knowledgeable.

For more information, and to register online:
conference.computers.org/bioinformatics

The **CONFERENCE CALENDAR** is a service to our IEEE Members. It outlines upcoming IEEE workshops and conferences in the Bay Area. Please submit items to the GRID Editor: editor@e-grid.net.

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