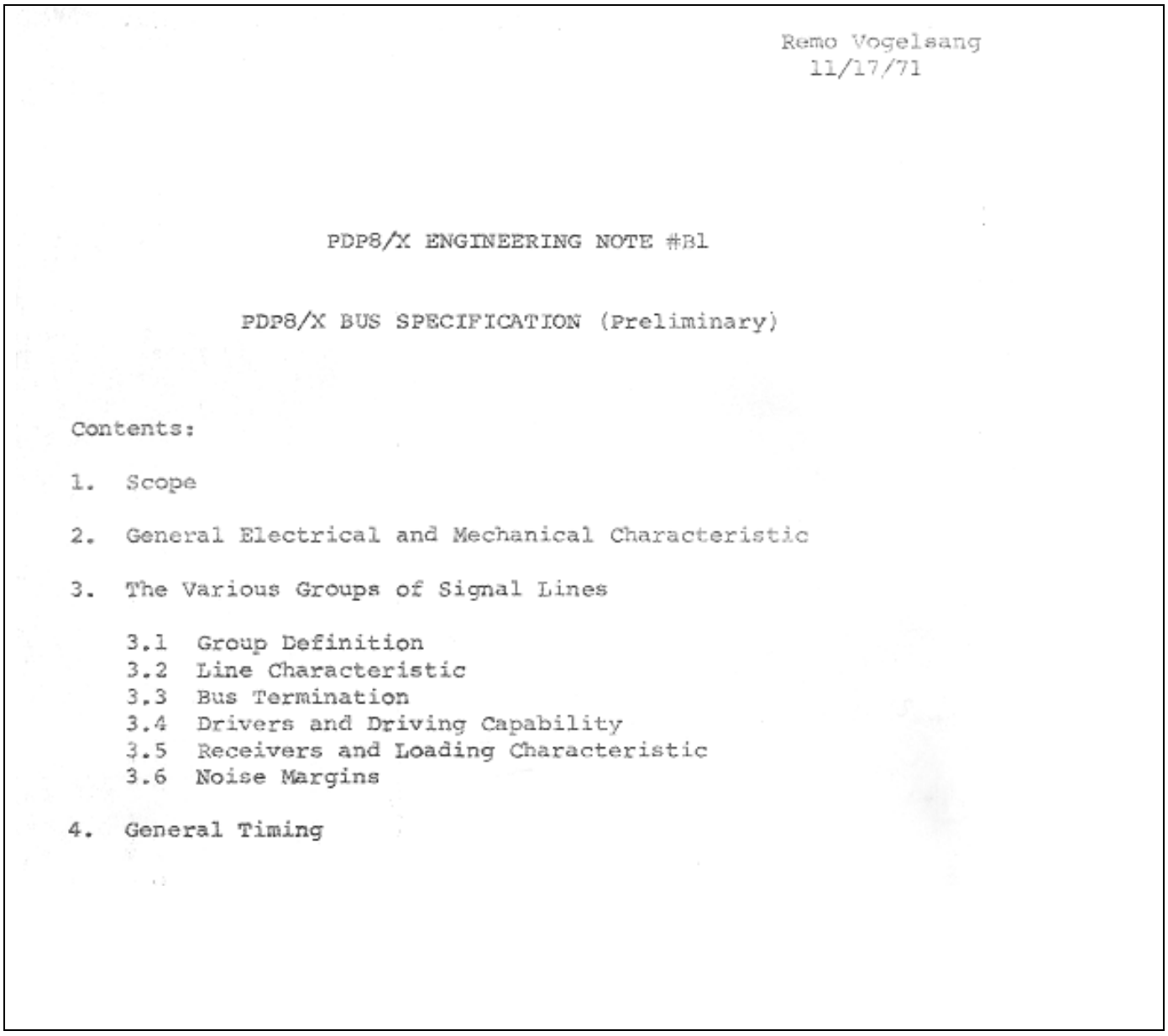
X-BUS *pioneering the Q-bus (also known as the LSI-11 Bus)*

Based on first-hand insights gained on several visits during 1971 at Los Angeles based North American Rockwell (now Rockwell International) semiconductor division's microcomputer production, I laid down a preliminary specification of a bus system employing address and data multiplexing, compatible with integrated circuit packaging. Its implications in the context of a conceivable future PDP-8 system were treated in broad scope in a set of Engineering Notes

#S1	*System Goals*	*Remo Vogelsang*	*21.12.71*
#B1	*Bus Specification*	*Remo Vogelsang*	*17.11.71*
#M1	*Module Types*	*Remo Vogelsang*	*24.11.71*
#M2	*Mechanical Packaging Concepts*	*Remo Vogelsang*	*15.12.71*
#OP1	*Compatible "OMNIBUS" Options*	*Bob Reagan / R.V.*	*14.02.72*
#OP2	*Implementing "OMNIBUS" Data Break*	*Louis Klotz*	*14.02.72*

By accidentally coining the conceivable vehicle for an address/data-multiplexed bus system a PDP-8/X, I brought out a not yet bygone acrimony still straining some people in management at that time. I got aware only little by little of the hapless events running under the famous project X shortly before I had joined DEC. Ironically I was sort of filling out a void which had opened then.



Remo Vogelsang
11/17/71

PDP8/X ENGINEERING NOTE #B1

PDP8/X BUS SPECIFICATION (Preliminary)

Contents:

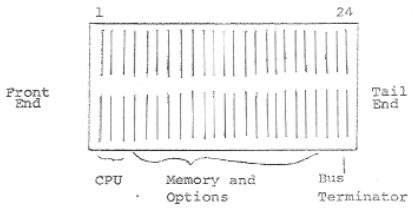
1. Scope:

It is the purpose of this specification to provide a description of the mechanical and electrical characteristic of the XBUS. This document reflects the present state of the development regarding the XBUS and is subject to change. It is most important for engineers being involved in the design or the review of the PDP8/X to fully understand the philosophy and implementation of the XBUS as outlined in this specification.

2. General Electrical and Mechanical Characteristic:

2.1 General Scheme:

The XBUS consists of an etched board with six H8Ø3 Module Sockets soldered to the board. The pin assignment is the same on all connectors (similar as the OMNIBUS).



The CPU has to be located at the front end of the bus and the BUS TERMINATOR at the tail end. Memory options and I/O options can plug anywhere in between.

It is an important characteristic of the XBUS that the electrical "length" is defined only by the electrical properties of one XBUS, regardless of any bus expansion.

2.2 BUS SCHEDULE

	A1	A2	B1	B2
A	T.P.	+5V	T.P.	+15V
B	T.P.	−5V	T.P.	−15V
C	GND	GND	GND	GND
D	TCØ	TC2	STROBE	INT REQ
E	TC1	BLANK	NOT LAST	BRK REQ
F	GND	GND	GND	GND
H	INIT	SW	DONE	POWER OK
J	RESØ	RES 1	RES 2	RES 3
K	GND	GND	GND	GND
L	EBØ	EB2	CØ	C2
M	EB1	EX	C1	C3
N	GND	GND	GND	GND
P	BØ	B3	B6	B9
R	B1	B4	B7	B10
S	B2	B5	B8	B11
T	GND	GND	GND	GND
U	~~+5V~~ −12V	T.P.	−15V	T.P.
V	~~+12V~~ +12V	T.P.	+15V	T.P.

Total number of available signal lines = 36

2.3 Mechanical and Electrical Properties

Length:	12 inches (24 slots)
Width:	5¾ inches (double width)
Prop. Delay Time:	10 ns Typ.
Time Skew Between any Lines:	5 ns. max.
Capacitance to Gnd.:	100 pf typ.
Characteristic Impedance:	100 ohm typ.
Number of Signal Lines:	36
Number of Test Points:	8
Number of Ground Lines:	20
Number of Power Lines:	8

3. The Various Groups of Signal Lines

Different functions on the XBUS call for different characteristics of drivers, receivers, terminators, etc. The electrical characteristic can be best described by breaking down the 36 signal lines onto five distinct groups.

3.1 Group Definition

3.1.1 Group #1: Bidirectional signal lines for TRI-STATE drivers.

BØ....B11	Bus Lines	(high true)
EBØ...EB2	Extended Bus Lines	(high true)
EX	Extension	(high true)
CØ....C3	Control Lines	(high true)

3.1.2 Group #2: General timing signal lines with Totem-Pole drivers; direction out.

TCØ...TC2	Time Count	(high true)
BLANK	Blank Pulse	(high true)
INIT	Initialize	(high true)

3.1.3 Group #3: Bidirectional signal lines for open emitter drivers.

STROBE	Bus Strobe	(high true)
DONE	Done Pulse	(high true)

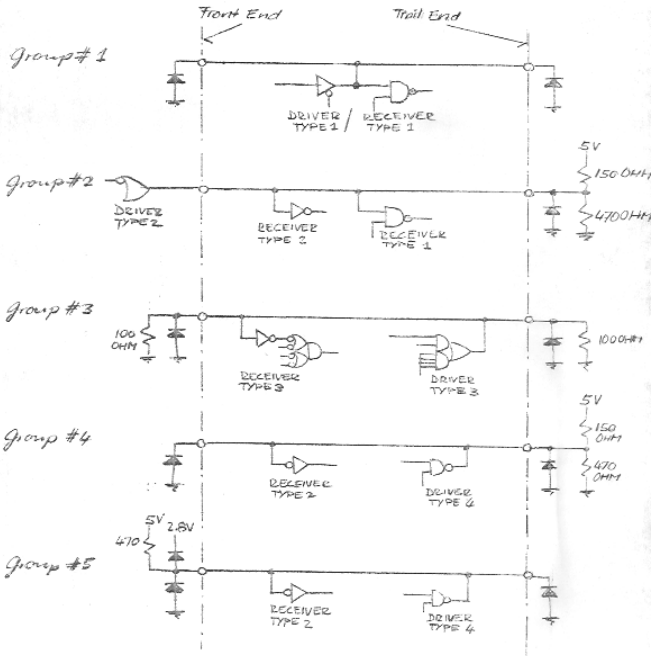
3.1.4 Group #4: One directional and bidirectional signal lines for open collector drivers.

NOT LAST	Not Last Transfer	(low true)
INT RQST	Interrupt Request	(low true)
BRK RQST	Break Request	(low true)

3.1.5 Group #5: Miscellaneous

$\overline{\text{POWER OK}}$	Power Not OK	(low true)
SW	Switch	(low true)
RESØ..RES1	Reserve	

3.2 Line Characteristic



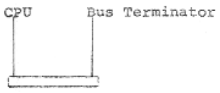
3.3 Bus Termination:

3.3.1 Front End: The termination hardware on the front end is located on any of the CPU boards. The clamp diodes required may be contained in IC gates. Note that the CPU boards have to be installed at the front end of the XBUS.

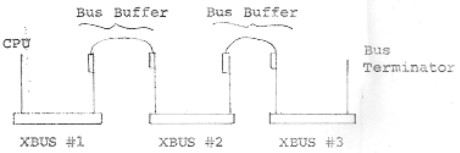
3.3.2 Tail End: All the required termination hardware for the tail end has to be contained on the "Terminator Board" which has to be installed always in the last slot of the XBUS.

3.3.3 Bus Extension: In order to extend the XBUS beyond the 24 slot length, a "Bus Buffer" is required. This "Bus Buffer" completely isolates one bus from another electrically. It replaces the "Terminator Board" on XBUS #1 and the drivers and receivers of the CPU on XBUS #2.

Single XBUS:



Multiple XBUS:



3.4 Drivers and Driving Capability

3.4.1 Driver Types

Driver Type	Location on XBUS	Group Used	Circuit Used	Notes
1	Anywhere	1	DM 8093 DM 8094 DM 8551	Tristate
2	Front End Only	2	DEC 74H40	Totem
3	Anywhere	3	8T13 (Signetics)	Open Emitter
4	Anywhere	4 5	DEC 8881 DEC 8881	Open Collector

3.4.2 Driving Capability (Operating range 0°C to 55°C)

Circuit	Driving Capability/Leakage Respect.		Notes
	Low State	High State	
DM 8093	16 mA at 0.4V	-2.4 mA at 2.4V	
DM 8094	16 mA at 0.4V	-2.4 mA at 2.4V	
DM 8551	16 mA at 0.4V	-2.4 mA at 2.4V	
S/N 8710	32 mA at 0.4V	-5.2 mA at 2.6V	
DEC 74H40	60 mA at 0.4V	-1.5 mA at 2.4V	
DEC 8881	16 mA at 0.4V 50 mA at 0.8V	-25 uA at 3.5V	
8T13	.7 mV at 0V	-75 mA at 2.6V	

3.5 Receivers and Loading Characteristic

3.5.1 Receiver Types

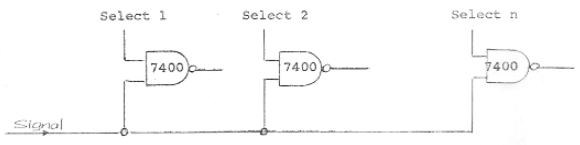
Receiver	Location	Group	Circuit Used	Notes
1	Anywhere	1,2	Any of the DEC 74XX or DEC 74HXX series circuits with 2-input-minimum positive AND or NAND configuration.	Regular TTL input with applied "Load Relief Technique" if possible
2	Anywhere	2,4,5	Any of the DEC 74XX or DEC 74HXX series circuits.	Regular TTL input
3	Anywhere	3	8T14(Signetics)	High input impedance and hysteresi

3.5.2 Loading Characteristic
(Operating range 0°C to 55°C)

Circuit	Input Loading Characteristic		Notes
	Low State	High State	
DEC 74XX	-1.6mA at 0.4V	40 uA at 2.4V	
DEC 74HXX	-2.0mA at 0.4V	50 uA at 2.4V	
8T14	-40uA at 0V	0.17 mA at 3.8V	

3.5.3 Load Relief Technique

The essence of this technique is that the option, device or field select network provides the "hold off" current for a receiver to relieve bus loading. This technique should be used interfacing to XBUS whenever it is possible.



Load Current

Assumption: The circuits have multi-emitter inputs.
Only one SELECT line is enabled at one time.

Resulting Load Current: SIGNAL LOW → -1.6 mA at 0.4V
└ nominal load per gate input

SIGNAL HIGH n * 40 uA at 2.4V
└ nominal leakage per gate input
└ number of gates

3.6 Noise Margins

The following table shows the guaranteed DC noise margins of all the used combination of drivers and receivers assuming the drivers are loaded within specification. (Operating range 0°C to 55°C)

Driver Type \ Receiver Type	Logic State	1	2	3
1	High	0.4V	——	——
	Low	0.4V		
2	High	0.4V	0.4V	——
	Low	0.4V	0.4V	
3	High	——	——	0.9V
	Low			0.7V
4	High	——	1.5V	——
	Low		0.3V	

4. General Timing:

4.1 General

The XBUS is a DYNAMIC bus. The information to be transferred remains on the bus only for the time necessary to make a transfer. After the transfer the bus is "floating" (TRISTATE drivers are being used) until the next transfer takes place. This scheme lends itself effectively for a timeshared, asynchronous operation.

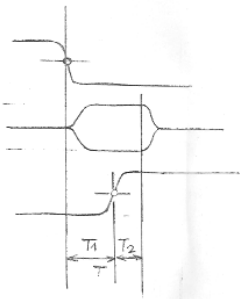
Most of the XBUS lines operate according to this scheme. Exempt are some of the timing and control signals.

4.2 Typical Timing Diagram

Transfer Ready
(Internal to a Device)

Bus Signals
(BØ...11, etc.)

Strobe or Done

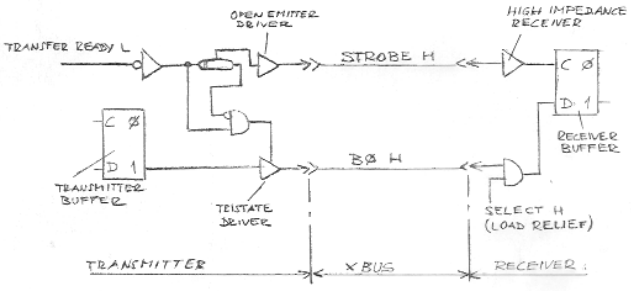


T_1 = Bus Set Up Time
+ Bus Skew

T_2 = Bus Skew

T = Total Transfer Time

4.3 Description of a Typical Transfer



Sequence:

1. Information has to be ready in the Transmitter Buffer.
2. Transfer Ready asserted, enables Tristate Drives, puts information to the bus.
3. Strobe appears on the bus, delayed by the amount of T_1 from Transfer Ready.
4. Strobe clocks the information from the bus into the Receiver Buffer.
5. Tristate Driver gets disabled after time T_2 from Strobe; bus "floats".
6. Transfer complete.