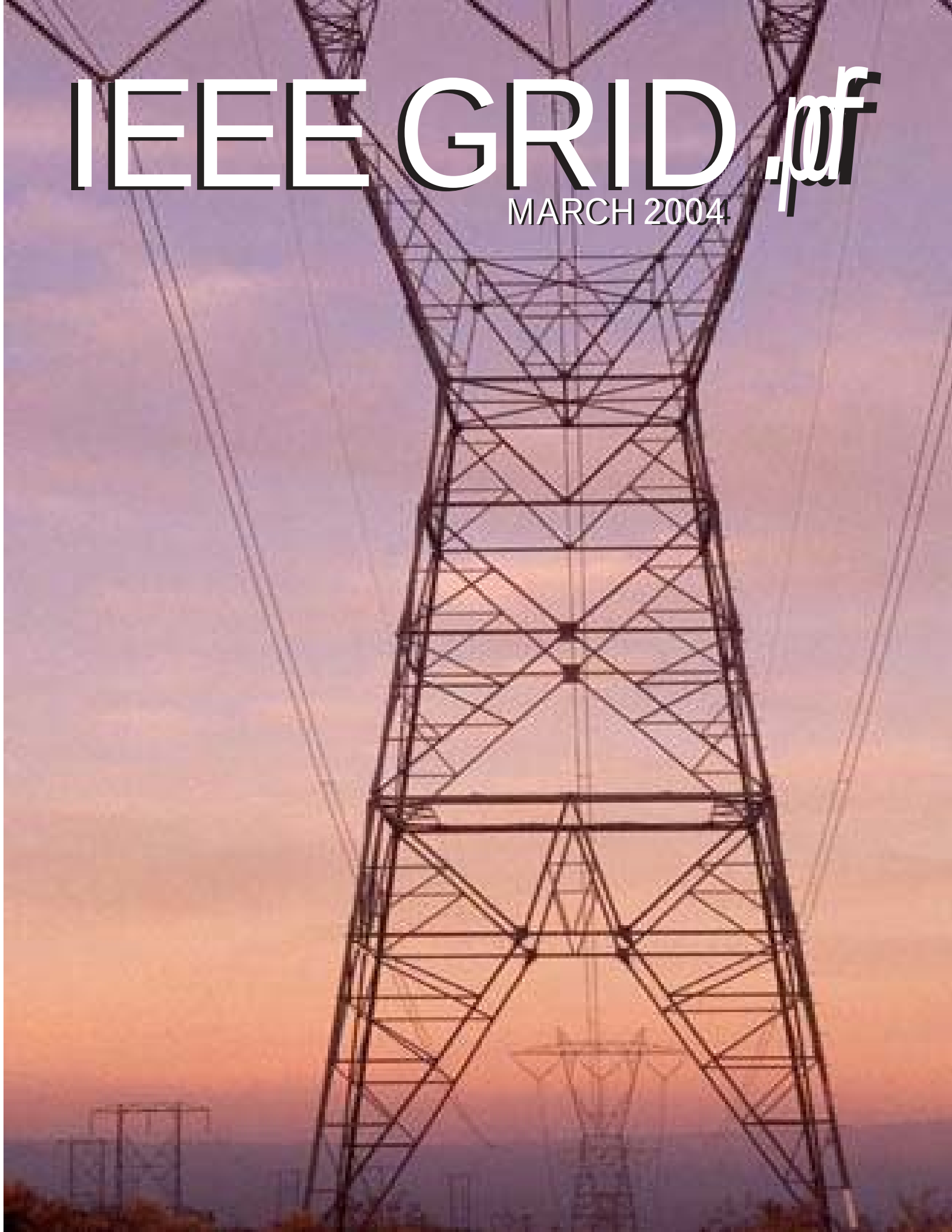
IEEE GRID .pdf
MARCH 2004

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IEEE Grid is the monthly newsmagazine of the San Francisco Bay Area Council of the Institute of Electrical and Electronics Engineers, Inc. As a medium for both news and opinion, the editorial objectives of IEEE Grid are to inform readers in a timely and objective manner of newsworthy IEEE activities taking place in and around the Bay Area; to publish the official calendar of events; to report on IEEE activities on a national and international scope; and to serve as a forum for comment on areas of concern to the engineering community by publishing contributed articles, invited editorials and letters to the editor.

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From the editor . . .

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A. Communications Systems and Networking:
1. Error Detection and Correction, 2. Signal Representation and Spectral analysis, 3. CDMA, 4. Modulation and Detection, 5. Performance Bounds, 6. Synchronization, 7. Ultra Wideband, 8. OFDM / Multicarrier, 9. Networks, 10. Wireless Communications, 11. Optical Communications

B. Adaptive Systems and Processing: 1. Adaptive Filtering, 2. Adaptive Signal Processing, 3. Adaptive Beamforming, Adaptive Technologies for Communication, 4. Intelligent Hearing Aids

C. Array Processing and MIMO: 1. Array Processing 2. Array Processing for Wireless Communications, 3. Sonar and Acoustical Array Processing, 4. Radar Array Processing, 5. MIMO / Space-time Coding

D. Biomedical Signal and Image Processing:
1. Medical Image Analysis, 2. Imaging Modalities, 3. Advances in Medical Imaging, 4. Biomedical Signal Processing, 5. Biomedical Applications, 6. Bioinformatics, 7. Image Registration and Multi-modal Imaging, 8. Image Reconstruction, 9. Computer Aided Diagnosis, 10. Functional Imaging, 11. Visualization

E. Signal Processing Algorithms and Applications: 1. DSP in Wireless Communications, 2. Radar and Sonar Signal Processing, 3. Energy Efficient DSP, 4. Low Rank Signal Processing, 5. Cooperative Analog / Digital Signal Processing, 6. Multimedia Signal Processing, 7. Multisensor / Multirate Signal Processing

F. Architecture and Implementation: 1. FPGA Implementation, 2. ASIC Implementation, 3. VLSI Implementation, 4. Computer Arithmetic, 5. Numerical Processing, 6. Architectures for Multimedia, 7. Security

G. Speech, Image and Video Processing:
1. Speech Processing, 2. Speech Coding, 3. Speech Recognition, 4. Narrowband / Wideband Speech and Audio Coding, 5. Document Processing, 6. Mathematical Models for Signal and Image Processing, 7. Image and Video Coding, 8. Image and Video Segmentation, 9. Image and Video Analysis, 10. Image / Video Security, Retrieval and Watermarking, 11. Image and Video Enhancement / Filtering, 12. Biometrics and Security

H. Tools and Strategies for Education

Prospective authors are invited to submit a 50 to 100 word abstract and an extended summary (500 to 1000 words, plus figures). Submissions must include the title of the paper, each author's name and affiliation, and the technical area(s) in which the paper falls with number(s) from the above list. Please visit the conference websites (web.nps.navy.mil/~asilomar, www.nps.navy.mil/asilomar) for specific information on the electronic submission process. **No more than FOUR submissions are allowed** per contributor, as author or co-author. **All submissions must be received by June 1, 2004**. Notifications of acceptance will be mailed by late August 2004, and author information will be available on the conference website by mid September 2004. Full papers will be due at the conference and published in the spring of 2005. All technical questions are to be directed to the Technical Program Chair, **Dr. Scott T. Acton**, e-mail: acton@virginia.edu, or the General Chair: **Dr. Keith A. Teague**, e-mail: teague@okstate.edu.

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SCV LEOS

TUESDAY MARCH 2

TUESDAY MARCH 2
SCV Lasers & Electro Optics Society
Subject: ***Advances in Flexible Network Processing***
Speaker: Peder Jungck (CloudShield)
Time: Pizza social at 7:00 p.m., presentation at 8:00
Place: National Semiconductor Credit Union Large Auditorium, 955 Kifer Road, Sunnyvale
RSVP: RSVP@silicavalley.com

Advances in Flexible Network Processing

Network communications equipment demand *is regaining some momentum amidst a very different market backdrop than two or three years ago. The issues today focus primarily on content based security, application service management, and privacy.*

Advances in network processor, FPGA and associated co-processor technologies will be discussed by Peder Jungck at he March 2 LEOS meeting, along with some of the new silicon and system level solutions that are making inroads into the market by supporting expansion or reducing cost and operational expenses. The speaker will compare the new breed of flexible packet processing platforms with the previous generation of solutions.

Government agencies, systems integrators and others have rolled out these new platforms to overcome complex high speed network application constraints. Jungck will examine several real world deployments.

Peder Jungck, founder and chief technology officer of CloudShield Technologies, Inc., is a networking industry visionary, IT executive and entrepreneur, who has pioneered high-speed content-based networking and security systems to meet the needs of government, carriers, and large enterprises.

During a career that spans more than 20 years, Peder has worked closely with large customers, helping them to simplify and streamline the deployment and management of large-scale, complex networks. Previously, he served as CTO of SVIC, and as managing partner and CIO of Internet-technology consulting firm Remington Associates, Ltd. Earlier in his career, at AT&T Global Information Systems/NCR, he led the Technology and Professional Services Group's services for customer J.C. Penney.

MONDAY MARCH 8

MONDAY MARCH 8
SCV CPMT Tutorial
Subject: ***Thermomechanical Reliability of Microsystems Packaging***
Speaker: Prof. Jianmin Qu (Georgia Institute of Technology)
Time: 9:00 a.m. - 5:00 p.m.
Place: Fairmont Hotel, San Jose
Fee: $375
Contact: Bonnie Crystall, 480 839-8988
Registration: www.semi-therm.org/

Thermomechanical Reliability of Microsystems Packaging

This course provides *an overview of the science and technology of thermo-mechanical reliability of microsystem packages. After a brief introduction to some basic mechanics theories and fundamental physics of failure concepts, failure modes pertinent to advanced packages (flip-chip, BGA, CSP, etc) are discussed. Emphasis is given to materials characterization, damage analysis due to fracture, fatigue and creep, processing modeling and accelerated tests. Topics to be covered include failure mechanisms, reliability analyses (numerical and experimental methods), and reliability evaluations. Case studies will be presented to illustrate the theories and methodologies.*

The key topics are: Fundamentals of Thermo-mechanical Reliability; Numerical Techniques (FEM,BEM, etc); Assembly Warpage Prediction; Effects of Die Size on Reliability; Life prediction of Interconnects (tin-lead and lead-free solders) Electrically Conductive Adhesives; Thermal Fatigue Life of Several Packages (FC DCA, CSP, BGA); Effective Properties of Underfill Materials; Moisture Effects on Interfacial Fracture Toughness; Modeling and Characterization of Interfacial Adhesion; and Application of Nanostructured Materials in Electronic Packaging.

Several other Tutorials are being conducted at the Fairmont on March 7 and 8 and may be of interest to SF Bay Area engineers:

"Experimental Measurements in Thermal Management of Electronic Systems" (2 days) taught by Prof. Alfonso Ortega, University of Arizona; Prof. Robert Moffat, Stanford University; Prof. Russel Westphal, Washington State University; and Prof. Jinny Rhee, San Jose State University.

"How to Achieve Electromagnetic Compatibility While Solving Thermal Problems" taught by Dr. Tom Van Doren, University of Missouri-Rolla.

"Compact Thermal Modeling: Theory and Practice" taught by Clemens J.M. Lasance, Philips Research Laboratories (The Netherlands) and Heinz Pape, Infineon Technologies (Germany).

For information and registration details on all courses, please visit the SEMI-THERM website at www.semi-therm.org/.

MONDAY MARCH 8

MONDAY MARCH 8
SCV Signal Processing Society
Subject: ***Telephony Speech Recognition Application Testing***
Speaker: Zaydoon Jawadi (CoAssure, Inc.)
Time: Fast food and drinks at 6:30 p.m., announcements at 7:00, presentation at 7:10
Place: National Semiconductor Credit Union, Building 31), 955 Kifer Rd., Sunnyvale
Cost: $1 donation for food requested
RSVP: Not required

Telephony Speech Recognition Application Testing

Self-service automated speech-recognition *and DTMF telephony applications provide convenient access to real-time information via the telephone, as well as cutting costs by eliminating the need for call center assistance by representative. Application issues, though, can result in customer dissatisfaction and unsuccessful self-service; furthermore, they can cause callers to opt for live agents, undermining the advantages and cost savings expected from the system. Therefore, comprehensive testing is essential for the success of such applications.*

Prior to deployment and any time hardware or software upgrades, various testing and analysis of functionality and performance need to be conducted. Traditionally, dialog traversal, also called call flow, is verified manually. However using automation, comprehensive, consistent, repeatable, automated testing can be achieved, along with cost savings.

This topic will be explored at the March 17 SPS meeting by Zaydoon Jawadi, CEO of CoAssure, Inc. Previously, he was founder and chairman of Can Do, Inc., general manager at Xyratex International, and founder and CEO of Zadian Technologies. Earlier in his career, he worked in engineering and engineering management in the computer and telecommunications industries. Mr. Jawadi holds an MS degree in computer science from Columbia University, NY.

SCV Electron Devices Society

TUESDAY MARCH 9

TUESDAY MARCH 9
SCV Electron Devices Society
Subject: ***The Teenage Years of the Transistor***
Speaker: Don Wollensen
Time: Pizza social at 6:00 p.m.,
presentation at 6:15
Place: National Semiconductor Corp. Building 31
Large Auditorium, 955 Kifer Road,
Sunnyvale
RSVP: Not required

The Teenage Years of the Transistor

The original point-contact transistor *was invented in 1947 by John Bardeen, Walter Brattain, and William Shockley. The "Teenage Years" start in 1960 and run until 1966, a period of great development, rise and fall of a number of companies and transitions from Germanium to Silicon and from labor intensive production to automated manufacturing. It was a period of displacing the venerable vacuum tube in consumer and industrial products and an enabler of missiles, satellites, space probes, and manned space flight. It was also the time of the first integrated circuits. It's part of the story of the legacy of which all of us in electronics benefit today.*

Donald L. Wollensen. Who will discuss this topic at the March 9 EDS meeting, spent 45 years in the field of electronics, starting out in the Navy as an Aviation Electronics Technician. After the Navy experience, he attended Cal Poly Pomona in the electronics engineering curriculum and graduated in 1963. While at Cal Poly he was an intern at North American Aviation and worked (in a small way) on the Apollo spacecraft.

After graduation from Cal Poly Pomona, he worked at Motorola Semiconductor Products, Inc. in Phoenix, and worked on Germanium transistors, Silicon transistors and diodes, and Gallium Arsenide transistors and diodes. He also worked on the first N Channel and P Channel complementary transistors (discretes!), which then led to initial work at Motorola on CMOS integrated circuits. Mr. Wollesen retired in January 2000 after 18 years at AMD working in technology research and development. He is author or co-author of 52 U.S. Patents and numerous technical papers.

SCV CPMT

MARCH 9-11

MARCH 9-11
SCV CPMT
Subject: ***Semiconductor Thermal Measurement and Management Symposium (SEMI-THERM)***
Speakers: 10 Sessions, 48 papers, exhibits
Fee: $735 ($675 for Members)
Place: Fairmont Hotel, San Jose
Registration: www.semi-therm.org
Contact: Bonnie Crystall, 480 839-8988 for a flyer and information

SEMI-THERM 2004

Semiconductor Thermal Measurement and Management Symposium

SEMI-THERM is the premier forum for the exchange of information between the industrial and academic communities on topics related to semiconductor thermal measurement, modeling and management. Using a unique combination of technical paper presentions, tutorials, short courses, exhibits, vendor workshops, topic tables and invited luncheon speakers, this Symposium provides a continuous stream of information exchange over three conference days and two short course days. Attendees and exhibitors come to San Jose from all over the world to participate in an informal atmosphere conducive to maximum exposure to leading technologies and the people behind the technologies.

This year there are four pre-Symposium Short Courses, available also to non-conference registrants. Technologists can get an Exhibits-only badge (free) to attend the exhibitor area at the Fairmont. This year's evening tutorial is "Optimization Techniques for Active Cooling Systems" taught by Reinhard Radermacher, University of Maryland, and two interesting lunch talks are "Trends in IC Technology and Their Impact on Power Dissipation" by Dr. Eric Beyne, IMEC in Belgium, and "Plans for a Thirty-Meter Ground Based Telescope" by Jerry Nelson, UC-Santa Cruz.

An Advance Program (with registration information) is available on the SEMI-THERM website, at www.semi-therm.org.

THURSDAY MARCH 11

THURSDAY MARCH 11
SCV Microwave Theory and Techniques Society
Subject: ***Microwave Frequency Synthesizers***
Speaker: A. David Williams (Teledyne Microwave)
Time: Refreshments and social hour at 6:00 p.m., presentation at 7:00
Place: Agilent Technologies, Santa Cruz Conference room, Building 50, 5301 Stevens Creek Blvd., Santa Clara
RSVP: Not required
Web: http://www.mtt-scv.org/mar_mtg.html

Microwave Frequency Synthesizers

A. David Williams first became involved *in the design of microwave frequency synthesizers in the late 1970s. Much has changed since then. His presentation at the March 11 SCV MTT meeting discusses design evolution and presents some examples showing how the arrival of new components and semiconductors has influenced designs.*

Additionally, the talk will cover the design of single and multi-loop indirect frequency synthesizers including fast switching and low phase noise devices. Finally, a new single loop, high-resolution design will be presented.

A. David Williams graduated from The Kingston Polytechnic (University of London) in 1970 having been sponsored by the General Electric Company of England. He spent 30 years as a GEC employee and became technology manager of the microwave operations at Marconi Electronic Devices in Lincoln, UK.

David moved to the USA in 1993 to become technical manager of the WLAN program at GEC-Plessey in Scotts Valley, and is now director of technology development at Teledyne Microwave in Mountain View.

David holds nine patents in various aspects of microwave engineering and has published sixteen technical papers.

MONDAY MARCH 15

MONDAY MARCH 15
SCV Circuits & Systems society
Subject: **Applying equation based synthesis to produce optimal pipeline A/D converters**
Speaker: Navraj Nandra (Barcelona Design)
Time: Refreshments and networking at 6:30 p.m., lecture at 7:00
Place: Cadence Design Systems, Bldg 5, 2655 Seely Ave, San Jose
RSVP: cas_scv_rsvp@yahoogroups.com

Applying Equation Based Synthesis to Produce Optimal Pipeline A/D Converters

Analog Design continues to be the bottleneck *in the design of mixed signal integrated circuits that are used in popular consumer electronics devices, and the communications and industrial electronics devices that enhance the productivity of today's businesses. Unlike digital circuits that can be automatically synthesized from a relatively simple description, analog circuits continue to require hand design, optimization and layout.*

There are a number of CAD startups that have been working to remove this bottleneck. One area in which this works is the application of optimization to adjust device parameters of a given circuit to meet a new set of performance targets. The target circuit for this application is a pipeline A/D converter.

Optimal device sizing and operational amplifier gain setting in a pipeline A/D converter is essential to meet the requirements of lower power consumption, reduced supply voltage and large SNR for many wireless and portable devices.

$$n_Q + \sum_{i=1}^{M} \frac{n_{stage\ i}}{G^{2(i-1)}} < \frac{(V_{\max}/2)^2/2}{10^{\frac{SNR_{\max}}{10}}}$$

Equation 1 defines the SNR limit of the pipeline A/D converter, where nQ is the quantization noise, nstage is the stage noise, and G is the gain of the stage. The right hand side of the equation is constant for a given pipeline specification in terms of dynamic range, Vmax being the analog range and SNRmax expressed in dB, the effective noise voltage. The lower supply voltage requirement presents the challenge of reduced dynamic range and SNR. Additionally, thermal noise limits the maximum SNR, the magnitude of the thermal noise being a function of the size of the sampling capacitor defined by s2thermal=kT/C. Note: this does not include the noise contribution from the operational amplifier. The sequence of setting the optimal gain, noise, and power, therefore, is the following:

Contined next page

WEDNESDAY FEBRUARY 18

• Earlier stages of the pipeline have lower gain and therefore noise contribution can be smaller
• Large proportion of noise is proportional to KT/C, to reduce noise C has to increase
• The earlier stages need larger capacitors which means more power is required

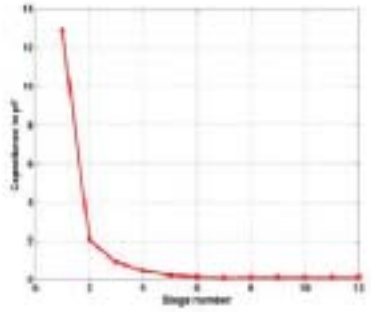
The effective resolution can be improved by increasing the sizes of the sampling capacitors (being determined by the noise floor) in the first few stages of the pipeline. The requirement on resolution is less at these stages in the pipeline, the sampling capacitors in the final stages can be made smaller, also parasitic capacitances begin to dominate and settling time requirements need to be taken into consideration. However capacitor sizing from the first stage of the pipeline to the last stage is a complex optimization task as the later stages contribute to both power dissipation and noise depending on their capacitor sizes.

In order to meet the requirements for lower power and higher performance, the designer is faced with making complex design trade-offs for the optimal capacitor sizes and also the optimal gain for switched capacitor blocks and minimum power consumption of the operational amplifiers and these determine the size of each stage.

This presentation will: introduce the equation based synthesis method as applied to the optimization of pipeline A/D converters; highlight the benefits of a synthesizable approach over traditional hand design; describe the pipeline architecture including the high gain operational amplifier; and conclude with silicon results from the prototype.

The architecture chosen for the synthesis is a traditional 9-stage design including a sample and hold stage in front for better dynamic linearity for high-frequency input signals. Each stage of the pipeline resolves a number of bits, and is implemented using a switched capacitor technique. In this architecture, accuracy relies only on capacitor matching, and it is possible to achieve up to 12-bit resolution without trimming. The circuit is differential, which ensures optimum immunity to interference from the power supply or the substrate. Digital error correction is added to generate the final digital code.

The synthesis method computes the sizes of the different components (transmission gates, capacitors and operational amplifier gain-bandwidth product) for each stage in the pipeline so that the design specifications are met in the desired process technology. The designer does not need to need find the optimal resolution of each stage or the optimal capacitor sizes through the pipeline. Figure 1 shows that using equation based synthesis the capacitors sizes are optimally sized through the pipeline.



[Fig 1 Capacitor scaling through pipeline]

The method is based on formulating the A/D design constraints in special convex form in terms of the component sizes of the A/D and intermediate design variables. The resulting GDSII layout includes a sample and hold amplifier, voltage reference and 2-phase clock generator from a single ended or differential single-phase clock input. The topology is compatible with standard CMOS processes. By using this topology and the synthesis approach a very wide specification range can be covered suitable for portable communication devices and wireless LAN.

To verify the effectiveness of the technique, a prototype 10bit 100 MS/s pipeline A/D converter was designed and fabricated in a 0.13 mm CMOS technology.

Speaker for this meeting is Navraj Nandra. He joined Barcelona Design in June 2001 as director of applications from Austria Mikro Systeme International, where he was U.S. Design Center manager supporting ASIC and COT designs in high voltage CMOS, SiGe and BiCMOS technologies.

Mr. Nandra has worked in the semiconductor industry since the mid 80s as an analog IC designer for Philips Semiconductors, EM-Marin (Neuchatel, Switzerland), and Thorn EMI Central Research Labs (UK). He has authored papers in A/D converter design and RFID design. In 1996 he was awarded the best poster for "A Contact-less Read/Write Transponder using Low Power EEPROM technology" at ESSCIRC in Neuchatel. He holds a Master of Science degree in microelectronic systems design from Brunel University and a postgraduate diploma in process technology from Middlesex Polytechnic, both in the UK.

TUESDAY MARCH 16

TUESDAY MARCH 16
SCV Magnetics Society
Subject: ***Magnetoresistive Random Access Memory: The Path To Competitiveness***
Speaker: Jian-Gang (Jimmy) Zhu (Carnegie Mellon University)
Time: Coffee and conversation at 7:30 p.m., presentation at 8:00
Place: Komag, 1710 Automation Parkway, San Jose
RSVP: Not required

Magnetoresistive Random Access Memory: The Path to Competitiveness

With the first commercial product *on the horizon [1,2], magnetoresistive random access memory (MRAM) is on a path to replace SRAM, DRAM, and FLASH (even disk drives in some applications) to be the universal solid-state memory. The non-volatility, fast access time, and compatibility with CMOS technology are three of the most important features that make MRAM potentially superior than other existing memory technologies.*

To fully exploit these potentials, present MRAM designs need to overcome three major obstacles: stringent fabrication tolerance, relatively high power consumption and write addressing disturbance. Although prototyping memory devices have been successful, new innovative designs are still required to make the technology truly competitive.

This lecture, by Jian-Gang (Jimmy) Zhu, ABB professor in engineering, Data Storage Systems Center and Department of Electrical and Computer Engineering, Carnegie Mellon University, will cover the micromagnetic magnetization reversal processes in various types of MRAM designs, including Motorola's 4Mbits toggle MRAM.

Over the past seven years, extensive micromagnetic analysis and experimental investigations have enabled many key understandings for obtaining robust magnetic switching and they have become the design principles for today's memory elements[3]. A comprehensive study of thermally activated magnetization reversal at small physical dimensions for various MRAM designs will be presented. The imposed area storage density limitations with the write disturbance will be discussed. The lecture will conclude with the presentation of a novel design that completely eliminates the write addressing disturbance and substantially lowers the power consumption [4].

1. e.g. S. Tehrani et al.: "Magnetoresistive Random Access Memory Using Magnetic Tunnel Junctions," Proceedings of the IEEE, p.703-714, May 2003.
2. B. N. Engel, "A 4-Mbit Toggle MRAM Based on a Novel Bit and Switching Method," MMM-Intermag, Paper GE05, Anaheim, California, 2004.
3. J.-G. Zhu and Y. Zheng: The micromagnetics of magnetoresistive random access memory, Spin Dynamics in Confined Magnetic Structures, Springer, Edited by B. Hillebrands and K. Ounadjela, p.289, 2002.
4. X. Zhu and J.-G. Zhu: "A vertical MRAM free of write disturbance," IEEE Trans. Magn. vol.39. p.2854, 2003.

Jian-Gang (Jimmy) Zhu *(IEEE Member '89, Senior Member '02) is a full Professor in the department of Electrical and Computer Engineering and the Data Storage Systems Center at Carnegie Mellon University and he holds the endowed chair ABB Professorship in Engineering. He received the B.S. degree in physics from Huazhong University of Science and Technology in 1982, the M.S. and the Ph.D. degrees, both in physics, from the University of California at San Diego in 1983 and 1989, respectively. In 1990, he joined the Department of Electrical Engineering at the University of Minnesota as an assistant professor. In 1992 he was granted the McKnight Land Grant Professorship by the Regents. He joined the faculty of Carnegie Mellon University in the beginning of 1997. He was a recipient of 1993-97 NSF Presidential Young Investigator Award. In 1996, his patent on Ultra-High Density Magnetic Sensor won the top 100 inventions award given by R&D magazine. He has authored or co-authored over 170 major technical journal publications and presented over 40 invited papers at various major international conferences. He has supervised and graduated 19 Ph.D. students. His current research includes advanced MRAM device design, advanced GMR heads design, advanced thin film recording media, digital tape recording system, patterned media, and mag-noise in magnetic nano-sensors. Professor Zhu is an advisory editor for the Journal of Magnetism and Magnetic Materials.*

WEDNESDAY MARCH 17

WEDNESDAY MARCH 17
SCV Engineering in Medicine & Biology Society
Subject: ***The Evolution of the Intraocular Lens***
Speaker: Reza Zadno (Three Arch Partners)
Time: Dinner at 6:15 p.m., presentation at 7:30
Place: Dinner in the Stanford Hospital Cafeteria, presentation in Room M114 of the Stanford Medical School
RSVP: Not required
Web: http://ieee.org/scv/embs/

The Evolution of the Interocular Lens

The primary cause of blindness *in the developed world is cataracts. In 2002 there were more than 6 million cataract procedures performed worldwide. This number includes over 3 million surgeries in the United States.*
Incredible technological leaps have been made, in both material development and lens design, in the 50 years since the first IOL was implanted. Technology improvements which had been centered on returning functional vision to elderly patients, will now provide both elderly and middle aged patients, the ability to conduct their day to day lives without the aid of glasses or contacts.

The inability to read at near distance due to aging is known as Presybopia. Patients who have experienced excellent vision, during their early life, are forced to begin wearing glasses. As with all other segments of this aging generation, the "Baby Boomers" will demand the highest quality of life. Patients seeking surgical treatments to regain both near and distance vision will rise dramatically during the next ten to twenty years.

The agenda of the March 17 EMB meeting is to briefly review the evolution of the intraocular lens. We will discuss changes and improvements in materials, and present new technologies such as multi-focal IOL's, adjustable IOL's and accommodating IOL's. These changes will gradually transform the cataract procedure into a refractive procedure as well as dramatically expand this segment of the vision market.

WEDNESDAY MARCH 17

Speaker for this meeting Reza Zadno was most recently at Three Arch Partners, working as entrepreneur in residence. Prior to joining Three Arch, he was with PercuSurge, Inc., which he co-founded in 1995, and where he served as VP of R&D and CTO until August 2000. PercuSurge developed, manufactured and marketed systems to contain and remove dislodged emboli during percutaneous vascular interventions, and was acquired by Medtronic in 2000.

Prior to PercuSurge, Reza was with Cardiac Pathways Corp. from the company's very early development stage until 1995, and served as director of the advanced development group. Cardiac Pathways developed, manufactured and marketed mapping and ablation systems for treatment of arrhythmia (IPO in 1996 and acquired by Boston Scientific in 2001).

From 1984-1992 Reza was with Raychem Corp. and worked in France, Belgium and USA as R&D engineer and project manager. At Raychem, he developed Nitinol alloys and products in applications such as laparoscopy instruments, guide wire materials, dental arches, and industrial products including electrical connectors. Reza holds MSc and PhD in metallurgy from Ecole Nationale Superieure des Mines de Paris and has filed more than 100 US and international patent applications.

THURSDAY MARCH 18

THURSDAY MARCH 18
OEB Communications Society
Subject: ***Mobile Phone Software Upgrade on the Fly***
Speaker: Bill Kaminsky (DoOnGo Technologies)
Time: Pizza and networking at 6:30 p.m., presentation at 7:00
Place: Bishop Ranch 1, 6101 Bollinger Canyon Road, San Ramon (just off I-680)
RSVP: (by 3/17) oeb@comsoc.org for pizza order
Info: Malik Audeh, audeh@ieee.org or 510 305-6022
Web: http://www.comsoc.org/oeb/

Mobile Phone Software Upgrades On the Fly

The next big thing *for the wireless communication industry is data services made possible by the newer wireless networks generally known as either 2.5G (Two and a half Generation, such as GPRS/EDGE) or 3G (3rd Generation, such as UMTS) networks.*

The industry is counting on the wireless data applications to increase the Average Revenue Per User (ARPU). These enhanced data services require increasingly complex handsets. At the same time competitive market forces are pushing the handset vendors to shorter development cycles. Handset manufacturers are meeting these challenges by adding the capability to update the device software using Over-the-Air (OTA) interface.

OTA software update capability provides a low cost method to deliver software patches (bug fixes) and software upgrades to add new features. Wireless service providers want to shorten the time to market and to offer feature upgrades to their customers after sale of the handset. OTA software update is a possible solution. The March 18 presentation will describe the market place, OTA update technology, key issues and evolving standards.

Bill Kaminski leads the new technology development for DoOnGo Technologies, a leading startup in the emerging over-the-air (OTA) update and management of wireless device software. He has been active in the telecommunications industry for over twenty years in various R&D and development positions. His areas of interest include system architecture, software development, communications systems, information system security and artificial intelligence.

Prior to DoOnGo, Bill led the network security technology program at Vodafone. He has held key R&D and management roles in several companies including Bell Laboratories where Bill began his career.

Bill holds a PhD in computer and electrical engineering from the University of Illinois. He teaches at the University of San Francisco as adjunct faculty in the MSIS program.

The chapter will continue to facilitate member networking by providing time to those who want to make a brief announcement. If you are looking for a position, have a position to fill, want to announce your new start-up, please bring your resume, job descriptions or company brochures and be prepared to make a match. Please keep your statements brief, so we'll have time for everyone. There is also time, before and after the formal meeting for one-on-one discussions.

THURSDAY MARCH 18

THURSDAY MARCH 18
OEB Industry Applications society
Subject: ***Lessons Learned From Electrical Failure Investigations***
Speaker: Wally Vahlstrom (Electro-Test Inc.)
Time: No-host social at 5:30 p.m.; Presentation at 6:15, Dinner at 7:15, presentation continues at 8:00 pm
Place: Marie Callendar Restaurant, The Garden Room, 2090 Diamond Blvd., Concord (nearby to Concord Hilton Hotel) 925 827-4930 for directions.
Cost: (dinner) $22 for IEEE members; $25 for non-members.
RSVP: (by March 17) Gregg Boltz, 925 210-2571 or gboltz@brwncald.com

Lessons Learned from Electrical Failure Investigations

The March 18 meeting *of the IEEE Industry Applications Society, for the Oakland East Bay Area, will feature a talk by Wally Vahlstrom of Electo-Test, Inc. His topic is electrical failure investigations.*

As electrical professionals we all hate to see good electrical equipment ruined due to installation mistakes, lack of maintenance, or poor operating procedures. Sadly, people have also been killed or injured due to relatively simple oversights, whereas others have miraculously escaped serious injury.

What lessons can be learned from these experiences? This presentation will consist of a review of several failure investigations involving electrical power system failures. Each case study is instructive and will include photos of the failed equipment and a discussion of the cause. The photos will show failures involving transformers, fuses, breakers, switchgear, meters, busduct and other power system equipment. The lessons learned from these failures have been condensed into a handy checklist to help improve electrical equipment maintenance and system reliability practices. The resulting checklist will be a valuable tool for all who attend the meeting and have responsibility for design, maintenance or operation of critical electrical equipment.

The speaker is Wally Vahlstrom, director of technical services for Electro-Test, Inc. (ETI). In his position, Mr. Vahlstrom is responsible for failure investigation work, energy management and auditing services, Nationally Recognized Testing Laboratory (NRTL) services, power system studies and reliability analysis, and instrument calibration and repair services.

Prior to joining ETI, Mr. Vahlstrom held a variety of positions at Pacific Gas and Electric Company (PG&E). His last position there was director of engineering. In this assignment he managed a multi-disciplined engineering department that provided project design for fossil and geothermal power plants with a combined capacity of 8000 MW. During more than 20 years with PG&E, Mr. Vahlstrom held various positions including chief electrical engineer. Some of his design and project responsibilities included electrical distribution systems and equipment, substations, transmission lines and nuclear, hydro, fossil and geothermal power plants.

Mr. Vahlstrom has a BS-electrical engineering degree from California State University, Fresno, and an MS-engineering degree from the University of Santa Clara. He is a registered professional electrical engineer. His professional affiliations include IEEE, National Association of Forensic Engineers (NAFE), and the Lightning Protection Institute.

SCV Computer Society

THURSDAY MARCH 18

THURSDAY MARCH 18
SCV Computer Society and Stanford IEEE Student Branch
Subject: ***Silicon Valley Shannon Lecture Series - Rate Control in Video Streaming***
Speaker: Nam Ling, PhD (Santa Clara University)
Time: Refreshments at 7:00 p.m., presentation at 7:30
Place: Auditorium Room 101 in the David Packard Electrical Engineering Building on the Stanford University campus.
Web: http://www.siliconvalleycs.org/

Rate Control in Video Streaming

One of the key issues in streaming video *over the Internet or wireless channels is to effectively adjust the bit rate adapting to the dynamics of available channel bandwidth and at the same time maintaining the highest possible and stable video quality with good coding efficiency. The recent ISO MPEG-4 AVC (advanced video coding) or ITU-T H.264 standard provides substantial improvements to coding efficiency for video transmission.*

This topic will presented by Nam Ling, PhD, of Santa Clara University at the March 18 meeting of the computer society and the Stanford IEEE Student Branch.

Prof. Ling's research focuses on designing algorithms for effective control of sending rate adaptive to available channel bandwidth. The adaptive bit rate control is based on a fluid-flow traffic model and a revised quadratic rate-distortion model. This method also gives heavier weights to earlier predictors in the picture sequence to achieve a better overall quality. Moreover, video distortion is reduced due to high motions or scene changes, by more accurately predicting frame complexity using the statistics of previously encoded frames in comparison with that of the current frame.

Recent results also include an improved frame skipping decision scheme to reduce the number of forced skipped frames that can cause poor reconstruction of video and motion jerkiness associated with the skips. The proposed bit rate control scheme is optimized for video quality, especially at low bit rates.

Continued next page

*Comparing to other existing schemes, this method allocates bits better to adapt to the dynamics of channel bandwidth. It effectively alleviates visual quality (PSNR) variation and significantly reduces the number of otherwise forced skipped frames. The overall visual quality value (PSNR) is also slightly improved. Part of the project was conducted jointly with the Institute for Infocomm Research, A*STAR, Singapore.*

Prof Ling is currently an associate dean of engineering and a full Professor of computer engineering. He was named 2002-2003 IEEE Distinguished Lecturer by the IEEE Circuits and Systems Society, and an Honorary Advisor to the National University of Singapore.

His research interests are in the fields of video coding, video streaming, and MPEG-2/MPEG-4/H.264 video decoder architecture. He has about 100 research publications, including a book on systolic arrays. Prof. Ling was named Arthur Vining Davis Junior Faculty Fellow in the U.S. in 1991-92. He received the SCU Outstanding Achievement Award in Teaching, Research, and Service, in 1992, and was named Researcher of the Year by SCU in 2000. In 2002, Prof. Ling also received the SCU Award for Recent Achievement in Scholarship.

Prof. Ling has served as an associate editor for the IEEE Transactions on Circuits and Systems-I, and was the chair and members of the IEEE Technical Committee on various subjects in various societies, including computer society. He was general/program/session chairs for many IEEE conferences; he is a well recognized scholar in his fields.

Solid State Circiuts

THURSDAY MARCH 18

THURSDAY MARCH 18
SCV Solid State Circuits Society
Subject: ***A Direct Conversion CMOS Transceiver for IEEE 802.11a Wireless LANs***
Speaker: Dr. Pengfei Zhang (RF Micro-Devices)
Time: Refreshments at 6:30 p.m., presentation at 7:00
Place: Cadence Design Systems, Bldg. 5, 2655 Seely Ave., San Jose
RSVP: ssc_scv_rsvp@yahoogroups.com For email reminder subscribe to: ssc-chptscv@majordomo.ieee.org
Web: http://www.ewh.ieee.org/r6/scv/scv_ssc.htm

A Direct Conversion CMOS Transceiver for IEEE B02.11a Wireless LANs

With the WLAN explosion, *RFICs have become a very important solid-state design activity. Dr. Pengfei Zhang will discuss this technology at the March 18 meeting of the SCV Solid State Circuits Society. His presentation describes a CMOS transceiver fully compliant with IEEE 802.11a standard in the Unlicensed National Information Infrastructure (U-NII) band at 5.15-5.35 GHz. It uses direct conversion architecture in order to reduce the chip area and power consumption.*

The transceiver contains the receiver with AGC, the transmitter with programmable output power and reconstruction filters and the frequency synthesizer. It achieves a sensitivity of -69 dBm and an error vector magnitude of -29.3 dB for 64QAM OFDM signals at 54Mbit/s data rate. Frequency synthesizer uses single-sideband mixing technique for LO generation to avoid frequency pulling. Realized in 0.18-um CMOS and operating from 1.8 V single supply, the chip consumes 171 mW in receive mode and 135 mW in transmit mode.

Pengfei Zhang (M'97) received the BS, MS and PhD degrees in electrical engineering from Tsinghua University, Beijing, China, in 1988, 1990 and 1994, respectively. From 1994 to 1996, he was a post-doctoral scientist of the Electrical Engineering Department at University of California, Los Angeles, where he did research on numerical simulation of SOI devices. From 1996 to 1999, he was with Rockwell Semiconductors, Inc, Newport Beach, where he worked on advanced process technology development for 56K-Modem. From 1999 to 2000, he was with Fujitsu Microelectronics, Inc., San Jose. There he worked on design methodology for signal integrity in mixed-signal IC's and RFIC design for wireless networking applications.

Since 2000, he has been with RF Micro Devices, San Jose (formerly Resonext Communications, Inc), where he is design manager of RFIC group at the WLAN Division, working on transceiver chip development for multi-standard applications. His research interests are in the area of integrated circuits for wireless communications.

CCMPT Short Course

MONDAY MARCH 22

MONDAY MARCH 22
SCV CPMT Tutorial
Subject: Compact Modeling and Analysis for Nanometer-scale CMOS Design
Speakers: IBM, Georgia Tech, U-Michigan, UC-SD, Purdue, Intel
Time: 9 a.m. - 4:30 p.m.
Place: DoubleTree Hotel, San Jose
Fee: $250 ($300 after 3/14), $150 students
Contact: Ali Iranmanesh, ISQED, 650 868-8844
Registration: www.isqed.org

Compact Modeling and Analysis for Nanometer-scale CMOS Design

This full-day tutorial focuses *on a range of critical issues in circuit design for sub-100nm CMOS. Five noted experts in their respective fields present the latest research in these compelling areas:*

"Nanometer-Scale CMOS Devices" (Kerry Bernstein, IBM T.J. Watson Research Center)
"Interconnect Modeling" (Prof. Jeff Davis, Georgia Tech)
"Manufacturability" (Prof. Andrew B. Kahng, UC-San Diego)
"Low-Power Design" (Prof. Kaushik Roy, Purdue University)
"Coping with Uncertainty" (Nagib Hakim, Intel Corp.)

The tutorial covers: The operation and idiosyncrasies of emerging deep submicron CMOS devices and materials appearing in future high speed logic products; Compact VLSI interconnect models for both parameter extraction and key transient waveform characteristics; Physical design complications and methodology changes as a result of sub-wavelength lithography and deep submicron manufacturing; Technology scaling and its impacts on dynamic and static power dissipation; and Various sources of uncertainty, their modeling, and their impact on various types of circuits.

This Tutorial is conducted the day prior to the International Symposium on Quality Electronic Design (ISQED) — see the Symposium website www.isqed.org for more information.

TUES-WED MARCH 23-24

TUESDAY-WEDNESDAY MARCH 23-24
SCV CPMT
Subject: IEEE Quality Electronic Design Symposium
Speakers: 18 sessions, 75 technical papers
Place: DoubleTree Hotel, San Jose
Fee: $525 ($425 for Members)
Registration: www.isqed.org/
Information: Ali Iranmanesh, ISQED, 650 868-8844

ISQED 2004

The 5th International Symposium on Quality Electronic Design *(ISQED 2004) is the premier Design and Design Automation conference, with technical sponsorship by the IEEE Electron Devices Society and the IEEE CPMT Society, and in cooperation with IEEE CASS, ACM/sigDA, and the Fabless Semiconductor Association (FSA), and with the Conference proceedings published by the IEEE Computer Society. The ISQED'04 conference spans three days, starting with a one-day Tutorial on "Compact Modeling and Analysis for Nanometer-scale CMOS Design". Tuesday and Wednesday bring three parallel tracks, hosting nearly 80 technical presentations, six keynote and luncheon speakers, three panel discussions, workshops/ tutorials and other informal meetings.*

Held this year at the DoubleTree Hotel in San Jose, ISQED aims at bridging the gap between (and integration of) electronic design tools and processes, integrated circuit technologies, processes & manufacturing, to achieve design quality. The conference provides a forum to present and exchange ideas and to promote the research, development, and application of design techniques and methods, design processes, and EDA design methodologies and tools that address issues which impact the quality of the realization of designs into physical integrated circuits. ISQED emphasizes a holistic approach toward design quality and intends to highlight and accelerate cooperation among the IC Design, EDA, Semiconductor Process Technology and Manufacturing communities.

SVC Engineering Management

WEDNESDAY MARCH 31

WEDNESDAY MARCH 31
SCV Engineering Management Society
Subject: ***Remote Management Strategies***
*Speaker: Barbara Miller (****Artemis Management)***
Subject: ***Pipeline Management***
Speaker: David Kirjassoff (Consultant)
Time: Forum at 6:00 p.m., dinner at 7:00, after dinner presentation at 7:45
Place: Wyndham Garden Hotel, 1300 Chesapeake Terrace, Sunnyvale - off Lawrence Expressway/Caribbean Drive at Hwy 237
RSVP: http://www.ieee-scv-ems.org
Cost: (with reservations by March 26) $25 IEEE member, $30 non member, $5 surcharge thereafter Cash or check at the door Student members - $5
Info: Rich Hendrickson, 408 203-3462

Managing Remote Resources and Pipelining Projects

The Santa Clara Valley Engineering Management Society presents a before-dinner forum on strategies and techniques to be successful as a virtual manager of resources distributed across locations and time zones. Following networking and a sit-down dinner, the featured topic will look at the engineering organization as a development pipeline where the flow rate is a function of both the quantity of resources applied and how well the pipeline is managed.

Before-Dinner forum

Remote Management Strategies

Many organizations today are distributed across a range of locations and time zones. Managers, employees and business partners in these dispersed environments face many challenges. Barbara Miller will provide you with concrete strategies and techniques to be successful as a virtual manager, team lead or project manager.

How do I lead my team whose members are located around the globe? How do I work with business partners or key stakeholders who I never see face to face? What are the best practices others are using to achieve results in a virtual world? Barbara will answer these questions and more in an interactive presentation that will provide you with specific techniques you can immediately implement to make a difference for yourself and your team.

Barbara Miller is a co-founder of Virtual Connection, and president of Artemis Management Consultants. She has helped organizations manage change, build teams, redesign work processes, and improve manager capabilities for thirty years. She has a Master's Degree in management science and women studies from George Washington University and has taught organizational theory and practice and group dynamics at the University of San Francisco's graduate program in HR/OD. Barbara spearheaded action research on work-life issues sponsored by the Ford Foundation.

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WEDNESDAY MARCH 31

After-Dinner presentation -

Pipeline Management

In reducing time-to-market, many companies focus on application of project management, improving the ability of development teams to plan, schedule, and stay on track. While this is an effective approach, it does not address the many sources of delay that are beyond the direct control of the development team. Shifting priorities, reallocation of resources, and queuing at common bottlenecks are frequently cited as sources of delay; and yet are not readily addressed by focusing at the team level.

In pipeline management we look at the development engineering organization from the perspective of operating a development pipeline. Design concepts feed into the entrance to the pipe, and exit as products ready for market. The capacity or flow rate of the pipeline is a function of both the quantity of resources applied, and how well the pipeline is managed to ensure a streamlined flow. In this presentation David Kirjassoff will explore the pipeline management tactics that help to increase the flow of new products.

David Kirjassoff has 18 years of experience in total quality management, large-scale organization change, and business process improvement in both the semiconductor and specialty chemicals industries, building on his eight years of line experience in process/project engineering and manufacturing management.

He currently operates an independent consulting practice, specializing in assisting technology companies with strategy deployment, product development effectiveness, team leadership, and virtual teaming.

In his previous role at National Semiconductor, he was director of organization performance, responsible for implementation and support of National's ongoing transformation process. This included chairmanship of the senior executive change council, design and facilitation of quarterly executive retreats, revision of business metrics and assessment processes, division-level organization redesign, and coordination of companywide process improvement and employee involvement efforts.

Mr. Kirjassoff has a BS in chemical engineering from Cornell University, and is a graduate of the Greater Boston Executive Program in Business Management at MIT's Sloan School of Management.

Professional Services Marketplace - d.davolt@ieee.org for information