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Serving the San Francisco, Oakland-East Bay, and Santa Clara Valley Sections of the IEEE
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| **July, August Chapter Meetings** - summaries | **System-on-Chip, Embedded Systems Confs** in Sept | **Conferences in the SF Bay Area** | **Reliability Engng, EMC Tutorials, Courses** | **Subscribe** |

Download the July GRID.pdf (1 MB) to learn about new developments, and refer to it during the month. Also check for updated information during the month at our GRID website: **www.e-grid.net/**.

Chapter Meetings for late July, August:

SCV-LEOS - 7/23: Tour: Naval Postgraduate School in Monterey - The number of participants is limited to 50, and we need your names in advance (for security reasons) ... [more]

SCV-LEOS - 8/3: "Directed Energy Weapons Systems" - The future path for Distant Early Warning (DEW) may well transition to high power solid state lasers and these create their own set of integration problems ... [more]

SF-PES - 8/18: Summer Banquet **"Electric Power: Demand Response Issues in California"** - Two speakers on the prospect of blackouts for the West Coast, what California is doing, and how Demand Response figures into the equation ... [more]

SCV-SSC - 8/19: "A Very Low Power CMOS Mixed-Signal IC for Implantable Pacemaker Applications" - A single-chip, very-low-power interface IC for implantable pacemaker systems uses new circuit techniques to achieve nano-power circuit operations with sub-micron CMOS processes ... [more]

SCV-WIE - 8/25: "RFID: the Next Big Thing for the Retail Industry" - Insights into the emerging technology of RFID and how it can be leveraged today with minimal enhancements to the current IT infrastructure ... [more]

The Council Marketplace
Do you need someone with special skills -- RF, reliability, communications, design, patent consultations? ... PCB layout, thermal measurements, SCSI, SANs? See our **Council Marketplace** page. Thank you for supporting our advertisers.

Other Events of Interest:
Tuesday, July 27: NanoBioConvergence presents:
Nanofabrication: Self-Assembly Part II
An evening discussion on creating nanoscale architecture through molecular recognition and self-assembly, with presentations of neural linkage for regenerative medicine and controlled protein assembly for biosensor devices.
Speakers: **Samuel I. Stupp**, Professor of Materials Science, Chemisty and Medicine, NWU (Founder of NanoMateria, Inc.), and **Jonathan Trent**, Nanotechnology & Astrobiology Research Group, NASA Ames Research Center

Location: Pillsbury Winthrop in Palo Alto (just off Page Mill Road)
Time: Light dinner, networking at 6PM; Program begins at 7PM
Cost: $25 for pre-registered attendees, $35 for registration at the door, $20 for students at the door with valid ID
See website for more details:
www.nanobioconvergence.org

Conferences and Workshops coming to the SF Bay Area -- Profiles

September 12-15: **IEEE International SOC Conference (SOCC'04)** -- Santa Clara Hilton, Santa Clara **[more]**

Systems-On-Chip (SOC) has become a dominant issue in today's ASIC industry. SOCs have created new challenges in Design Methods, Design Tools, Design Automation, Manufacturing, Technology, and Test. The SOC Conference provides a forum for sharing advances in SOC technologies and applications. SOCC is sponsored by the IEEE Circuits and Systems Society. With three days of technical papers and a full day of technical workshops, SOCC is held in conjunction with the International Cadence Usergroup Conference across the street at the Westin Hotel. ***Early registration discount through August 13th.***

Key session themes:
Analog, Mixed Signal, and RF Design - High-performance circuits and methodologies - High-performance systems and architectures - System level architecture and design - Network processing architectures and circuits - Low power architecture - Low-power design - Reconfigurable architectures - Reconfigurable applications - Analog to digital conversion - Embedded systems - Embedded processors for SOC - Multimedia processors - Multi-threshold circuits - Deep-submicron design - Digital signal processing - DSP circuits - On-chip testing of embedded silicon transducers - Design for testability and reliability - Analog circuits - Wireless communication - Interconnect modeling - Issues of SOC ... plus a poster session

  - plus Keynote, Plenary, and Luncheon Talks, Panel Discussions, reception, vendor fair ...

September 27-30: **GSPx: the International Embedded Signal Processing Conference and Exhibition** -- Santa Clara Convention Center **[more]**

GSPx is specifically focused on embedded solutions, with a Technical Program and Technical Workshops developed to quickly immerse you in the latest technological innovations. There are three days of technical papers and a full day of technical workshops, in parallel with exhibits and the two-day Executive Summit. There's even a day of Professional Development Workshops organized by the IEEE -- see some of the details below. ***Early registration discount through August 6th.***

Key session themes:
- Analog & Mixed Signal Design - Architectures - Benchmarking - Cores - EDA & System Design Tools - Embedded H/W & S/W - FPGA-Based Solutions - Instrumentation and Testing - Modeling and Simulation - Parallel Processing - SoC Design
Application areas: - Aerospace - Automotive - Biomedical - Consumer Electronics - Cryptography - Digital Filtering - Industrial Controls - Multimedia - Navigation - Power Management - Radar - Robotics - Software Defined Radio - Speech Processing - Telephony
... plus others

  - plus Keynote, Plenary, and Luncheon Talks, Panel Discussions, reception, vendor fair ...

Technical and Professional Development Workshops:
(Workshops-only registrations OK)
- "Real Time Operating Systems for DSPs and Heterogeneous Systems Containing DSPs"

Tutorials on Sunday: (Tutorials-only registrations OK)
- Trade-Offs in RF Analog Circuit Design for SOC Applications
- Substrate Coupling Noise and its Reduction through Early Design Planning in Mixed-Signal SoCs
- 90-nm SOI CMOS SoC Technology with Low-Power Millimeter-Wave Digital and RF Circuit Capability
- SoC Design Methodology: A Practical Approach
- Heterogenenous Modeling of SoCs with System C using Multi-MOC Kernel of System C
- High-Performance CMOS Circuits for Sub-90nm Design
  … and more! Check website for scheduling details

Visit **www.e-grid.net/conf/socc.html** for more details.

See the **Conference Calendar** in the **GRID.pdf** for additional events.

- "Using C to Implement Real-time Image and DSP Algorithms in FPGA & Programmable SoCs"
- "Designing Advanced Wireless Applications with SPW"
- "System on Chip Design Incorporating Silicon Hive Programmable Domain-Specific Accelerators"
- "Model-Based Design for Signal Processing Systems with Simulink"
- "Efficient DSP Design for FPGA Implementation"
- "ASIP Implementation of Advanced Wireless Applications with LISATek"
- "Developing Handset Solutions Around The StarCore Family of Processors"
- "FPGA Signal Processing"

FREE IEEE Professional Development Workshops:
- "Taking Charge of Your Destiny: The New Rules for Career Success"
- "Networking for Success"
- "Project Management"
Attendance to these PD Workshops is **free** with the (free) Expo admission -- great for our unemployed Members! Sign up today!

Visit **www.e-grid.net/conf/gspx.html** for more details.

Summary of Upcoming Bay Area Conferences

AUGUST:
August 9-13: **IEEE Electromagnetic Compatibility Symposium (EMC'04)**, Santa Clara Convention Center **[more]**
... five full days with workshops and special sessions, over 200 exhibitors of EMC-related products and services (free). See the two-page flyer (with listing of exhibitors) in the **GRID.pdf**, or visit **www.e-grid.net/conf/emc.html**.

August 13-15: **IEEE Product Safety Engineering Symposium (PSES'04)**, Santa Clara Convention Center **[more]**
... Technical Sessions, Workshops, Tutorials, Demonstrations, Exhibits. See the one-page flyer in the **GRID.pdf**, or visit **www.e-grid.net/conf/pses.html**.

August 16-19: **IEEE Computational Systems Bioinformatics Conference** on the Stanford University campus **[more]**
... keynote speakers, poster presentations, and tutorials for bioinformatics' eclectic mix of disciplines. See the one-page flyer in the **GRID.pdf**, or visit **www.e-grid.net/conf/csb.html**.

August 22-27: **International Conference on Ferrites** (ICF 9) in San Francisco **[more]**
... science and technology of ferrites and related materials, more than 250 presentation. Reduced-rate registration through July 23. See the one-page flyer in the **GRID.pdf**, or visit **www.e-grid.net/conf/icf.html**.

August 25-27: IEEE **Hot Interconnects Symposium** at Stanford University **[more]**
... high-performance chips, software, and systems ... multiprocesor and system-level interconnects. See the one-page flyer in the **GRID.pdf**, or visit **www.e-grid.net/conf/hoti.html**.

SEPTEMBER:
Sept 1-5: **IEEE Int'l Conference on Engineering in Medicine and Biology (EMBC'04)** Westin St. Francis Hotel, SF **[more]**
... Technical Sessions, Workshops, Tutorials, Seminars, "Best Practices" roundtables, more. Reduced rates through July 1. See the one-page flyer in the **GRID.pdf**, or visit **www.e-grid.net/conf/emb.html**.

Sept 12-15: **IEEE International SOC Conference (SOCC'04)** Santa Clara Hilton, Santa Clara **[more]**
... advances in **Systems-on-Chip** technologies and applications -- Design Methods, Design Tools, Design Automation, Manufacturing, and Test. Visit **www.e-grid.net/conf/socc.html**.

Sept 21-23: **IEEE Wescon/2004,** Anaheim Convention Center **[more]**
... Includes **NANOWorld**, **Enterprise Integration EXPO**, the Autonomous Vehicle Technology Showcase, exhibits -- owned by engineers and run by engineers to benefit engineers. See the one-page flyer in the **GRID.pdf**, or visit **www.e-grid.net/conf/wescon.html**.

Sept 27-30: **GSPx: the International Embedded Signal Processing Conference and Exhibition,** Santa Clara Convention Center **[more]**
... Includes **Executive Summit**, Technical sessions and workshops, exhibits. Visit **www.e-grid.net/conf/gspx.html**.

Tutorials, Workshops, Professional Development Courses

Workshops at this year's EMC'04 in Santa Clara on Monday Aug 9 or Friday Aug 13 (Workshop-only registrations OK) **[more]**

NARTE EMC Exam: Monday: Exam Prep Workshop - Friday: NARTE EMC Engineer Exam
PCB Design - Double-Sided and Multilayer: intended for the novice to intermediate product designer - the design steps necessary to make PCBs meet EMC requirements.
Fundamentals of EMC Design: Understanding and applying basic design principles - how to design circuits and systems with built-in compatibility - fast rise and ultra-wide-bandwidth energy signals, sensitive sensors - medical, military, communications, IT, and instrumentation.

Plus a Dozen More -- See the full details for all of them in the Advance Program.   And remember - you can come for as little as one day of Workshops (minimal cost), or an afternoon at the exhibits (free) - in the heart of Silicon Valley.

Reliability Engineering & CRE Exam Preparation Course
  - Seven-week evening course
  - Starts **Tuesday, August 10th**
  - Tuesdays from 6 - 10 PM (thru Sept 21)
  - Location: QualMark Corp, 990 Richard Ave, Santa Clara
  - Course Fee: $995 (includes text book)
  - 25% discount for unemployed
  - This course fills up quickly and seating is limited

Intended for Design, Quality, and Reliability Engineers who need a good, in-depth course in reliability, and for those wishing to pass the ASQ's Certified Reliability Engineer exam.
Ops ALaCarte has offered this Exam Preparation Course for several years. Students have found it very valuable in preparing for the exam. The success rate in passing is several times higher for students that have taken the course compared to those that have not! Even if you are not planning on taking the exam but need a good, in-depth course in reliability, this can benefit you substantially.

For more information, send an email to **creprep@opsalacarte.com** or

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Technologists who are not members of IEEE are **encouraged to subscribe, at no cost, to this e-GRID Newsletter**, to find opportunities to "network" with the electrical engineering community and hear about Chapter events through our twice-monthly emails.   This is a controlled list (ie, no spam) -- get more information.   You provide your own subscribe/unsubscribe services and can join and leave this IEEE DList when desired.   To update the list, send an email message to:
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Please invite other non-Member technologists in the Bay Area to join this list, to receive notification of Chapter meetings, tutorials, workshops, conferences, and other news within the San Francisco Bay Area Council, IEEE. See **http://www.e-grid.net/**

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