1 APRIL 1961

THE INSTITUTE OF RADIO ENGINEERS, INC.
1 East 79th Street, New York 21, New York

61 IRE 28. C
Re: 60 IRE 28 PS7

TO: Members of the Standards Committee and
Chairmen of all Measurements Subcommittees

FROM: J. G. Kreer, Jr., Measurements Coordinator

SUBJECT: Proposed IRE Standards on Solid State Devices: Methods of Testing Junction Transistors for Large-Signal Applications, 1960

The enclosed Proposed IRE Standards on Solid State Devices: Methods of Testing Junction Transistors for Large-Signal Applications, 1960 is forwarded to you for comment. Additional copies are available for Committee and Subcommittee members, upon request to the Technical Secretary, IRE, L. G. Cumming, 1 East 79th Street, New York 21, New York.

It is urgently requested that this Proposed Standard be given careful consideration by the Measurements Subcommittees and that written comments be forwarded not later than May 20, 1961.

Comments should be sent to the following:

Dr. R. L. Pritchard
Texas Instruments, Inc.
P. O. Box 5012
Dallas, Texas

with a copy to:

Mr. J. G. Kreer, Jr.
Bell Telephone Laboratories, Inc.
Whippany, New Jersey

If no comments are received by May 20, 1961, it will be assumed that the Proposed Standard is satisfactory and it will be submitted for approval by the IRE Standards Committee.

J. G. Kreer, Jr.
Measurements Coordinator

Enclosure
ccs: Solid State Devices Committee

THE INSTITUTE OF RADIO ENGINEERS, INC.
1 East 79th Street, New York 21, N. Y.

60 IRE 28, PS7
December, 1960

# PROPOSED IRE STANDARDS ON SOLID STATE DEVICES METHODS OF TESTING JUNCTION TRANSISTORS FOR LARGE-SIGNAL APPLICATIONS, 1960

## Committee Personnel

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# NOTE

The Figures shown in conjunction with the text of this proposal have been included for reference purposes only and the final Figures that will appear are appended at the rear.

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METHODS OF TESTING JUNCTION TRANSISTORS FOR LARGE SIGNAL APPLICATIONS

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# Methods of Testing Junction Transistors for Large-Signal Applications

## 1.0 General

### 1.1 Scope

This standard describes and recommends methods of measurement of the important characteristics of junction transistors in large-signal applications. Examples of this type of usage include power amplifiers, pulse amplifiers, sinusoidal oscillators, multivibrator-type switches, current switches and regenerative pulse generators.

Large-signal modes of operation involve excursions of the operating point over large ranges of the device characteristics. Often, the operating point may move from a low-current cut-off region, through an essentially linear active region, to a high-current saturation region. The transistor can be considered as a switch, being OFF in the low-current cut-off region and ON in the high-current saturation region.

Transistors generally fall into two categories:

a) Devices whose common-base short-circuit forward-current transfer ratio $h_{fb}$ is greater than unity, and

b) Devices whose common-base short-circuit forward-current transfer ratio $h_{fb}$ is less than unity.

Point-contact and four-region transistors, for example, generally fit into the first category and three-region junction transistors into the latter. Methods of testing point-contact transistors for large-signal applications have been described in a previous standard.[1] This standard considers the methods of test for three-region junction transistors of category "b".

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1. "IRE Standards on Solid-State Devices: Methods of Testing Point-Contact Transistors for Large-Signal Applications", 1958 (58 IRE 28.S1) PROC. IRE, Vol. 46 pp 878-888 May, 1958.

In the case of junction transistors, the large-signal behavior may be expressed in an approximate analytical form which applies over the entire range of operation. In addition, piecewise linear approximations of the characteristics are frequently required to specify the performance requirements of specific devices. The procedures for measuring the parameters of both the analytical and the piecewise approximations are described.

1.2 Four-Terminal Representation

In non-linear applications, the device behavior must be specified adequately in all regions of operation. Pulse or switching operation is a special case of large-signal operation and many of the tests described in the following sections apply directly to other large-signal applications such as Class B or Class C amplifiers.

In large-signal applications the transistor can be represented by a two-port network whose dc behavior may be described by input voltage $V_I$ and current $I_I$ and output voltage $V_O$ and current $I_O$ as shown in Fig. 1. This is analogous to the small-signal case,[2] where the ac behavior may be similarly described.

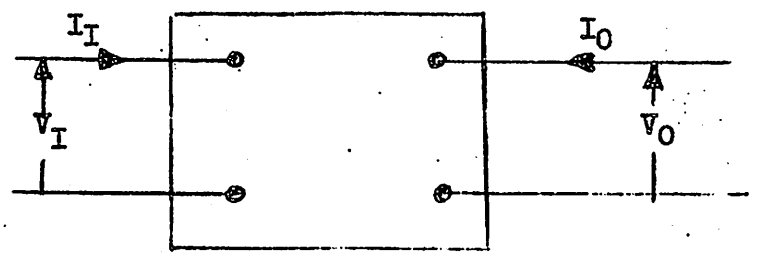


Fig 1. - General Two-Port Network Representation

2. "IRE Standards on Solid-State Devices: Methods of Testing Transistors", 1956, (56 IRE 28. S2) Proc. IRE, Vol. 44 No. 11 pp 1542-1561 November, 1956.

There are many ways of specifying the functional relationships between $V_I$, $I_I$, $V_O$ and $I_O$, and the choice of the appropriate set depends upon the nature of the device to be characterized. The small-signal h parameters or analogous large-signal parameters are used in this standard where appropriate. Small signal parameters are recommended for some measurements because of ease of instrumentation and interpretation, together with greater reproducibility.

1.3 Regions of Operation

In large-signal applications, the device behavior must be described over the entire range of operation, and it is convenient to divide the static characteristics into three regions[3,4] for purposes of making measurements.

Region I - A region in which both the emitter and collector junctions are biased in the reverse or high-resistance direction. Considered as a switch the transistor is in the OFF condition.

Region II - A region in which the emitter junction is biased in the forward direction, the collector junction is biased in the reverse direction, and the collector current is not limited by the external collector circuit. This region is usually called the "active region".

Region III - A region in which the emitter and collector junctions are biased in the forward direction and the magnitude and direction of the collector current are determined primarily by the external collector circuit. Considered as a switch, the transistor is in the ON condition.

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3. A. E. Anderson, "Transistors in Switching Circuits", Proc. IRE, Vol. 40, No. 11, pp 1541-1558, November, 1952

4. J. J. Ebers and J. L. Moll, "Large-Signal Behavior of Junction Transistors", Proc. IRE, Vol. 42, No. 12, pp 1611-1772, December 1954.

Non-linearities complicate the analysis of circuits in which the operating point of the transistor traverses two or more of the above regions. However, a combination of static and dynamic parameters may be chosen which adequately describes the behavior of the junction transistor in the three regions.

1.4 Switching Properties

In switching and pulse amplifier applications, the transistor is usually connected so that a signal applied at the input terminals can control the impedance at the output terminals to provide either a high or low output impedance. The primary factors of importance in such applications are the impedances in the two regions (ON or OFF), the speed with which the transistor switches from one region to the other, and the input loading characteristics.

The delay, rise, storage, and fall times [4,5] of the transistor are highly circuit-dependent, varying with the drive currents and voltages and the terminating impedances.

1.5 List of Terms

The notation used in this standard is consistent with "IRE Standards on Letter Symbols for Semiconductor Devices". [6]

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5. J. L. Moll, "Large-Signal Transient Response of Junction Transistors". Proc. IRE Vol. 42 No. 12 pp 1773-1784, December 1954

6. "IRE Standards on Letter Symbols for Semiconductor Devices", 1956 (56 IRE 28. S1) Proc. IRE. Vol. 44 pp. 934-937, July, 1956.

| Notation | Ref. Sect. | Definition |
|---|---|---|
| $BV_{CBO}$, $BV_{EBO}$, $BV_{CEO}$ | 2.2 | The breakdown voltage between the electrode indicated by the first subscript when it is biased in the reverse (high resistance) direction and the reference electrode, the other electrode being open-circuited. |
| $BV_{CES}$ | 2.2 | The breakdown voltage between the electrode indicated by the first subscript when it is biased in the reverse (high resistance) direction and the reference electrode, the other electrode being short-circuited to the reference electrode. |
| $BV_{CEX}$ | 2.2 | The breakdown voltage between the electrode indicated by the first subscript when it is biased in the reverse (high resistance) direction and the reference electrode, the other electrode being returned to the reference electrode through a given resistance and/or specified reverse bias. |
| $C_{ie}$ | 2.8 | The input capacitance is the shunt capacitance at the input terminals with the output ac open-circuited. |
| $C_{ob}$, $C_{oe}$ | 2.8 | The output capacitance is the shunt capacitance at the output terminals with the input ac open-circuited. |
| $C_{cb}$ (dir.). | 2.8 | The direct interterminal capacitance between the collector and base terminals in the capacitance appearing between collector and base terminals with all other terminals ac grounded. |
| $f_{hfb}$, $f_{hfe}$ | 2.7 | The small-signal short-circuit forward-current transfer ratio cut-off frequency is the frequency in cycles per second at which the absolute value of the small-signal short-circuit forward-current transfer ratio is $\sqrt{2}/2$ times its value at the low frequency specified. |
| $f_1$ | 2.7 | The unity current transfer ratio frequency is the frequency in cycles per second at which the absolute value of $h_{fe}$ is unity. |
| $f_t$ | 2.7 | The frequency in cycles per second at which the -6 db./ octave asymptote of $h_{fe}$ crosses the zero db. axis on a log $h_{fe}$ vs. log f plot, this asymptote intersecting the low-frequency asymptote at the frequency $f_{hfe}$. |

| Notation | Ref. Sect. | Definition |
|---|---|---|
| $g_{fe}$ | 2.5 | The small-signal short-circuit transconductance is the quotient of the ac output current divided by the ac input voltage, with zero ac output voltage. |
| $h_{fe}$, $h_{fb}$ | 2.5 | The small-signal short-circuit forward-current transfer ratio is the ratio of the ac output current to the ac input current, with zero ac output voltage. |
| $h_{FE}$ | 2.5 | The static forward-current transfer ratio is the ratio of the dc output current to the dc input current. |
| $h_{FE}$ ($\Delta$) | 2.5 | The large-signal forward-current transfer ratio is the ratio of the change in output current ($\Delta I_O$) to the corresponding change in input current ($\Delta I_I$) between two specified operating points, at a constant collector-to-emitter voltage. |
| $h_{FE}$ (inv.) | 2.5 | The inverse static forward-current transfer ratio is the ratio of the dc output current to the dc input current when the collector and emitter terminals are interchanged and the redefined configuration is measured in a normal manner. |
| $h_{ie}$ | 2.9 | The small-signal short-circuit forward-current transfer ratio is the ratio of the ac output current to the ac input current, with zero ac output voltage. |
| $\mathcal{R}e$ $h_{ie}$ | 2.9 | The real part of the small-signal short-circuit input impedance is the real part of the quotient of the ac input voltage divided by the ac input current with zero ac output voltage. |
| $h_{IE}$ | 2.5 | The static input resistance is the quotient of the dc input voltage divided by the dc input current. |
| $h_{IE}$ ($\Delta$) | 2.5 | The large-signal input resistance is the quotient of the change in dc input voltage ($\Delta V_I$) divided by the corresponding change in dc input current ($\Delta I_I$). |
| $I_{CBO}$, $I_{EBO}$<br>$I_{CEO}$, $I_{BEO}$ | 2.3 | The cut-off current between the electrode indicated by the first subscript, when it is reverse-biased by a voltage less than the breakdown voltage, and the reference electrode, the other electrode being open-circuited. |
| $I_{CBS}$, $I_{EBS}$<br>$I_{CES}$, $I_{BES}$ | 2.3 | The cut-off current between the electrode indicated by the first subscript, when it is reverse-biased by a voltage less than the breakdown voltage, and the reference electrode, the other electrode being short-circuited. |

| Notation | Ref. Sect. | Definition |
|---|---|---|
| $I_{CEK}$, $I_{BEX}$ | 2.3 | The cut-off current between the electrode indicated by the first subscript, when it is reverse-biased by a voltage less than the breakdown voltage, and the reference electrode, the other electrode being returned to the reference electrode through a given resistance and/or specified reverse-bias. |
| $\tau_s$ | 2.10 | The saturation stored-charge time constant is the quotient of the excess charge stored divided by the excess drive current above that required to maintain operation in the saturation region. |
| $Q_s$ | 2.10 | The stored charge is the total charge stored in the base and collector regions when the transistor is operated in the saturation region. |
| $t_d$ | 2.10 | The delay time of a pulse is the time interval from a point at which the leading edge of the input pulse has risen to 10% of its maximum amplitude to a point at which the leading edge of the output pulse has risen to 10% of its maximum amplitude. |
| $t_f$ | 2.10 | The fall time of a pulse is that time duration during which the amplitude of its trailing edge is decreasin from 90 to 10% of the maximum amplitude. |
| $t_r$ | 2.10 | The rise time of a pulse is that time duration during which the amplitude of its leading edge is increasing from 10 to 90% of the maximum amplitude. |
| $t_s$ | 2.10 | The storage time of a pulse is the time interval fro a point 10% down from the maximum amplitude on the trailing edge of the input pulse to a point 10% down from the maximum amplitude on the trailing edge of the output pulse. |
| $V_{CE}(sat)$, $V_{BE}(sat)$ $V_{CB}(sat)$, $V_{EB}(sat)$ | 2.4 | The saturation voltage is the dc voltage between the electrode indicated by the first subscript and the reference electrode for the saturation conditions specified. |
| $V_{CE}(sus)$ | 2.2 | The sustaining voltage is the dc voltage between the collector and emitter in the common emitter connection at specified values of collector and base currents. |

| Notation | Ref. Sect. | Definition |
|---|---|---|
| $V_{RT}$ | 2.2 | The reach-through voltage (sometimes referred to as "punch-through voltage") is that value of reverse voltage for which the reverse-biased PN junction spreads sufficiently to electrically contact another junction or electrode. |
| $y_{fe}$ | 2.5 | The small-signal short-circuit forward-transfer admittance is the quotient of the ac output current divided by the ac input voltage, with zero as output voltage. |

## 1.6 Characteristics for Large-Signal Applications

Methods of measurement for the following static and dynamic characteristics are described in this standard. It should be recognized that many of these characteristics are interdependent; for instance, the measurement of collector-to-emitter saturation voltage $V_{CE(sat)}$ listed in 1.6.4 inplies a minimum forward-current transfer ratio $h_{FE}$. The measurement of an abbreviated set will usually suffice for particular devices and specific applications.

### 1.6.1 Static Characteristic Families

1) $I_C$ vs. $V_{CE}$ curves with $I_B$ as a parameter
2) $I_B$ vs. $V_{CE}$ curves with $I_C$ as a parameter
3) $I_B$ vs. $V_{BE}$ curves with $I_C$ as a parameter
4) $h_{FE}$ vs. $I_C$ curves with $V_{CE}$ as a parameter
5) $I_C$ vs. $V_{CB}$ curves with $I_E$ as a parameter
6) $I_C$ vs. $I_B$ curves with $V_{CE}$ as a parameter

### 1.6.2 Breakdown Voltages

$BV_{CBO}$, $BV_{EBO}$, $BV_{CEO}$, $BV_{CES}$, $BV_{CEX}$, $V_{RT}$, $V_{CE}$ (sus)

### 1.6.3 Reverse Cut-off Currents

$I_{CBO}$, $I_{CBS}$, $I_{EBO}$, $I_{EBS}$, $I_{CEO}$, $I_{CES}$, $I_{BEO}$, $I_{BES}$, $I_{CEX}$, and $I_{BEX}$

### 1.6.4 Saturation Voltages

$V_{BE}$ (sat), $V_{CE}$ (sat), $V_{CB}$ (sat), $V_{EB}$ (sat)

### 1.6.5 Current Amplification Factors and Transadmittance, Transconductance

$h_{fe}$, $h_{fb}$, $h_{FE}$, $h_{FE}$ ($\Delta$), $y_{fe}$, $g_{fe}$

### 1.6.6 Input Resistances

$h_{IE}$, $h_{IE}$ ($\Delta$)

1.6.7 Cut-off and Unity Current Transfer Ratio Frequencies

$f_{hfb}$, $f_{hfe}$, $f_l$, $f_t$

1.6.8 Capacitances

$C_{ob}$, $C_{oe}$, $C_{ie}$, $C_{cb}$ (dir.)

1.6.9 Real Part of $h_{ie}$

$Re\, h_{ie}$

1.6.10 Switching Times

$t_d$, $t_r$, $t_s$, $t_f$

1.6.11 Saturation Stored Charge and Saturation Stored Charge Time Constant

$Q_s$, $\tau_s$

## 1.7 General Precautions

### 1.7.1 Instrumentation

Attention is called to the necessity, especially in tests involving low measurement currents and powers, of eliminating or correcting for errors due to the presence of the measurement instrumentation in the test circuits. This applies particularly to voltmeter currents, ammeter voltage-drops, and to stray capacitances, parasitic inductances and leakage currents introduced by test sockets, jigs, etc.

### 1.7.2 Maximum Ratings

The test conditions such as electrode voltages and currents and junction temperatures should be maintained within the maximum device ratings specified. These ratings are limiting values which, if exceeded, may result in permanent changes in the characteristics of the transistor. It should be recognized that some combinations of absolute maximum ratings cannot normally be attained simultaneously. When particular tests are required to extend somewhat beyond a

specified continuous maximum rating, such portions of the testing procedure should be performed as rapidly as possible.

1.7.3 Repeatability of Measurement

Care must be taken to insure that measured parameter values are repeatable within the precision of measurement after performance of any or all tests.

1.7.4 Polarities

The correct voltage polarities for the type of transistor (PNP or NPN) must be observed at all times. All of the measurement arrangements are shown in terms of PNP transistors for illustrative purposes.

1.7.5 Temperature Effects

Transistors are inherently temperature-sensitive devices. The ambient temperature and the internal temperature rise due to power dissipation in the device must be taken into account during all tests.

The ambient temperature should be specified and recorded to insure correlation of successive measurements on devices. Adequate precautions should be taken in the design of the test equipment to insure control of the junction temperatures. For example, pulse techniques may be required to insure that rated junction temperatures are not exceeded.

1.7.6 Spurious Current Surges

Precautions must be taken in handling and testing devices to insure that they are not subjected to static electric discharges or high electric fields.

## 2.0 Methods of Measurement

### 2.1 Static Characteristic Families

In accordance with the two-port network representation outlined in Section 1.3, input, output, and transfer characteristics may be measured to describe the junction

transistor. Methods for obtaining static characteristics are covered in Section 2.0 of "IRE Standards on Solid State Devices: Methods of Testing Transistors".[2]

2.2 Breakdown Voltages

When a junction is biased in the reverse direction, an increase in voltage will cause a relatively small increase in current until the breakdown voltage is approached. When the voltage applied reaches the breakdown voltage, a further small increase will cause a large increase in the current flowing across the junction.

Breakdown phenomena are, in general, reversible and do not lead to destruction or damage of the device unless the power dissipated in the high-current region of the breakdown characteristic is sufficient to elevate the junction temperature beyond acceptable maximum limits. However, in certain device types, permanent changes in the characteristics have been observed when breakdown voltages are exceeded. In these cases special precautions must be taken to eliminate spurious pulses or spikes in the testing apparatus.

The following sections describe procedures for determining actual breakdown voltage values. In many cases, for testing convenience, it may be sufficient to test the devices to assure that a minimum value of breakdown voltage is equalled or exceeded. All of the test circuits shown are applicable to this method of checking, except that the testing procedure would be modified with the bias supply voltages fixed at the desired minimum value of breakdown voltage, and the resultant current measured to insure that the specified current is not exceeded.

2.2.1 $BV_{CBO}$

The collector breakdown voltage may be determined using the general dc measurement arrangement shown in Fig. 2, with a short circuit between terminals C-C' and a constant-current collector supply.

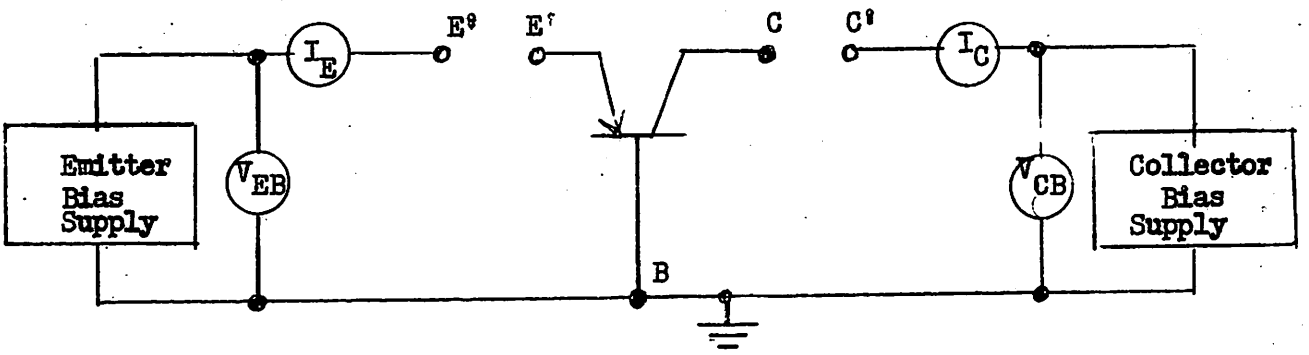



Fig. 2 - General DC Measurement Arrangement - Common Base

The collector breakdown voltage may be measured at a designated value of $I_C$ well above the normal collector cut-off current ($I_{CBO}$) of the device. With the emitter open-circuited, as previously specified, the applied collector current is increased until the designated value is reached; then the breakdown voltage is read on meter $V_{CB}$.

2.2.2 $BV_{EBO}$

The emitter breakdown voltage may be determined using the general dc measurement arrangement shown in Fig. 2, with a short circuit between terminals E-E' and a constant-current collector supply.

The emitter breakdown voltage may be measured at a designated value of $I_E$ well above the normal emitter cut-off current ($I_{EBO}$) of the device. With the collector open-circuited, as previously specified, the applied emitter current is increased until the designated value is reached; then the breakdown voltage is read on meter $V_{EB}$.

2.2.3 $BV_{CEO}$

The collector breakdown voltage in the common-emitter connection may be determined using the general dc measurement arrangement shown in Fig. 3, with a short circuit between terminals C-C' and a constant-current collector supply.

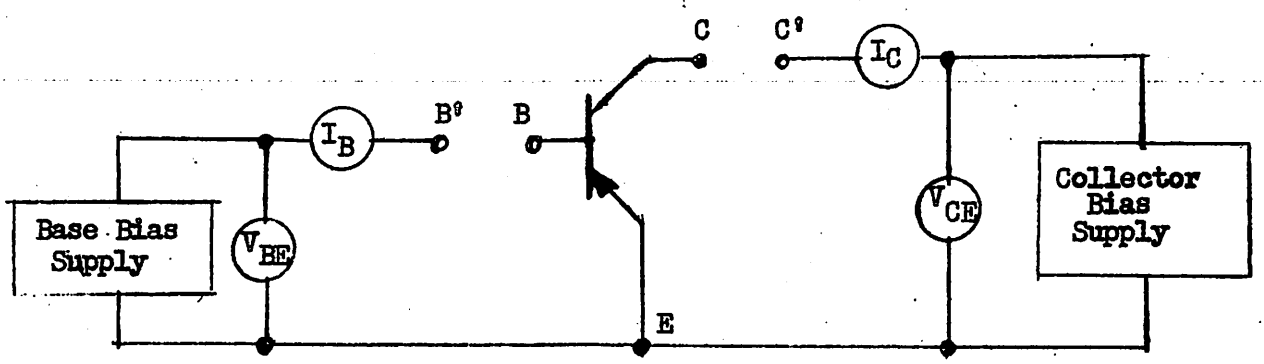



Fig. 3 - General DC Measurement Arrangement - Common Emitter

The collector breakdown voltage may be measured at a designated value of $I_C$ well above the normal collector cut-off current ($I_{CEO}$) of the device. With the base open-circuited, as previously specified, the applied collector current is increased until the designated value is reached; then the voltage is read on meter $V_{CE}$.

2.2.4 $BV_{CES}$

The collector breakdown voltage in the common-emitter connection with the base shorted to the emitter may be determined using the general dc measurement arrangement shown in Fig. 3, with terminals B-E and C-C' short-circuited, respectively, and a constant-current collector supply. The collector breakdown voltage may be measured at a designated value of $I_C$ well above the normal collector cut-off current ($I_{CES}$) of the device. With the base and emitter short-circuited, as previously specified, the applied collector current is increased until the designated value is reached; then the breakdown voltage is read on meter $V_{CE}$.

2.2.5 $BV_{CEX}$

It is frequently desired to place requirements on the collector breakdown voltage in the common-emitter connection with a bias voltage and/or a resistance between emitter and base electrodes.

The collector breakdown voltage under these conditions may be determined using the general dc measurement arrangement shown in Fig. 3 with a short circuit between terminals C-C', and either a short circuit or the specified resistance introduced between terminals B-B'. The base bias supply is usually constant-voltage and the collector supply constant-current. With the specified value of base-bias supply voltage indicated on the voltmeter $V_{BE}$ and the terminals B-B' either shorted or connected by means of the specified resistance, the applied collector current is increased until the designated value is reached; then the breakdown voltage is read on meter $V_{CE}$.

The same testing procedure may be used to measure the collector breakdown voltage where the test conditions require that the base electrode be connected to the emitter electrode by a resistor alone, without base-to-emitter bias. In this case the arrangement of Fig. 3 may be used, with the specified resistance introduced between terminals B-E, a short circuit between terminals C-C', and a constant-current collector supply.

2.2.6 $V_{RT}$

The reach-through voltage may be determined using the measurement arrangement shown in Fig. 4.

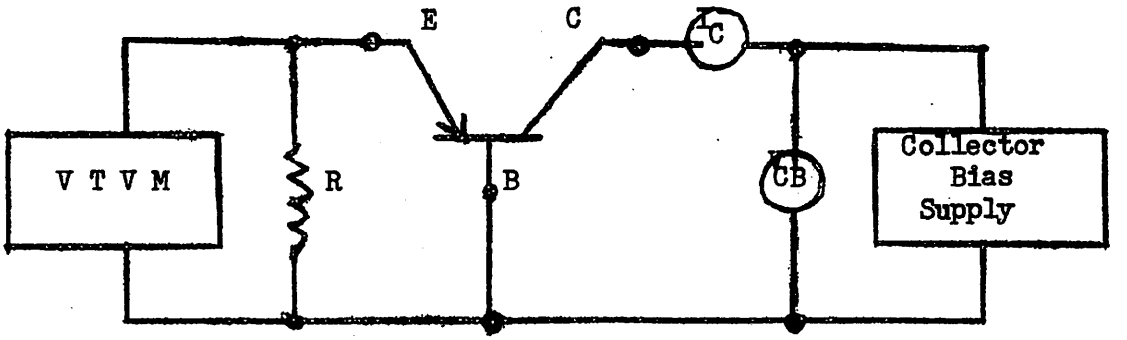



Fig. 4 - Measurement of Reach-Through Voltage $V_{RT}$

The circuit comprises a constant-current source of collector biasing potential with collector current and voltage monitoring facilities. The emitter is terminated in a fixed high resistance (e.g., 1 megohm) to provide a reasonably constant terminating impedance. The high impedance voltmeter monitors the emitter floating potential ($V_{EBF}$). As the collector potential is increased, the emitter floating potential remains relatively constant at a low value until the reach-through voltage is attained. The emitter potential then increases almost linearly with further increases of the collector voltage. When a specified value of emitter floating potential is reached, the voltage indicated by meter $V_{CB}$ may be used to calculate the reach-through voltage, using the relationship:

$$V_{RT} \approx V_{CB} - V_{EBF} \qquad (1)$$

Alternatively, the reach-through voltage may be determined using the general dc measurement arrangement shown in Fig. 3, with terminals B-B' and C-C' short-circuited, respectively. With the specified reverse base-bias voltage from a constant-voltage source indicated on voltmeter $V_{BE}$, the collector current supply is increased until a designated value is reached; then, the voltage indicated by meter $V_{CE}$ is the reach-through voltage.

2.2.7 $V_{CE}$ (sus)

The sustaining voltage in the common-emitter connection may be determined using the general dc measurement arrangement shown in Fig. 3 with terminals C-C' and B-B' short-circuited, respectively, and constant-current supplies. The sustaining voltage may be measured at specified values of $I_C$ and $I_B$ chosen to insure operation in the breakdown region. With the base current at its specified value, the collector current is increased to the specified value; then the sustaining voltage is read on meter $V_{CE}$.

2.2.8 Precautions

Test conditions for all breakdown voltage measurements should be such that absolute maximum ratings are not exceeded. The precautions should include limits on maximum instantaneous currents and applied voltages. High series resistances (constant-current bias supplies) and low capacitances are usually required.

2.3 Reverse Cut-off Currents

2.3.1 $I_{CBO}$, $I_{CBS}$, $I_{EBO}$ and $I_{EBS}$

The cut-off currents $I_{CBO}$, $I_{CBS}$, $I_{EBO}$, and $I_{EBS}$, may be measured using the general dc measurement arrangement shown in Fig. 2. $I_{CBO}$ is the collector current at a specified value of $V_{CB}$, with a short circuit between terminals C-C' and a constant-voltage collector supply.. Similarly, $I_{EBO}$ is the emitter current at a specified value of $V_{EB}$, with a short circuit between terminals E-E' and a constant-voltage emitter supply.

$I_{CBS}$ is the collector current at a specified value of $V_{CB}$, with terminals C-C' and E-B short-circuited, respectively and constant-voltage collector supply. Similarly, $I_{EBS}$ is the emitter current at a specified value of $V_{EB}$, with terminals E-E' and C-B short-circuited, respectively, and a constant-voltage emitter supply.

2.3.2 $I_{CEO}$, $I_{CES}$, $I_{BEO}$, and $I_{BES}$

The cut-off currents $I_{CEO}$, $I_{CES}$, $I_{BEO}$, and $I_{BES}$ may be measured using the generalized dc measurement arrangement shown in Fig. 3. $I_{CEO}$ is the collector current at a specified value of $V_{CE}$, with a short circuit between terminals C-C' and a constant-voltage collector supply. Similarly, $I_{BEO}$ is the base current at a specified value of $V_{BE}$, with a short circuit between terminals B-B' and a constant-voltage emitter supply. $I_{CES}$ is the collector current at a specified value of $V_{CE}$, with terminals C-C' and B-E short-circuited, respectively and a constant-voltage collector supply. Similarly, $I_{BES}$ is the base current at a specified value of $V_{BE}$, with terminals B-B' and C-E short-circuited, respectively, and a constant-voltage emitter supply.

It should be noted that

$$|I_{CBS}| = |I_{CES}| \qquad (2a)$$

$$|I_{EBO}| = |I_{BEC}| \qquad (2b)$$

Consequently, these cut-off currents can be measured with either the common-base or common-emitter arrangement.

2.3.3 $I_{CEX}$ and $I_{BEX}$

It is frequently desired to place requirements on the collector and emitter cut-off currents in the common-emitter and common-collector connections with the opposite electrode reverse- or forward-biased to approximate actual operating conditions.

The collector cut-off current $I_{CEX}$ may be measured using the general dc measurement arrangement of Fig. 3, with terminals B-B' and C-C' short-circuited, respectively. The base bias supply is usually constant-voltage and the collector supply constant-current. $I_{CEX}$ is the collector-to-emitter current at a speci-

fied value of $V_{CE}$, with the designated value of base-to-emitter bias voltage indicated on the voltmeter $V_{BE}$.

The cut-off current $I_{BEX}$ may be measured using the general dc measurement arrangement of Fig. 3, with terminals B-B' and C-C' short-circuited, respectively. The collector supply is usually constant-voltage and the base supply constant-current. $I_{BEX}$ is the base-to-emitter current at a specified value of $V_{BE}$, with the designated value of collector-to-emitter bias voltage indicated on the voltmeter $V_{CE}$.

2.3.4 Precautions

The bias-supply voltage for a particular junction must have the correct polarity so that the junction is reverse-biased during reverse cut-off current measurements. For example, with respect to the common-base measurement arrangement, Fig. 2, $V_{CB}$ and $V_{EB}$ are negative for PNP transistors and positive for NPN transistors. In the case of the common-emitter measurement arrangement, Fig. 3, $V_{CE}$ is negative for PNP transistors and positive for NPN transistors, while $V_{BE}$ is positive for PNP transistors and negative for NPN transistors.

The bias-supply voltage for a particular junction must be less than the breakdown voltage of the junction. It is important to recognize that the cut-off currents of a junction transistor are extremely temperature sensitive. Consequently, the device temperature should be recorded when measuring these currents. This is particularly important when it is required to correlate data obtained over a relatively long period of time involving successive measurements on devices.

## 2.4 Saturation Voltages

When a transistor is operated in Region III, the emitter and collector junctions are forward voltage-biased, and the collector current is determined principally by the external circuit conditions.

2.4.1 $V_{CE}$ (sat)

The collector-to-emitter saturation voltage in the common-emitter connection may be determined using the general dc measurement arrangement shown in Fig. 3 with terminals B-B' and C-C' short-circuited, respectively, and constant-current supplies. The saturation voltage may be measured at designated values of $I_C$ and $I_B$ chosen to insure operation in the saturation region. With the base current at its designated value, the collector bias current is increased to the designated value; then the collector-to-emitter saturation voltage is read on meter $V_{CE}$.

2.4.2 $V_{BE}$ (sat)

The base-to-emitter saturation voltage in the common-emitter connection may be determined using the general dc measurement arrangement shown in Fig. 3 with terminals B-B' and C-C' short-circuited, respectively and constant-current supplies. The saturation voltage may be measured at designated values of $I_B$ and $I_C$ chosen to insure operation in the saturation region. With the base current at its designated value, the collector bias current is increased to the designated value; then the base-to-emitter saturation voltage is read on meter $V_{BE}$.

2.4.3 $V_{CB}$ (sat)

The collector-to-base saturation voltage in the common-base connection may be determined using the general dc measurement arrangement shown in Fig. 2 with terminals E-E' and C-C' short-circuited respectively, and constant-current supplies. The saturation voltage may be measured at designated values of $I_C$ and $I_E$ chosen to insure operation in the saturation region. With the emitter current at its designated value, the collector bias current is increased to the designated values then the collector-to-base saturation voltage is read on meter $V_{CB}$.

2.4.4 $V_{EB}$ (sat)

The emitter-to-base saturation voltage in the common-base connection may be determined using the general dc measurement arrangement shown in Fig. 2 with terminals E-E' and C-C' short-circuited respectively, and constant-current supplies. The saturation voltage may be measured at designated values of $I_E$ and $I_C$ chosen to insure operation in the saturation region. With the emitter current at its designated value, the collector bias current is increased to the designated value; then the emitter-to-base saturation voltage is read on meter $V_{EB}$.

2.4.5 Precautions

In saturation voltage measurements, using the general dc measurement arrangements of Figs. 2 and 3, provision should be made for shorting the current meters after adjustment to the desired levels since the voltage-drops across the current meters may be comparable with the saturation voltages. Alternatively, the voltmeter connections may be switched to the device terminals for these measurements.

2.5 Current Transfer Ratios, Transadmittance and Transconductance

2.5.1 Small-Signal Forward-Current Transfer Ratios ($h_{fe}$, $h_{fb}$)

Methods of test are described in Sections 3.5 and 3.6 of "IRE Standards on Solid-State Devices: Methods of Testing Transistors".[2] The operating-point bias conditions and frequency of measurement must be specified.

2.5.2 Transadmittance ($y_{fe}$) and Transconductance ($g_{fe}$)

Methods of test are described in Sections 3.5 and 3.6 of "IRE Standards on Solid-State Devices, Methods of Testing Transistors".[2] The operating-point bias conditions and frequency of measurement must be specified.

### 2.5.3 Large-Signal Current Transfer Ratios

Large-signal current transfer ratios useful for large-signal amplifier and switching characterization may be measured using the arrangements shown in Figs. 5 and 6.

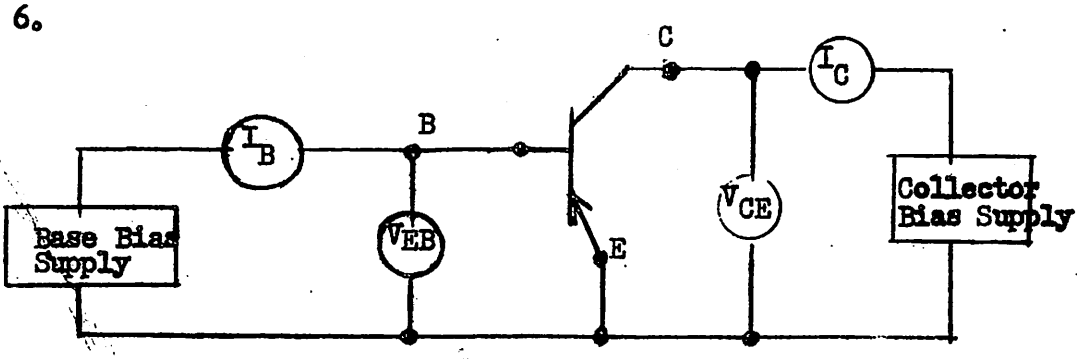



Fig. 5 Large-Signal Current Transfer Ratio Measurement-Arrangement I

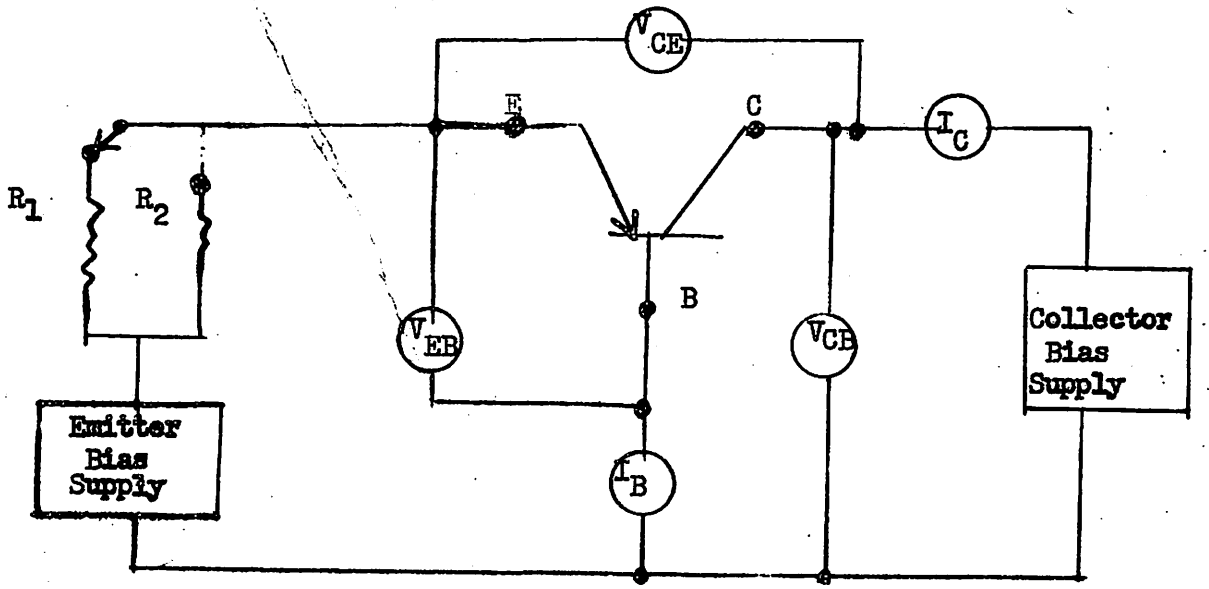



Fig. 6 Large-Signal Current Transfer Ratio Measurement-Arrangement II

2.5.3.1 $h_{FE}$

The static large-signal forward-current transfer ratio is usually specified at a given collector-to-emitter voltage ($V_{CE}$) and collector current $I_C$, or base current $I_B$. Using the arrangement shown in Fig. 5, $h_{FE}$ may be measured by applying a voltage of the desired magnitude between collector and emitter terminals and increasing the base current until the specified collector current $I_C$ or base current $I_B$ is reached.

Alternatively, the arrangement shown in Fig. 6 may be used to measure $h_{FE}$. The emitter bias supply and series resistor $R_1$ are adjusted to provide the desired current $I_C$ and the collector voltage supply is adjusted to provide the specified voltage $V_{CE}$. The static forward-current transfer ratio is defined by the ratio of the collector current $I_C$ to the base current $I_B$.

2.5.3.2 $h_{FE}$ (inv)

The inverse static large-signal forward-current transfer ratio is usually specified at a given collector-to-emitter voltage ($V_{CE}$) and emitter current $I_E$, or base current $I_B$. Using the measurement arrangements shown in Figs. 5 and 6, $h_{FE}$ (inv) may be measured following the procedures described in Section 2.5.3.1, except that the devices are inserted in the test circuitry with collector and emitter electrodes inverted. The inverse static large-signal forward-current transfer ratio is defined by the ratio of the emitter current $I_E$ to the base current $I_B$.

2.5.3.3 $h_{FE}$ ($\Delta$)

The large-signal forward-current transfer ratio $h_{FE}$ ($\Delta$) is usually specified at given collector-to-emitter voltages ($V_{CE}$) over ranges of collector and base currents. This ratio may be measured using the arrangement shown in Fig. 6 by applying a constant current of the desired magnitude to the emitter

electrode by means of the emitter bias supply and a suitably proportioned series resistor, $R_1$. The collector voltage supply is adjusted to provide the specified voltage $V_{CE}$. Both $I_C$ and $I_B$ are measured. The emitter electrode is then switched to the other resistor, $R_2$, to provide a higher emitter current than formerly passed through the devices; the collector supply is readjusted to provide the specified $V_{CE}$, and $I_C$ and $I_B$ are again measured. $R_1$ and $R_2$ are proportioned to cover the operating range of interest. The large-signal forward-current transfer ratio $h_{FE}$ ($\Delta$) is defined by the following relationship:

$$h_{FE}\ (\Delta) = \frac{I_{C_2} - I_{C_1}}{I_{B_2} - I_{B_1}} \qquad (3)$$

## 2.6 Input Resistances

The static and large-signal input resistances $h_{IE}$ and $h_{IE}$ and $h_{IE}$ ($\Delta$), useful for amplifier and switching characterizations, may be measured using the arrangement shown in Fig. 6.

### 2.6.1 $h_{IE}$

The static input resistance $h_{IE}$ may be evaluated under the same test conditions as outlined in Section 2.5.3.1, measuring the base-to-emitter voltage and base current. The static input resistance is defined by the quotient of the base-to-emitter voltage divided by the base current.

### 2.6.2 $h_{IE}$ ($\Delta$)

The large-signal input resistance $h_{IE}$ ($\Delta$) may be evaluated under the same test conditions as outlined in Section 2.5.3.2, measuring base-to emitter voltages and base currents at the desired operating points. The large-signal input resistance $h_{IE}$ ($\Delta$) is defined by the following relationship:

$$h_{IE}\ (\Delta) = \frac{V_{EB_2} - V_{EB_1}}{I_{B_2} - I_{B_1}} \qquad (4)$$

2.6.3 Precautions

The large-signal measurements covered by the measurement circuits of Figs. 5 and 6 are frequently made on devices capable of dissipating watts of power, using external heat sinks. It is common practice to use heat transfer agents and spring clips to improve the heat transfer between device and heat sink. The temperature of the device mounting may be monitored by a thermocouple. Care must be taken to minimize the voltage drops in the leads connecting the measurement instrumentation between device electrodes and biasing supplies. The measurements performed on higher power devices are usually made with low applied collector voltages to reduce the internal power dissipation, thus limiting the internal temperature rise of the device.

Pulse techniques may be employed, using low repetition rates and pulse widths consistent with device frequency limitations, to facilitate testing under maximum current conditions without exceeding maximum junction temperatures.

## 2.7 Cut-off and Unity Current Transfer Ratio Frequencies

Terminal parameter measurements on higher-frequency devices, particularly on complex device structures, indicate that simplified equivalent circuits may not completely describe the behavior of the device. In large-signal and switching applications particularly, the forward-current transfer ratio vs. frequency characteristics must be adequately described and characterized.

### 2.7.1 $f_{hfb}$

Methods of measuring $h_{fb}$ as a function of frequency are described in Sections 3.5 and 3.6 of IRE Standards on Solid-State Devices, Methods of Testing Transistors.[2] The dc biasing conditions defining the operating point at which the measurement is to be made must be specified. As shown in Fig. 7 $|h_{fb}|$ is relatively constant at low frequencies; as the frequency of measurement is

increased, $h_{fb}$ decreases at a rate approaching an asymptote of 6 db/octave. The frequency at which $h_{fb}$ equals $\sqrt{2}/2$ of its low frequency value is defined as $f_{hfb}$.

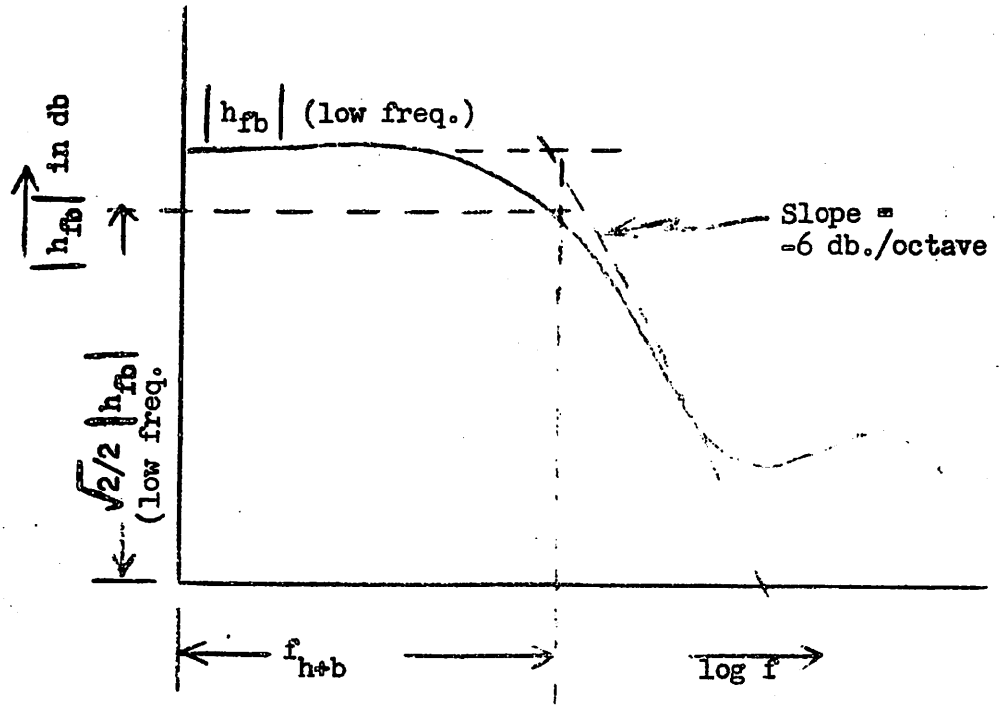



Fig. 7 Typical Forward-Current Transfer Ratio vs. Frequency Characteristic - Common Base

2.7.2 $f_{hfe}$, $f_l$, $f_t$

Methods of measuring $h_{fe}$ as a function of frequency are described in Sections 3.5 and 3.6 of IRE Standards on Solid State Devices, Methods of Testing Transistors.[2] The dc biasing conditions defining the operating point at which the measurement is to be made must be specified. As shown in Fig. 8, $|h_{fe}|$ is relatively constant at low frequencies, as the frequency of measurement is increased, $|h_{fe}|$ decreases at a rate approaching an asymptote of approximately 6 db/octave. The frequency at which $|h_{fe}|$ equals $\sqrt{2}/2$ of its low frequency value is $f_{hfe}$.

The frequency at which $|h_{fe}|$ equals unity ($|h_{fe}|$ in db = 0) is $f_1$.

The product $f|h_{fe}|$ is $f_t$ provided that the measurement frequency f is substantially greater than $f_{hfe}$.

A useful criterion for establishing the measurement frequency is based upon the magnitude of the forward-current transfer ratio, as shown in (5)

$$f_t > f \gg f_{hfe}$$

$$0.3\,|h_{fe}|\,(\text{low freq.}) > |h_{fe}|\ \text{meas.} > 2 \qquad (5)$$

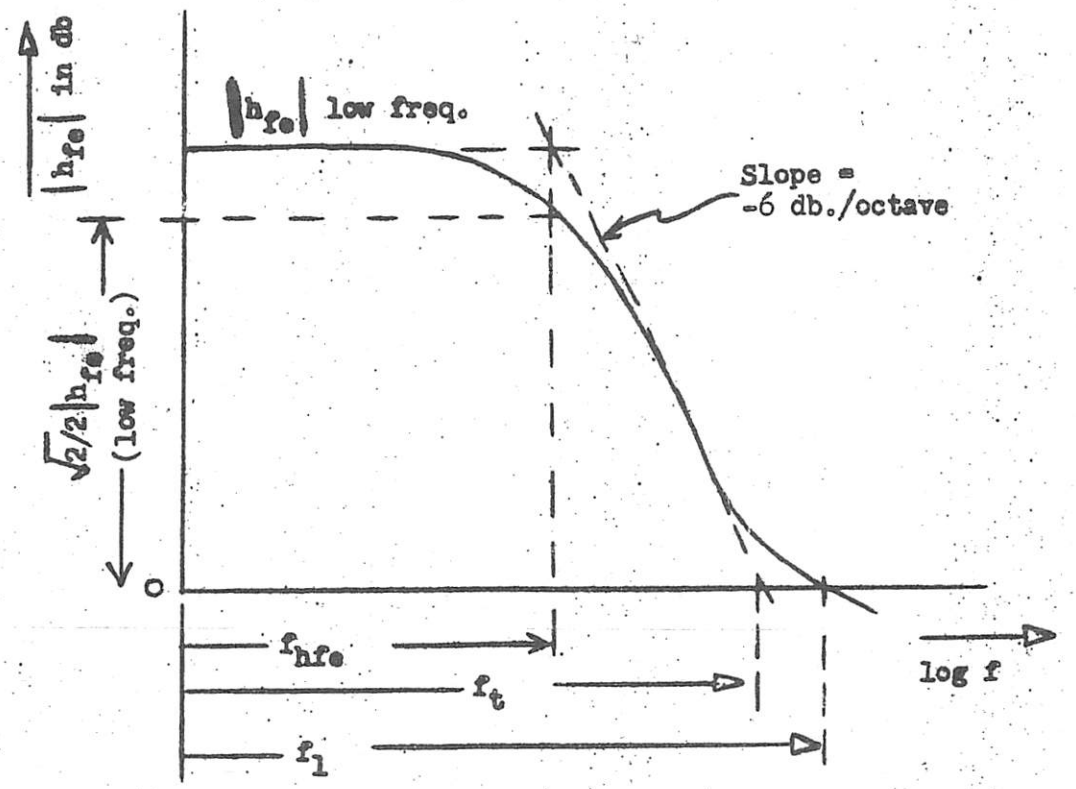



Fig. 8 Typical Forward-Current Transfer Ratio vs. Frequency Characteristic - Common Emitter

2.7.3 Precautions

Care should be taken in interpreting [illegible] $f_{hfb}$ measurements. Due to direct transmission of signal from emitter to collector at frequencies greater than $f_{hfb}$, the short-circuit forward-current transfer ratio $h_{fb}$ may exceed the values predicted by the 6 db/octave asymptote as indicated in Fig. 8.

It is possible, in certain devices, for $h_{fb}$ to exhibit a secondary peak with a value exceeding unity.

## 2.8 Capacitances

### 2.8.1 $C_{ob}$, $C_{oe}$

The output capacitances $C_{ob}$ and $C_{oe}$ may be measured by resonance or bridge methods described in Section 3.5.5.10 of IRE Standards on Solid-State Devices, Methods of Testing Transistors.[2] Alternatively, the output capacitances may be determined as the shunt susceptive part of the output admittance using the method of measurement described in Section 3.5.7.5, same reference. The dc biasing conditions defining the operating point at which the measurement is to be made, and the measurement frequency, must be specified.

### 2.8.2 $C_{ie}$

The input capacitance may be measured by resonance or bridge methods described in Section 3.5.5.10 of IRE Standards on Solid-State Devices, Methods of Testing Transistors.[2] The measurement frequency and the dc biasing conditions defining the operating point must be specified.

### 2.8.3 $C_{cb}$ (dir.)

The direct inter-terminal capacitance between the collector and the base may be measured by using a direct-capacitance bridge[7], with the emitter terminal grounded to the common shield.

Alternatively, the following two-terminal capacitances can be measured by resonance or bridge methods described in Section 3.5 of "IRE Standards on Solid-State Devices: Methods of Testing Transistors".[2] and the direct capacitance can be calculated using the following relationship.:

$$C_{cb}(\text{dir.}) = \frac{C_1 + C_2 - C_3}{2} \qquad (6)$$

7. "IRE Standards on Electron Tubes: Methods of Testing", 1950 (50 IRE 7. S2) Sec. 7.1 Proc. IRE Vol. 38 pp 918-1093, August-September, 1950

where:

$C_1$ is the capacitance between the collector terminal and ground, with base emitter terminals grounded.

$C_2$ is the capacitance between the base terminal and ground, with collector and emitter-terminals grounded.

$C_3$ is the capacitance between the collector and base terminals strapped together and ground, with the emitter-terminal grounded.

The measurement frequency and the dc biasing conditions defining the operating point must be specified.

2.8.4 Precautions

The shunt capacitance introduced by the test circuitry and mounting jigs should be kept to a minimum and its value subtracted from the measured capacitance. The measured value should be corrected if it is necessary to use a dc blocking capacitor for testing convenience.

## 2.9 Real Part of $h_{ie}$ (Re $h_{ie}$)

The high frequency performance of transistors is usually limited by the series extrinsic base resistance $r_b$, the parallel collector-base capacitance, carrier transit time and emitter transition capacitance. Often the extrinsic base resistance $r_b$ is taken to be equal to Re $h_{ie}$ at a frequency sufficiently high that Re $h_{ie}$ is essentially independent of frequency (See Fig. 9). This, however, implies that the device can be represented by one of the simple equivalent circuits, such as the hybrid pi[8]. If such an equivalent circuit is not valid for the particular device configuration, the locus of $h_{ie}$ will deviate from the semi-circle as shown by the dashed lines in Fig. 9.

### 2.9.1 Re $h_{ie}$

The resistive and reactive components of the short-circuit input impedance may be measured by any of the test methods described in Sections 3.5.6

8. L.J.Giacoletto "The Study and Design of Alloyed-Junction Transistors", 1954 IRE Conv. Rec., Vol. 2, Pt. 3, p. 102; 1954
L.J.Giacoletto, "Study of p-n-p Alloy Junction Transistor from DC Through Medium Frequencies," RCA Review, Vol. 15, pp. 506-562

and 3.5.7 of IRE Standard on Solid State Devices, Methods of Testing Transistors.[2] A typical plot in the $h_{ie}$ complex plane showing the frequency dependence of the components[7] of $h_{ie}$ is shown in Fig. 9.

2.9.2 Precautions

Care should be taken to either eliminate or correct for any external inductance placed in series with the emitter, as Re $h_{ie}$ is very sensitive to this particular parasitic parameter at high frequencies. Base lead inductance and stray capacitances should also be considered, although they are relatively less important.

2.10 Dynamic Measurements

2.10.1 Switching Times

The switching speed of a transistor may be characterized by the delay, rise, storage[9] and fall times ($t_d$, $t_r$, $t_s$, and $t_f$, respectively).[4,5] The pulse characteristics defining these times are shown in Fig. 10.

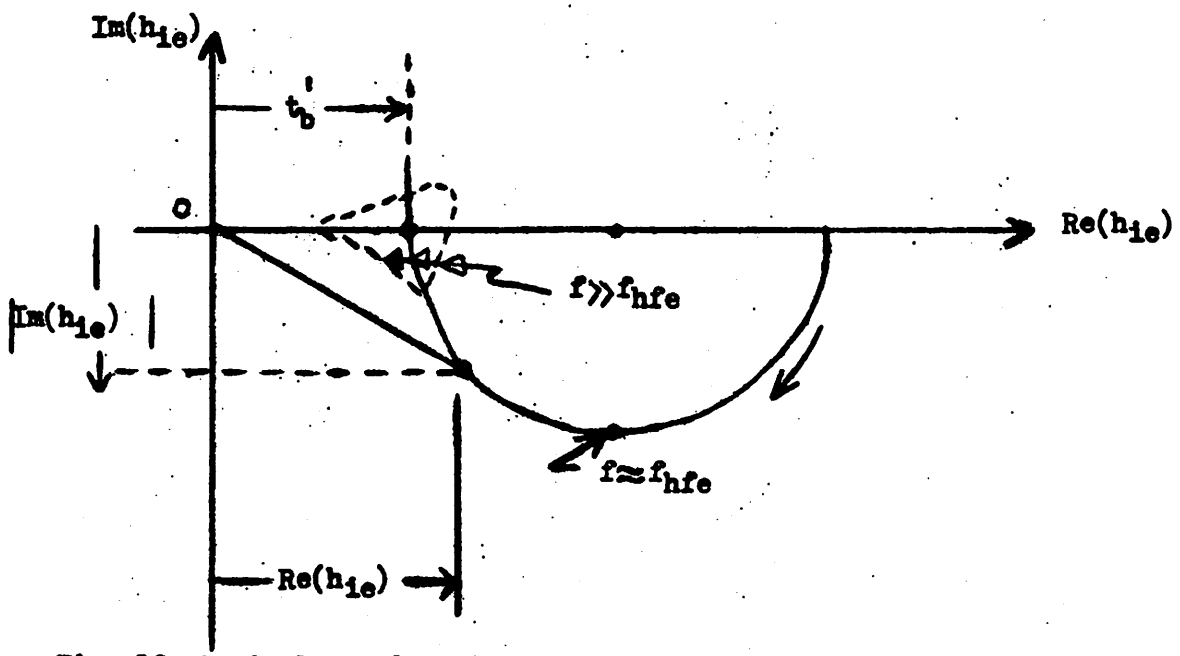



Fig. 19 Typical Complex Plane Representation of Short-Circuit Input Impedance $h_{ie}$

7. R. P. Abraham, "Transistor Behavior at High Frequencies", IRE Trans. on Elect. Dev. Vol. ED - 7, No. 1, pp. 59-69, 1960.

9. R. P. Nanavati, "Prediction of Storage Time in Junction Transistors", IRE Trans. on Elect. Dev., Vol. EO-7, No. 1, pp. 9-15, 1960

transistor to be measured. Typical input voltage driving conditions are illustrated in Fig. 12. The output waveform is monitored by means of an oscilloscope or other suitable output detector to determine the various switching times.

2.10.1.3 Combinational Drive

A useful combination of constant-current and constant-voltage drive conditions which may be used to approximate particular operational requirements is afforded by the measurement arrangement shown in Fig. 11 with terminals B-B' short-circuited. In this case, the turn-off times ($t_s$ and $t_f$) are obtained with a constant-current ON condition and a constant voltage "turn-off" impulse fed to the base through the capacitor C. The transistor is operated in the common-emitter connection with a specified collector load resistance $R_C$ and collector bias supply voltage $V_{CC}$. The output waveform is monitored by means of an oscilloscope or other suitable output detector to determine the various switching times.

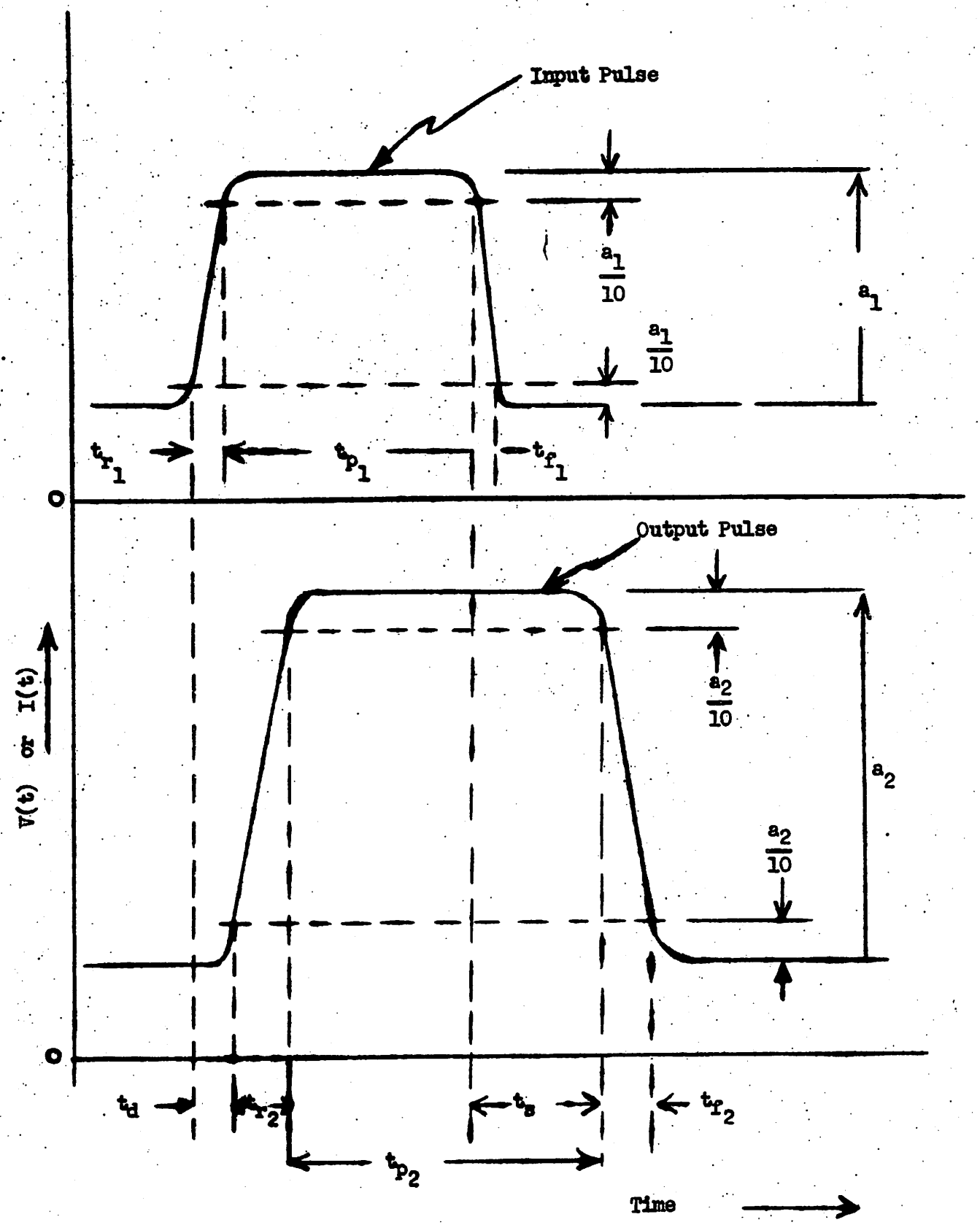



Fig. 10 Pulse Characteristics

$a_1$ = Input Pulse Amplitude

$a_2$ = Output Pulse Amplitude

$t_r$ = Pulse Rise Time

$t_p$ = Pulse Time

$t_d$ = Pulse Delay Time

$t_s$ = Pulse Storage Time

$t_f$ = Pulse Fall Time

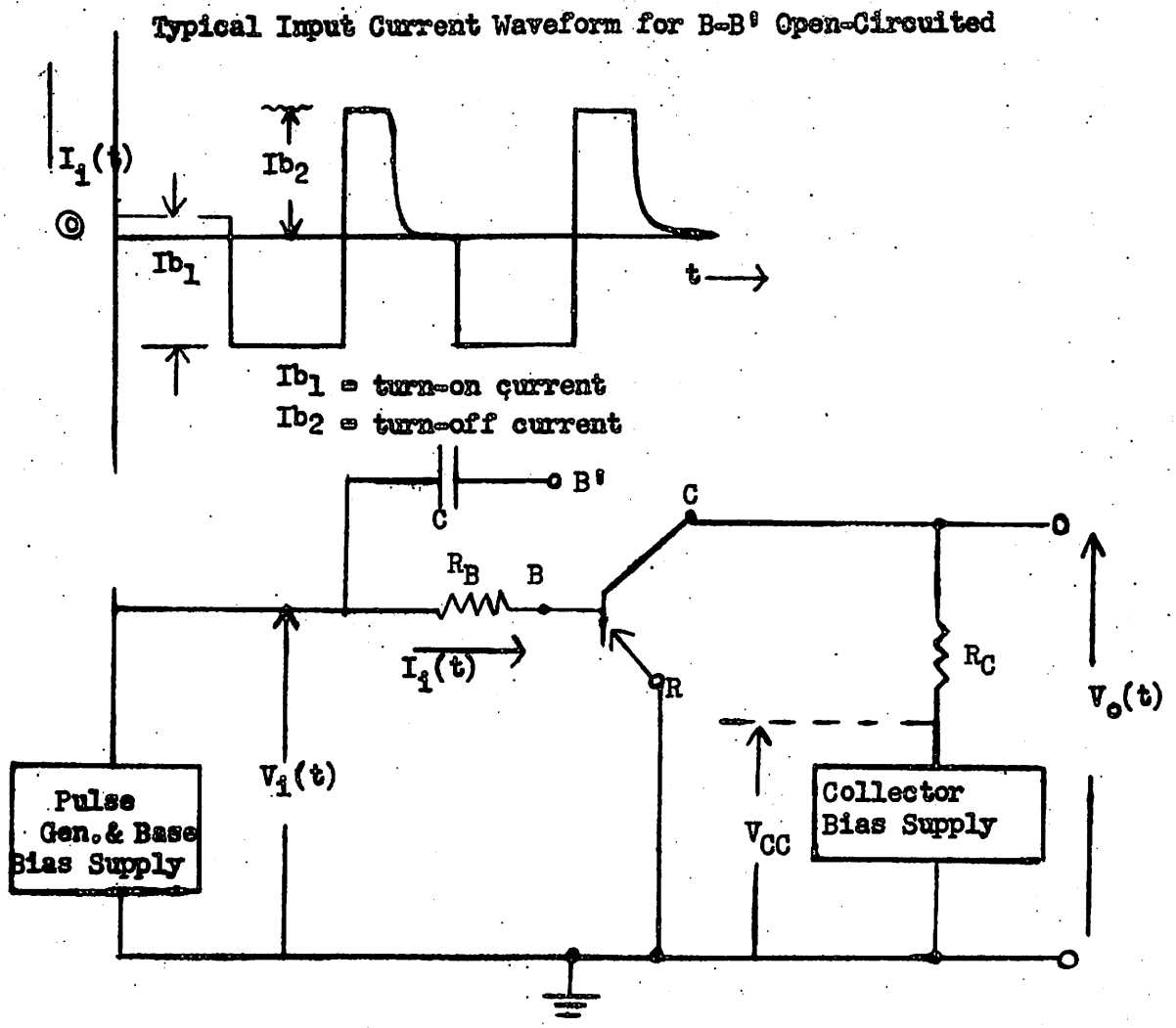



Fig. 11 Arrangement for Measuring Switching Times Using Constant-Current Drive

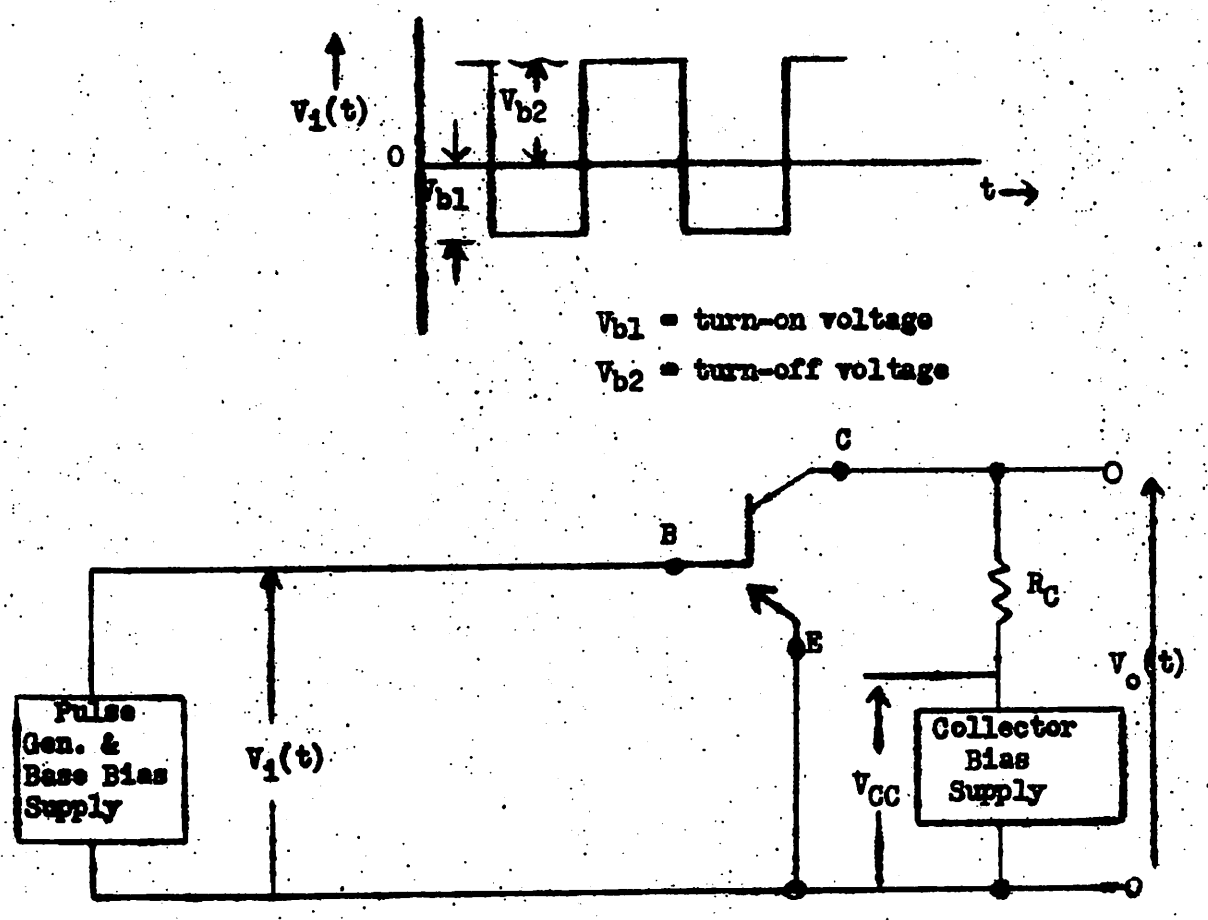



Fig. 12 Arrangement for Measuring Switching Times Using Constant-Voltage Drive

2.10.2 Saturation-Stored Charge Measurements ($Q_s$)

The stored charge is useful as an indication of the speed of recovery of a transistor from an ON to an OFF state, where in the ON condition, operation in Region III is assumed. The saturation stored charge may be defined as the total charge stored in the base and collector regions of the transistor for the ON condition specified by the collector current and the base current drive.

The saturation stored charge may be measured using the circuit arrangement shown in Fig. 13. The transistor is operated with zero dc collector current, and the emitter current $I_E$ is adjusted to the specified dc value. The input voltage $\left[ V_i (t) \right]$ pulse level impressed upon the base terminal is set to provide the prescribed back-biasing to periodically switch the diode CRI between conduction and non-conduction. The emitter is thereby open-circuited and the stored charge is transferred to the capacitor C in the collector circuit. The diode CRI in series with the emitter serves to isolate the transistor from the dc emitter current source during the non-conduction period and should be selected for high-speed switching properties, (i.e., low storage, fast recovery, etc.) Alternatively, a suitable electron tube diode may be used.

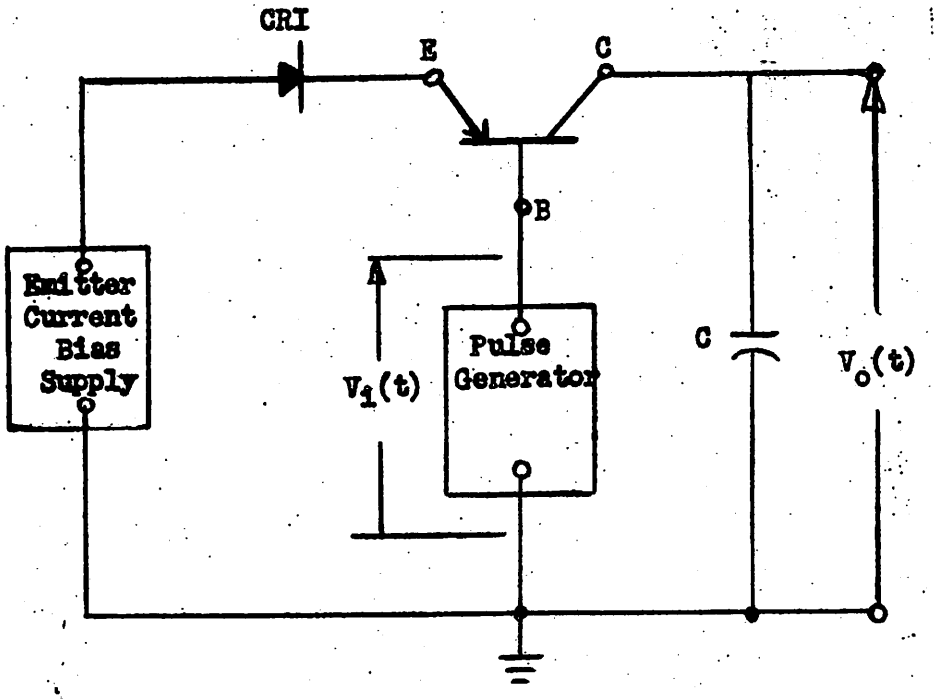
The peak output voltage $V_o$ across the capacitor C may be measured with an oscilloscope or other suitable peak pulse detector. The saturation stored charge Qs is the product of the peak pulse output voltage and the total capacitance between collector and ground.

$$Qs = V_o (C + C_s) \qquad (7)$$

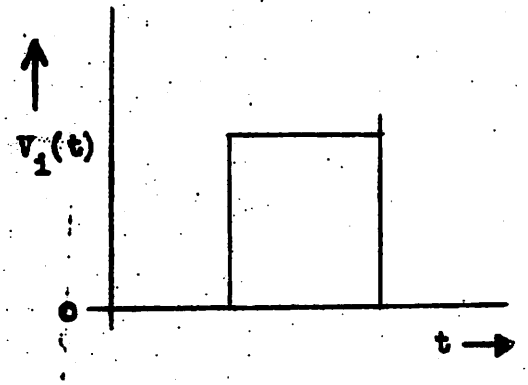
where : $V_o$ is the peak output voltage

C is the capacitor value

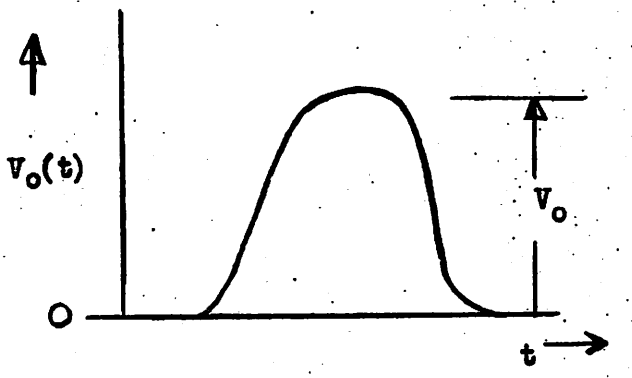
$C_s$ is the stray capacitance, including measurement probe capacitance




Measurement Circuit
Fig. 13a




Base Drive Voltage
Fig. 13b




Collector Output Voltage
Fig. 13c

Fig. 13 Measurement Circuit for Saturation Stored Charge $Q_s$ and Typical Waveforms - First Method

Typical waveforms are shown with the measurement circuit in Fig. 13.

Alternatively, the saturation stored charge for any specified value of collector current and base current drive may be measured using the arrangement shown in Fig. 14. The base driving current and ON collector current may be approximated using the relationships:

$$I_B = \frac{V_1}{R_B} \quad \text{and} \quad I_C = \frac{V_{CC}}{R_C} \tag{8}$$

where: $V_1$ is the peak input voltage. The capacitor C is adjusted for the minimum capacitance required to achieve the desired output waveform $V_o$ (t) having a sharp turn-off characteristic as illustrated in Fig. 14c. The saturation stored charge Qs is the product of the peak input voltage ($V_1$) and the amplitude ($V_1$) and the capacitance C.

$$Q_s = V_1 C \tag{9}$$

2.10.3 Saturation Stored-Charge Time Constant Measurements ($\tau_s$)

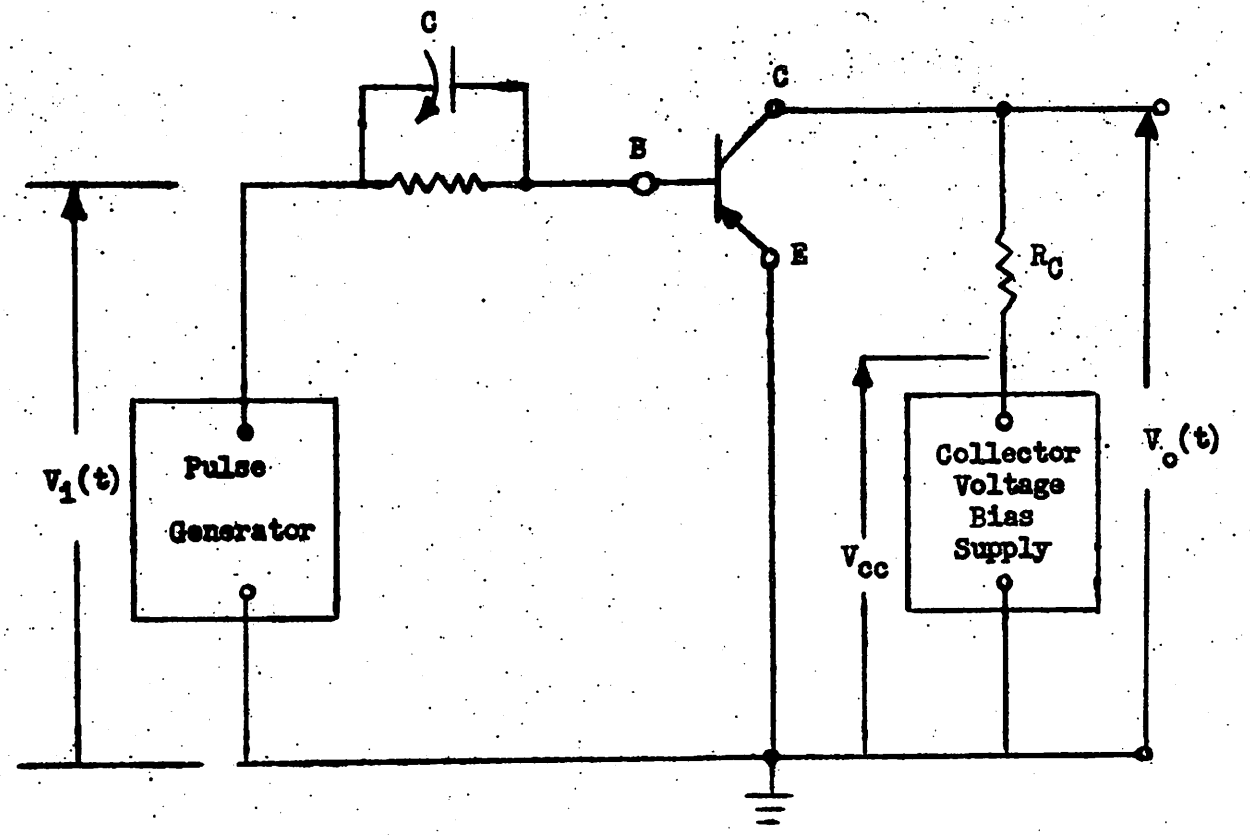
The saturation stored-charge time constant ($\tau_s$) is proportional to the excess charge stored per unit of excess drive (base) current and may be used to characterize the saturation charge storage properties of a transistor. The following relationship may be used:

$$\tau_s = \frac{Q_s}{I_{B1} - I_{Bs}} \tag{10}$$

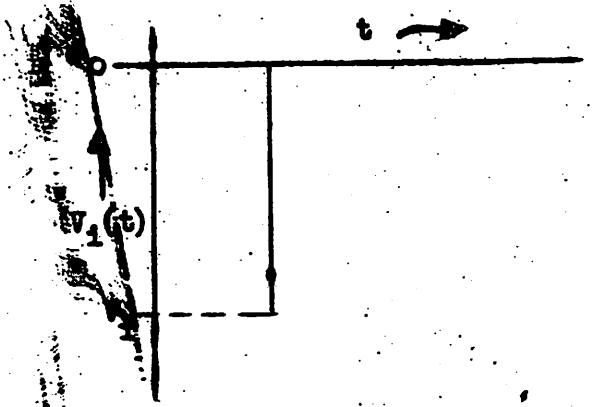
where: $Q_s$ is the saturation stored charge in micro-microcoulombs

$I_{B1}$ is the base current drive in the ON condition

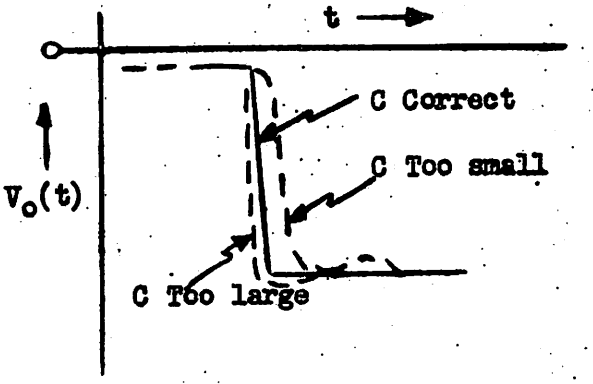
$I_{Bs}$ is the minimum base current to obtain saturation.




Measurement Circuit
Fig. 14a




Base Drive Voltage
Fig. 14b




Collector Output Voltage
Fig. 14c

Fig. 14 Measurement Circuit for Saturation Stored Charge $Q_s$ and Typical Waveforms - Second Method

The minimum base current to obtain saturation should be evaluated in terms of the particular circuit under consideration and may be calculated by:

$$I_{BS} = \frac{I_{C1}}{h_{FE}} \qquad (11)$$

where: $I_{C1}$ is the ON collector current

$h_{FE}$ is the static value of the forward current transfer ratio in the active region near saturation

It should be noted that if the first method of measurement of Qs outlined in Section 2.10.2 is used, $I_{Bs} = 0$ since $I_{C1} = 0$.

An alternate method of measuring the saturation stored-charge time constant ($\tau s$) is to measure the storage time ($t_s$) as outlined in Section 2.10.1 and calculate $\tau_s$ using the relationship:

$$\tau s = \frac{t_s}{\ln \left| \frac{I_{B1} - I_{B2}}{I_{Bs} - I_{B2}} \right|} \qquad (12)$$

In the above expression $I_{B2}$ is the base current drive during the interval the transistor is being removed from saturation and the other variables are as previously defined. If $I_{B2}$ is a reverse current, the sign is negative.

2.10.4 Precautions

The time constant ($\tau s$) is not necessarily the storage time in any particular circuit. The storage time ($t_s$) of a transistor under actual operating conditions may be calculated using (12).

In switching time measurements using the measurement arrangement of Fig. 11, specific attention to the absolute values of the bias supply potentials, pulse amplitudes, and the precision of the base and collector resistances is required if correlation between measurements made on test equipment instrumentation is to be achieved. These precautions, in general, hold for all time-based measurement instrumentation. In addition, the effects of stray capacitance introduced by the test probes of monitoring oscilloscopes must be taken into consideration.

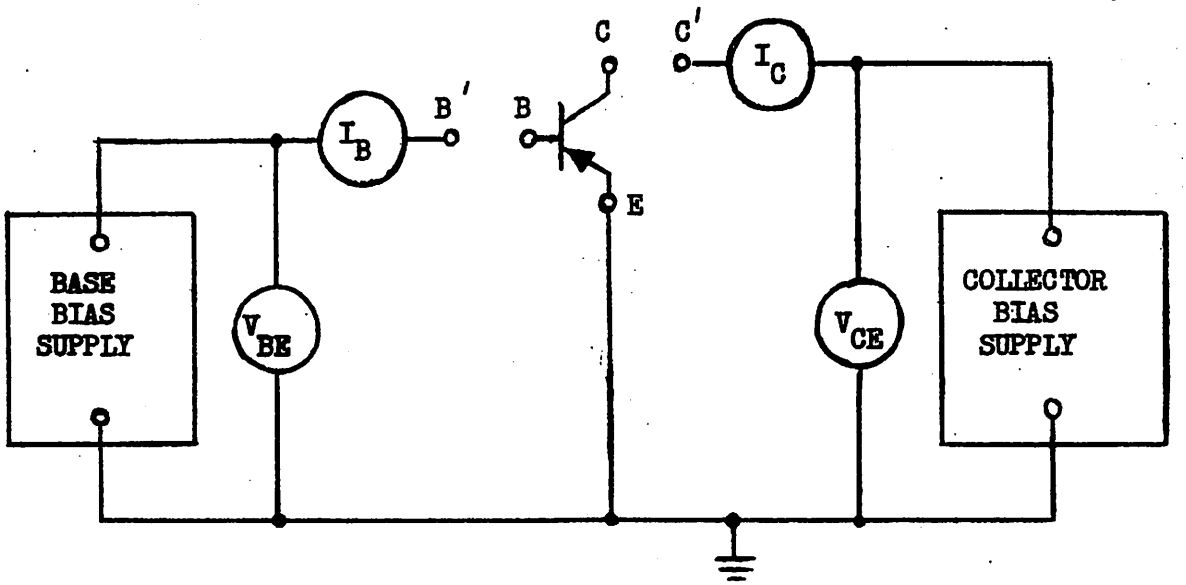



FIG. 3 GENERAL DC MEASUREMENT ARRANGEMENT - COMMON EMITTER

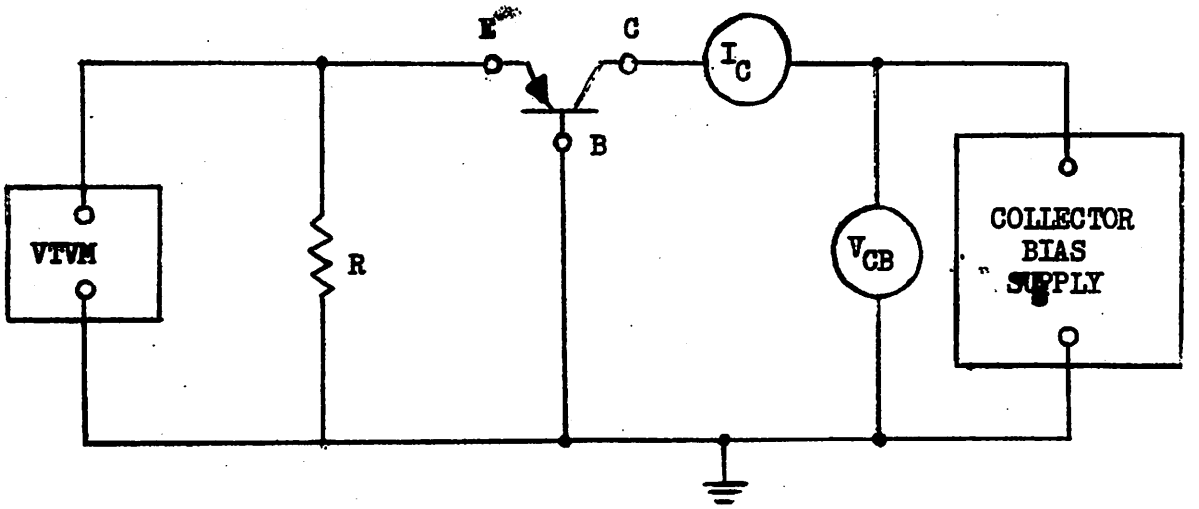



FIG.4 MEASUREMENT OF REACH - THROUGH VOLTAGE - $V_{RT}$

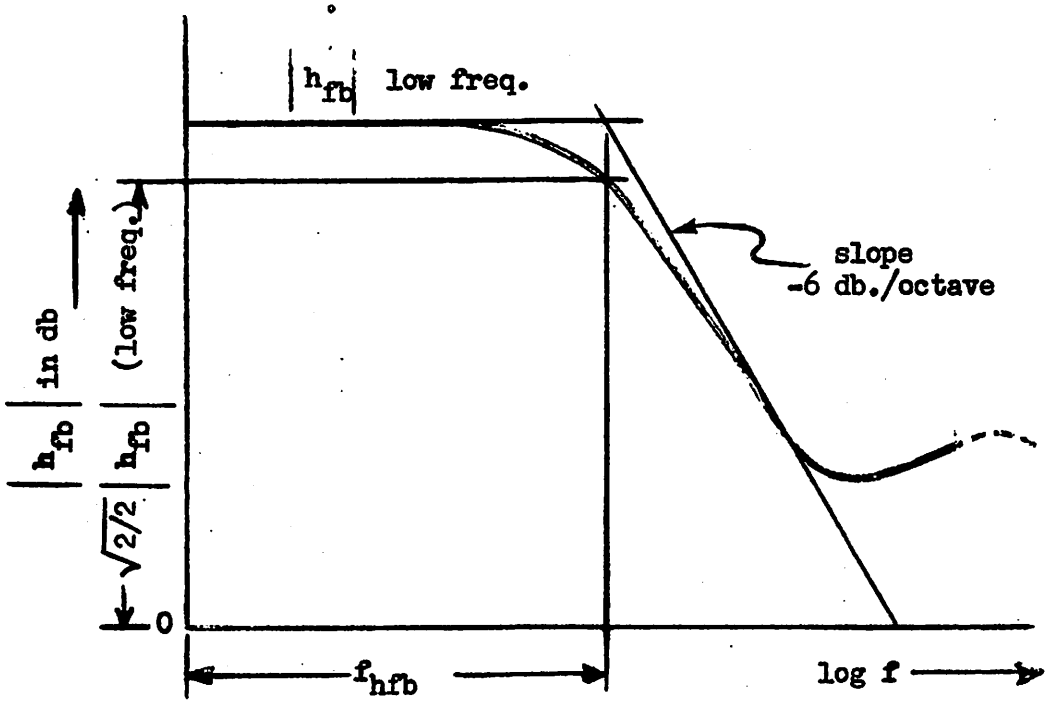



FIG. 7 TYPICAL FORWARD - CURRENT TRANSFER RATIO vs. FREQUENCY CHARACTERISTIC - COMMON BASE

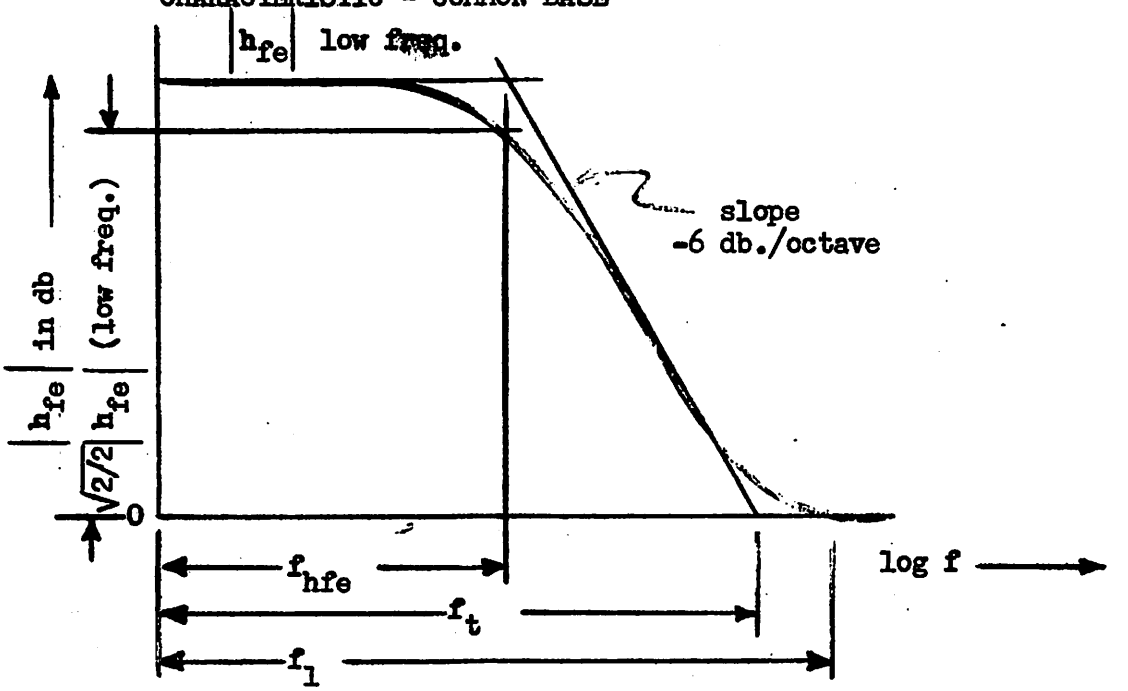



FIG. 8 TYPICAL FORWARD-- CURRENT TRANSFER RATIO vs. FREQUENCY CHARACTERISTIC - COMMON EMITTER

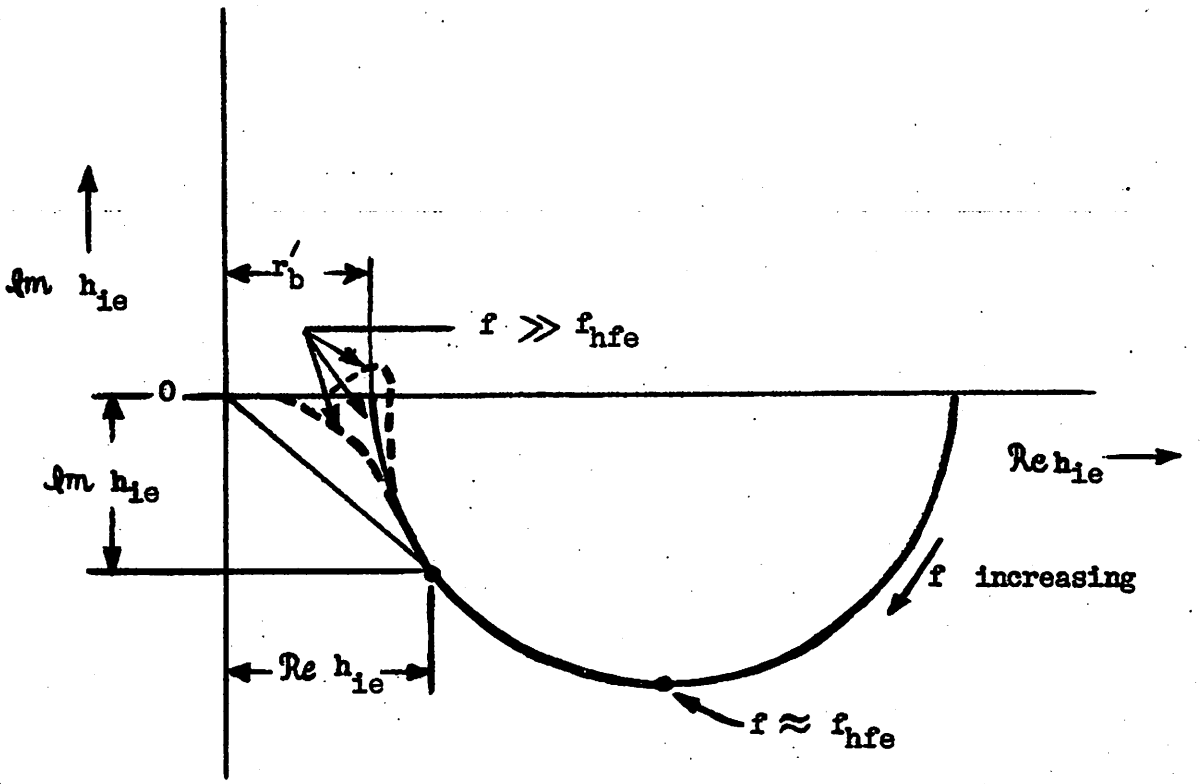
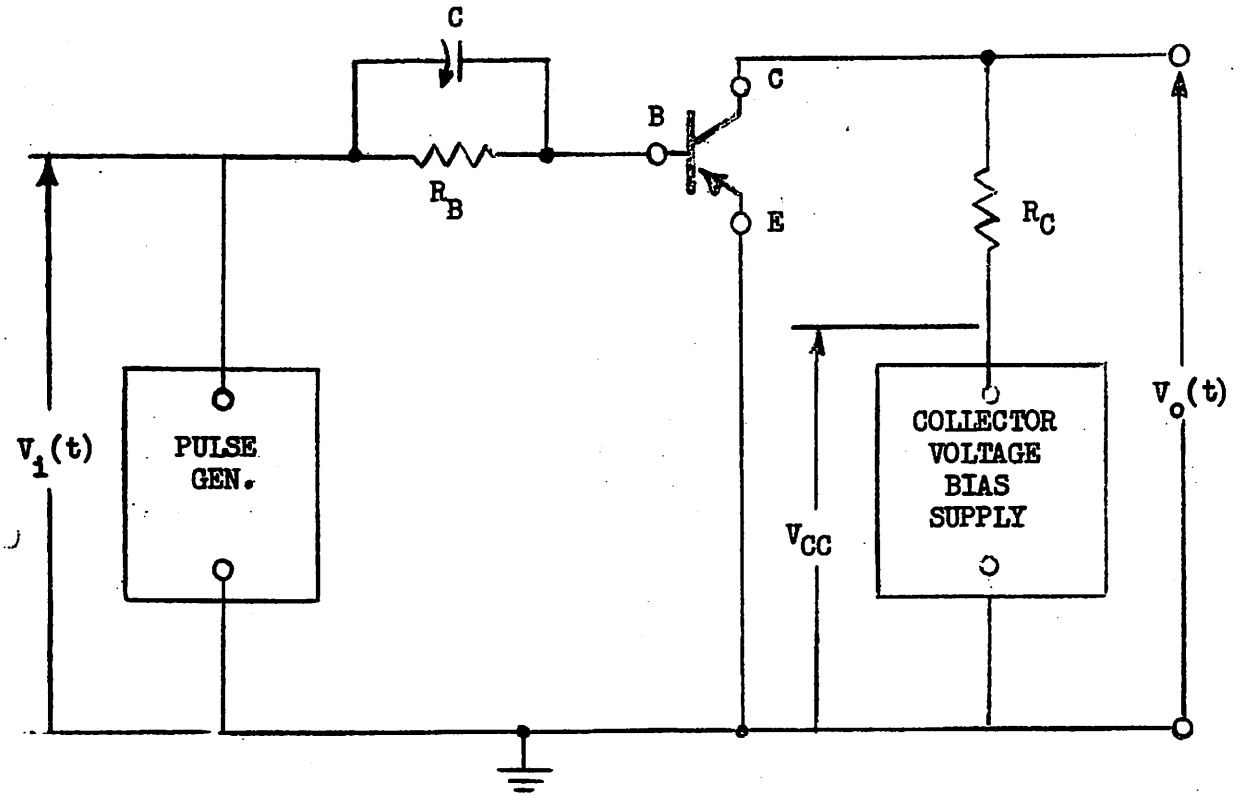
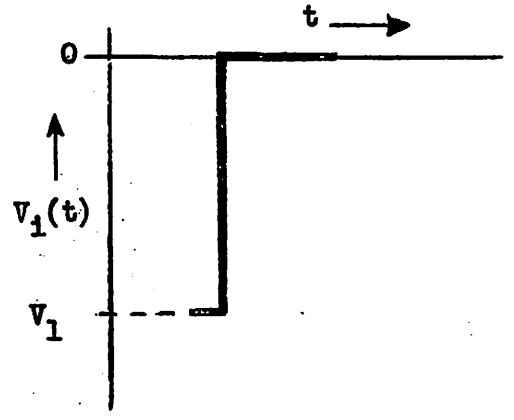


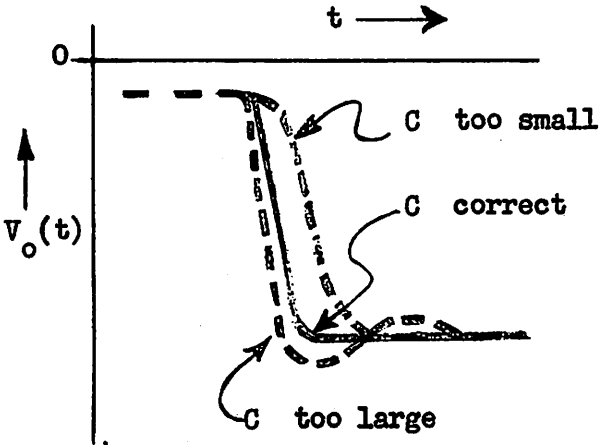

FIG. 9 TYPICAL COMPLEX PLANE REPRESENTATION OF SHORT-CIRCUIT INPUT IMPEDANCE $h_{ie}$




14 a MEASUREMENT CIRCUIT




14 b BASE DRIVE VOLTAGE




14 c COLLECTOR OUTPUT VOLTAGE

Fig. 14 MEASUREMENT CIRCUIT FOR SATURATION STORED CHARGE $Q_s$ AND TYPICAL WAVEFORMS - SECOND METHOD

MARCIANO