Chapter Meetings and Events

SCV-WIE & Nano - 6/1 | **Angstromology - A Tour of the Universe at the Nanoscale Level & Beyond** - what it is, isn't [more]

SCV-CAS - 6/6 | **Wireless Sensor Networks: Trends, Applications, and Development Platforms** - high-bandwidth input data with communication at low-bandwidth levels ... [more]

SCV-CNSV - 6/7 | **Tales of Consulting - On the Humorous Side** - 5 consultants talk about consulting experiences over a Chinese banquet dinner ... [more]

SCV-Comm - 6/8 | **A Software-Defined Radio Architecture for Future Cell Phones: Incentives and Challenges** - a programmable baseband processor for multi-standard hand sets ... [more]

SCV-CPMT - 6/8 | **Reliability Issues in Lead-Free Soldering** - the important issues for lead-free solder interconnection systems, including components, PCBs, and solder joints ... [more]

SCV-EDS - 6/14 | **Carbon Nanotubes and Nanofibers as On-chip Interconnects** - electrical and thermal characterization for next-generation back-end IC processing ... [more]

SCV-EMB - 6/15 | **A Pendant-Geometry CT Scanner for Breast Cancer Detection:** Design, Characterization and Assessment - [more]

SCV-IM - 6/15 | **Digital Verification and Design Validation Solutions** - breakthroughs in semiconductor test equipment ... [more]

SCV-SSC - 6/16 | **Design Challenges for a UWB Radio** - a design implementation based on the MBOA approach ... [more]

SCV-AP - 6/21 | **Ultrawideband Radar Methods and Techniques of Through-Barrier Imaging** - enabling real-time multi sensor imaging and monitoring objects through barriers ... [more]

SCV-EDS - 6/24 | **Mobility Enhancement for Advanced CMOS Devices** - half-day seminar with 6 speakers ... [more]

SCV-CE - 6/28 | **Embedding Small-Form-Factor Hard Disk Drives with CE-ATA** - new disk drive interface standard for consumer electronics applications ... [more]

SCV-EDS - 7/12 | **Dielectric Scaling Challenges And Approaches In Floating Gate Non-Volatile Memories** - new approaches to meet reliability and performance requirements ... [more]

SCV-CPMT - 7/21 | **Reliability of Lead-free Solder Joints: Intermetallic Reactions** - solder reaction, spalling, and Kirkendall void formation ... [more]

Upcoming Conferences in the Bay Area

June 21-23: **POFWorld '05**, Santa Clara Conv'n Ctr
Plastic Optical Fiber for Home and Auto –
sessions, tutorials, exposition [more]

July 11-12: **Int'l Electronics Manufacturing Technology Symposium**, SF Marriott Hotel
Focus on *Manufacturing at the Wafer Level* [more]

July 17-22: **Heat-Transfer Conf** collocated with **Integration and Packaging of MEMS, NEMS, and Electronic Systems (InterPACK'05)**
St. Francis Hotel, San Francisco
Sessions, tutorials, panels, exhibits [more]

Aug. 15-17: **16th Annual Magnetic Recording Conference**, Held at Stanford University
Early-bird discount through July 18th [more]

Professional Skills Courses from EMS, CPMT, ETA:

Breakthrough Project Management [more]
- June 7-8 at Hewlett Packard, Cupertino

Transitioning from Individual Contributor to Manager
- June 9 at Cypress Semiconductor, San Jose [more]

Managing Meetings [more]
- June 14 at Sybase, Dublin

Speed Reading [more]
- June 16 at Cypress Semiconductor, San Jose

Half-Day Tutorials (Monday July 11):
At IEMT Symposium in San Francisco
– Flip Chip Technology: A User's Guide (and others)
– Lead-Free Packaging and Assembly
– Advanced Packaging Technology Solutions [more]

Full-Day and 2-Hour Tutorials (Sunday July 17):
At InterPACK in San Francisco
– Thermomechanical Reliability of Microsystem Packaging
– High-Power Microelectronics Thermal Management
– Thermal and Mechanical Issues in Three-D Packaging
– Nano Scale Thermal Transport Modeling
– On-Chip Thermoelectric Cooling [more]

IEEE GRID

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IEEE **GRID** is the monthly newsmagazine of the San Francisco Bay Area Council of the Institute of Electrical and Electronics Engineers, Inc. As a medium for both news and opinion, the editorial objectives of IEEE **GRID** are to inform readers in a timely and objective manner of newsworthy IEEE activities taking place in and around the Bay Area; to publish the official calendar of events; to report on IEEE activities of a national and international scope; and to serve as a forum for comment on areas of concern to the engineering community by publishing contributed articles, invited editorials and letters to the editor.

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From the editor . . .

Summer is almost upon us – it's not long until school is out and many families will be heading out on vacation. Things slow down for the IEEE, too, and we schedule fewer Chapter meetings.

But for those who are around, there are several international conferences coming to the Bay Area – in IC packaging, magnetic recording, plastic optical fibers, and other topics. If you find one in your own specialty, be sure to register (some have free passes to their exhibits).

I've just returned from a two-week trip to Europe, where I attended servral different IEEE functions. First was a small workshop in Germany on signal propagation on IC and package interconnects. I addressed them on the new IEEE XPLORE interface (v. 2.0) and the coming 2.1 in July. This opens the search/ refine tool to any technologist worldwide, so that anyone can now "save" a complex search, and receive alert emails when new content is placed in XPLORE that matches the criteria. Neat stuff! And, did you know that all 1,200,000 XPLORE papers/standards are full-text searchable on Google now? Give it a try, the next time you have some key words or phrases you'd like to search. You'll find many "hits" in the IEEE's extensive database, and anyone can use it (and get the details about the paper, including the abstract). Of course, you'd need an account (your company or university one is fine) to download the actual PDF of the paper.

Then Gail and I drove across the Czech Republic to eastern Poland, then to Warsaw, where I met with staff at the Technical University there. Then on to Wroclaw to pay a visit to their university and discuss research projects. We cut back through the Czech Republic to Vienna, where I gave a talk on multimedia education and educational initiatives to a one-day Electronics Packaging Academic Conference. In both Germany and Vienna I had meetings of my Transactions editors and associate editors who were able to attend. Yes, it felt a lot like a vacation!

Paul Wesling **editor@e-grid.net**

NOTE: This PDF version of the IEEE GRID – the **GRID.pdf** – is a monthly publication and is issued a few days before the first of the month. It is not updated after that. Please refer to the Online edition and Interactive Calendar for the latest information: **www.e-GRID.net**

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TMRC'2005

Early-bird discount through July 18th

Join leading experts in the magnetic recording field

IEEE Magnetics Society

IEEE

16th Annual Magnetic Recording Conference

"Heads and Systems"

August 15-17, 2005

Held at Stanford University in Palo Alto
at the Hewlett Teaching Center Auditorium and Stone Pine Plaza

With utmost pleasure we announce this year's 16th annual TMRC. The main topics for the conference are Heads and Systems. This includes Read heads, Write heads, Perpendicular recording heads and systems, Recording systems, Advanced coding/detection, and Reliability/Mechanics.

With areal density growing at roughly 40% per year, key technologies to be presented at this conference include: new generation of advanced GMR, Tunnel MR, CPP GMR, Perpendicular recording heads and systems, novel coding/detection schemes, and head reliability and mechanics – all technologies that will be playing key roles in the near future.

The oral sessions will be held at the Hewlett Teaching Center Auditorium, and Stone Pine Plaza is to be used for Posters and Bierstube. I am sure you will find time to stroll through the pleasant Stanford campus.

Harry Gill, Hitachi Global Storage Technologies
Conference Chairman, TMRC 2005

Details:

- All Oral Sessions: Hewlett Teaching Center Auditorium (Continental Breakfast each day)
- Poster/Bierstube sessions: Stone Pine Plaza
- TMRC Banquet, 6:00-9:00 PM, Clark Center LinX Café
- Banquet Speaker: Dr. Mark Kryder, CTO, Seagate Technologies, "Magnetic Recording at the Crossroads"

PROGRAM

6 sessions with 36 papers, in the following areas:

- Read Heads - Write Heads
- Perpendicular Recording - Recording Systems
- Advanced Coding, Detection, and ECC
- Reliability and Mechanics

Invited speakers from the following companies and universities will present leading work in the magnetic recording area: Alps, Anelva, Fujitsu, Headway, Hitachi, Hutchinson, Matsushita, Maxtor, SAE, Seagate, Sony, TDK, Toshiba, UC Berkeley, CMU, UCSD/CMRR, Harvard

Plus Poster Sessions

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Center for Micromagnetics & Information Technologies (**MINT**) – University of Minnesota

Center for Materials for Information Technology (**MINT**)
University of Alabama

Center for Research on Information Storage Materials (**CRISM**) – Stanford University

Computer Mechanics Laboratory (**CML**)
University of California, Berkeley

Registration:

Lowest fees through July 18th (includes CD-ROM):

- IEEE Member: $260
- Non-Member: $315
- Full-time Student/Life member: $95
- Tuesday evening reception/banquet: $50/person

Parking for Monday – Wednesday:

Free on-campus parking is located at the Galvez Field lot at the corner of Galvez Street and Campus Drive East. The lot is within walking distance of the conference site. From Galvez Street walk to Serra Mall, turn right and walk past the Oval until you arrive to the Hewlett Teaching Center. Disabled parking passes are honored everywhere on campus. Please refer to the maps at the end of the TMRC booklet.

REGISTER TODAY!

Registration Discount through July 18

Download the Advance Program and Map:

Advance Program CLICK!

More information on the TMRC website:

tmrc.nanointernational.org

2005 Heat Transfer Conference and InterPACK '05 Co-located

July 17-22, 2005 **Westin St. Francis Hotel, San Francisco, CA, USA**

The **ASME Heat Transfer** and **InterPACK Conferences** serve as the premier venues for enabling hundreds of engineers to meet, exchange ideas and technical information, and learn of the latest advances in technology in heat transfer and electronic and photonic packaging technical disciplines and industries. In 2005, these two premier conferences are co-located in beautiful San Francisco, allowing engineers to expand their technical horizons through participation in both conferences under one roof. The InterPACK Conference has expanded to include emerging packaging technologies at the Micro and Nano scales.

The **InterPACK '05 Conference** promotes international cooperation, understanding, and development of efforts and disciplines in Microelectronics, Photonics, Microwave, MEMS and NEMS Systems Packaging and Integration. Emerging knowledge, research results, new developments, and novel thermal, mechanical, electrical, and materials packaging product concepts in Electronic Packaging Engineering will be presented in unique forums.

Focus of InterPACK '05:

- Telecommunications
- Packaging Technology
- Electrical Design, Simulation and Test
- Microelectronic Systems
- Photonics
- Airborne, Space and Defense Electronic Systems
- Microelectromechanical Systems (MEMS) and Nanoscale Phenomena in Electronics

25 Tracks of Session Papers:

- Tracks on Photonic and Electronic Systems, Micro/Nano Systems, Thermal Management, Reliability, Testing/Characterization of MEMS, Embedded Passives, Fluidics, Electro-Thermal Interactions, more
- Over 300 presented papers

Keynote Speakers:

Bill Holt, VP/GM, Technology & Manufacturing, Intel
Yoshio Nishi, Stanford Nanofabrication Facility
Katherine Frase, VP, Packaging and Test, IBM Corp
Raymond Li, VP, ATI Technologies
Brian Spalding, Managing Director, CHAM (UK)
Hans Stork, Sr VP, CTO, Silicon Dev't, Texas Instruments
Juergen Gromer, President, Tyco Electronics
Joy Crisp, Mars Rover Project Scientist, JPL

Full-Day and 2-Hour Tutorials (Sunday July 17):

(Need not register for HTC or InterPACK to attend)

Selected Topics: Thermomechanical Reliability of Micro-system Packaging – High-Power Microelectronics Thermal Management – Thermal and Mechanical Issues in Three-D Packaging – Nano Scale Thermal Transport Modeling – On-Chip Thermoelectric Cooling – Failure Analysis of PCB Packages – Numerical Methods in Micro- and Nano-Scale Thermal Transport – Design of Experiments for Thermal Engineering – Stress and Thermal Test Chips for Evaluation of Electronic Packaging Reliability – and more (see program)

The **ASME Heat Transfer Summer Conference** addresses issues facing the automotive, aerospace, chemical, nuclear, biotechnology, electronic and energy markets. The exchange of technical information will occur in areas ranging from energy to electronic systems as well as on research from computational and numerical methods to multi-phase phenomena.

Focus of the Heat Transfer Summer Conference:

- Heat transfer in energy systems
- Thermophysical properties
- Heat transfer in multiphase systems
- Heat transfer in manufacturing & materials processing
- Heat transfer in electronic equipment
- Low temperature heat transfer

19 Tracks of Session Papers:

- Tracks on Heat Transfer in Aerospace, Biotechnology, Manufacturing, Gas Turbines; Theory and Fundamental Research; Energy Transfer, Visualization, Modeling; and more
- Over 400 presented papers

Location:

- Held at the beautiful **Westin St. Francis Hotel**, on Union Square in San Francisco, July 17-22, 2005
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IEEE Professional Skills Courses

SCV Chapters, Engineering Management & Components, Packaging and Manufacturing Technology Societies

Breakthrough Project Management

Date/Time: Tues-Wed, June 7-8, 8:30AM-4:30PM
Instructor: Barry Flicker
Location: Hewlett-Packard, Cupertino
Fee: $575 for IEEE Members; $625 non-members

This 2-day course provides participants with a common methodology, terminology and tools that produce more efficient results and increased buy-in through improved visibility, reliability and consistency.

Key Topics: - Project Barriers & Breakthroughs - Team Development & Leadership - Define POS & Scope - Use the Trade-Off Flexibility Matrix - Make Fact-Based Decisions - Define Tasks - Create Work Breakdown Structure - Analyze Risks & Contingency Plans - Diagram Dependencies (CPM,PERT) - Manage the Project: Step-by-Step - Effective Meetings

"The methods and processes used for this class were not just tools and packages. They were a way to approach, manage and think, as well as communicate and deliver projects with less firefighting. I particularly liked the flexibility matrix, POS, risk analysis and critical path analysis."

Transitioning from Individual Contributor to Manager

Date/Time: Thurs, June 9, 8:30AM-4:30PM
Instructor: Roxanna Dunn
Location: Cypress Semiconductor, San Jose
Fee: $350 for IEEE Members; $425 non-members

"The class exceeded my expectations; it helped me understand my role and how my own skill set affects the way I lead. This course was very worthwhile."

Managing Meetings

Date/Time: Tuesday, June 14, 8:30AM-4:30PM
Instructor: Barry Flicker
Location: Sybase, Dublin
Fee: $350 for IEEE Members; $425 non-members

Improve your skills – register for one of these classes, or for others coming up in June and July. Bring a team!

For complete course information, schedule, and registration form, see our website:

www.effectivetraining.com

SCV Women in Engineering

WEDNESDAY JUNE 1

Angstromology - A Tour of the Universe at the Nanoscale Level & Beyond

Speaker: Robert Cormia, Foothill College
Time: Social and refreshments ($2 donation) at 6:15 PM, Presentation at 7:00 PM
Place: SRI International, 333 Ravenswood Ave, Menlo Park (Parking is free at the Ravenswood Ave entrance)
RSVP: by May 27 to k.chin@ieee.org with name and affiliation/company
Web: ewh.ieee.org/r6/scv/wie/

Robert Cormia is a full-time faculty member at Foothill College, where he teaches XML, bioinformatics, and informatics. Bob's background includes a long career in technology and business development while working at Surface Science Laboratories, specializing in materials analysis and new market development. After entering the Internet in 1994 as an educator and Web developer, Bob developed the eCommerce curriculum at Foothill College. Bob joined Foothill College full-time in fall 2001, where he developed courses in Internet projects, XML for biologists, bioinformatics, and the upcoming nanotechnology program. He completed the UCSC extension Certificate in Bioinformatics in 2003, and helped to develop Foothill College's certificate in bioinformatics. Bob now pursues research topics in Semantic Web Technologies, and strategies for solar energy development to reduce global warming.

Nanoscience and nanotechnology have been all the latest buzz, and we've all heard phrases like 'the next big thing is really small'. But quoting Meyya Meyyappan, 'small is necessary, but not sufficient' to define nanotechnology. If you talk to engineers, they'll claim nanotechnology is nothing more than materials science. Chemists will remind you that they've been 'positioning atoms' for hundreds of years. Biologists will quip that nature figured out nanotechnology billions of years ago. Physicists remark that nuclear fission is a controlled process at the pico scale (just to one up us). IBM used quantum technology to 'beam' a particle ten years ago, and just to insult us, our children play with perfect micelles in the form of soap bubbles, and we wash our dishes with economical Langmuir-Blodgett films every day. 'Angstromology' is a tour of the universe at the quantum scale, shedding some light on what is, isn't or what might be, nanotechnology. For the scientist and non-scientist alike, you'll understand that it is a small world after all.

SCV Circuits and Systems

MONDAY JUNE 6

Wireless Sensor Networks: Trends, Applications, and Development Platforms

Speaker: Dr. Hamid Aghajan, Stanford University
Time: Fast food/drinks at 6:30 PM, Presentation at 7:00 PM
Cost: none
Place: Cadence Design Systems, Building 5, 2655 Seely Avenue, San Jose
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/cas/

Hamid Aghajan is a consulting professor in the Department of Electrical Engineering at Stanford University, where he has helped establish and now supervises the Wireless Sensor Networks Laboratory with sponsorship of Professor Andrea Goldsmith. Hamid has ten years of industrial experience in algorithm design for application domains in wireless communications, optical telecommunications, biotechnology, and semiconductor manufacturing industries. He has consulted for several corporations, research labs, startups, and investors on the technical and commercial aspects of various wireless technologies as well as image processing and sensor networks applications. He was a co-founder and vice president of an optical telecom start-up company in 2001, and has also served on the Board of Advisors of high technology companies active in various wireless sensor networks applications.

Hamid is currently supporting research programs of a group of students at Stanford University on various aspects of wireless sensor networks with an emphasis on decentralized and collaborative processing methods for automated network node localization, applications of wireless image sensor networks, and RFID-enabled networks. In addition, he is supervising the development of several hardware and simulation platforms at the lab, including the design of two new wireless motes, which enable effective algorithm and application development in these fields. Hamid has published numerous journal and conference papers and holds 5 US patents. He has a Ph.D. degree in Electrical Engineering from Stanford University.

Energy and bandwidth constraints are major concerns in developing applications in wireless sensor networks. Hence, most traditional applications in this field are designed to deal with input data that is of low-bandwidth nature. In this talk we examine the possibilities in using high-bandwidth input data while the network communication is maintained at low-bandwidth levels. In particular, we will provide examples of how on-board computing and collaborative processing techniques can be employed to address problems in network self-organization and tracking applications using distributed image sensors. Several hardware and software platforms developed at the Wireless Sensor Networks Lab at Stanford University that enable efficient algorithm development and testing for these applications will also be introduced.

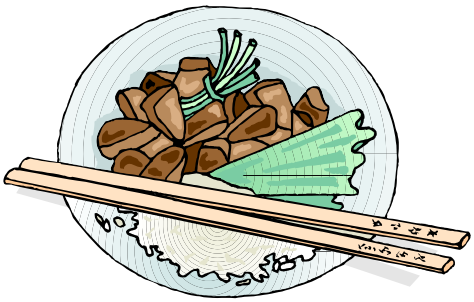
SCV Consultants' Network of Silicon Valley

TUESDAY JUNE 7

Tales of Consulting - On the Humorous Side (and Chinese Banquet Dinner)

Speakers: Five consultants discussing their experiences
Time: Chinese Banquet Dinner served at 6:30 PM
Cost to CNSV members: $16 if reserved by May 31 (your guest is also only $16); higher for non-CNSV attendees and after 5/31
Place: House of Sichuan, 20007 Stevens Creek Blvd, Cupertino
RSVP: Send your check, payable to IEEE-CNSV, to Dick Ahrons, 983 Garrity Way, Santa Clara
Web: www.ieee-sv-consult.org/

Our June mid-year event features a full Chinese Banquet Dinner including beef, duck, shrimp and fish dishes. The banquet price includes wine, both red and white. 5 consultants will talk about their consulting experiences, stories on the humorous side, and on the interesting side. The best, most entertaining story wins a bottle of wine.



WEDNESDAY JUNE 8

A Software-Defined Radio Architecture for Future Cell Phones: Incentives and Challenges

Speaker: Nikolaus Bruels, Infineon Corporate Research, Munich, Germany
Time: 6:00 PM (pizza & soda), 6:30 PM presentation
Place: National Semiconductor Credit Union, Bldg. 31, 955 Kifer Rd., Sunnyvale
RSVP: Please reserve by email to rsvp@comsocscv.org
Web: www.comsocscv.org

Nikolaus Bruels received the Master's degree in electrical engineering from the RWTH Aachen in 1989. From 1990 to 1999, he was with the Siemens Corporate Research, where he worked on data path architectures for neural networks and image processing systems. Since 1999, he has been a project manager with Infineon Corporate Research, department for Systems Technology, in Munich, Germany.

His main focus is on dedicated circuits and architectures for critical applications in the communication domain. Currently, he is an industrial visitor at the Berkeley Wireless Research Center where he works on a digital baseband processor for a Software Defined Radio.

Despite the efforts to converge the different wireless communication standards world-wide, the number of coexisting WiFi and mobile phone standards is still increasing. Future cell phones as universal communication devices will have to support even more standards and protocols than today. A software programmable baseband processor platform looks like a promising way to reduce NRE and development costs for multi-standard hand sets. However, the challenge of reconciling the flexibility and versatility goals with high processing power, long battery life, and small footprint is extremely demanding. Within Infineon's Corporate Research Department, a programmable baseband processor is being developed that is able to meet all of these requirements. In this talk, the Infineon approach will be discussed and the principles of the new architecture will be presented.

WEDNESDAY JUNE 8

Reliability Issues in Lead-Free Soldering

Speaker: Dr. Dongkai Shangguan, Director – Advanced Process Technology, Flextronics
Time: Seated dinner served at 6:30 PM ($25 if reserved before June 5; $30 after & at door); free presentation at 7:30 PM
Place: Ramada Inn, 1217 Wildwood Ave (Fwy 101 frontage road, between Lawrence Expy and Great America Pkwy), Sunnyvale
RSVP: Please reserve and pay in advance using our PayPal on-line system or email Janis Karklins, Karklins@ieee.org
Web: www.cpmt.org/scv/

Dr. Donkai Shangguan received his BS degree in Mechanical Engineering from Tsinghua University, China, Ph.D. degree in Materials from the University of Oxford, U.K., and MBA degree from San Jose State University. He conducted post-doctoral teaching and research at the University of Cambridge and then at the University of Alabama, and lectured at Wayne State University as Adjunct Faculty.

Dongkai worked for 10 years at Ford Motor Co. / Visteon Corporation as Senior Technical Specialist, Supervisor of Advanced Electronics Manufacturing, and Manager of Supplier Quality, before he joined Flextronics International in 2001 where he is currently Director for Advanced Process Technology with the Corporate Technology Group.

Dongkai has published one book and over 150 papers (including many journal publications and several book chapters), has given numerous technical presentations and keynotes, and his latest book on lead-free solder interconnect reliability will be published soon. He has 20 U.S. and international patents issued and a number of U.S. and international patents pending. He is currently a regular columnist for the "Global SMT & Packaging" magazine.

Dongkai is a senior member of IEEE and SME, and actively participates in professional organizations and consortia, and has chaired technical sessions and panels at numerous conferences. He has received a number of recognitions for his contributions to industry, including the "Total Excellence in Electronics Manufacturing Award" from the Society of Manufacturing Engineers (SME), and the "Soldertec Lead-Free Soldering Award".

While a significant volume of work has been conducted in the past ten years by the industry on manufacturing issues to enable the gradual conversion to lead-free solders, reliability studies of lead-free solder interconnects are still emerging. The issue of reliability is complicated by the wide variety of application environments and requirements, which give rise to different loading conditions. The physics of failure, which is directly related to reliability, is a critical topic still under intense investigation for lead-free solders. The topic is further complicated by the fact that the relative reliability comparison between eutectic Sn-Pb solder and the lead-free solder alloys varies with the loading conditions. These complications create great difficulties for the development of appropriate acceleration testing profiles and for reliability prediction. This presentation will review the important reliability issues for lead-free solder interconnection systems, including the components, the PCB, and the solder joints, under different loading conditions (thermomechanical, dynamic mechanical, electrochemical, etc).

See also the July 21st lunch meeting:

Reliability of Lead-free Solder Joints: Intermetallic Reactions

on Page 19

SCV Electron Devices

TUESDAY JUNE 14

Carbon Nanotubes and Nanofibers as On-chip Interconnects

Speaker: Dr. Cary Yang, Center for Nanostructures, Santa Clara University
Time: Pizza social at 6:00 PM; Presentation at 6:15 PM
Cost: free
Place: National Semiconductor Corp. Building 31 Large Auditorium, 955 Kifer Road, Sunnyvale
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/eds/announcements/ieee-scv-eds-20050601.html

Cary Yang received the B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Pennsylvania in 1970, 1971, and 1975 respectively. After working in various research positions at M.I.T., Stanford, and NASA, he founded Surface Analytic Research, Inc. in Mountain View and directed sponsored research in surface and nanostructure science. In 1983 he joined Santa Clara University and is currently Professor of Electrical Engineering, Associate Dean of Engineering and Director of the Center for Nanostructures. Dr. Yang has been a consultant to industry and government, and a visiting professor at Tokyo Institute of Technology, University of Tsukuba, National University of Singapore, the University of Pennsylvania, and the University of California, Berkeley. He is a Fellow of IEEE and served as Santa Clara Valley Chapter Chair, Regions/Chapters Chair, Vice President, and President of the IEEE Electron Devices Society. From 2002 to 2003, he served as an elected member of the IEEE Board of Directors, representing Division I.

He was an editor of the IEEE Transactions on Electron Devices, in the area of MOS devices. In 2004, he was named the recipient of the IEEE Educational Activities Board Meritorious Achievement Award in Continuing Education "for extensive and innovative contributions to the continuing education of working professionals in the field of micro/nanoelectronics".

As integrated circuit (IC) technology continues the trend towards sub-100 nanometer feature sizes, it is imperative to retain performance of back-end features such as on-chip interconnects while gaining the cost benefit of scaling. Some major barriers to achieving continuous scaling include high resistance of deep submicron copper lines and power dissipation in densely packed integrated circuits. This work presents fundamental electrical and thermal characterization of multiwall carbon nanotubes (MWNT) and carbon nanofibers (CNF) as a possible solution for next-generation back-end integrated circuit processing. Results of temperature-dependent electrical resistance measurements for MWNT and CNF arrays demonstrate distinct metallic behavior of these novel nanoscale devices. Microstructural characterization using high-resolution electron microscopy techniques are presented and its implications discussed. The use of CNF/copper composite material as a thermal interface for IC packaging is explored and fundamental thermal resistance measurement results show promise of such a composite material for thermal management applications.

WEDNESDAY JUNE 15

A Pendant-Geometry CT Scanner for Breast Cancer Detection: Design, Characterization and Initial Clinical Assessment

Speaker: John M. Boone, Ph.D., UC Davis
Time: optional dinner with the speaker in the Stanford Hospital cafeteria at 6:15 PM; Presentation at 7:30 PM
Place: presentation at Clark Center Auditorium (see website for maps)
Cost: none; campus parking free after 4 PM
RSVP: not required
Web: ieee.org/scv/embs/pages/upcoming.html

John M. Boone, Ph.D., received his undergraduate degree in medical physics from UC Berkeley, and graduate degrees in Radiological Sciences from UC Irvine. After faculty positions at the University of Missouri and Thomas Jefferson University (in Philadelphia), Dr. Boone joined the faculty at UC Davis in 1992. Dr. Boone is currently Professor and Vice Chairman of Radiology (for Research) and Professor of Biomedical Engineering at UC Davis. His is certified by the American Board of Radiology in Radiological Physics, is a fellow of the American Association of Physicists in Medicine and of the Society of Breast Imaging, and won an Outstanding Achievement Award in the Society for Photo-optical and Instrumentation Engineers. Dr. Boone's research interests include the development of a dedicated CT scanner for early breast cancer detection, Monte Carlo evaluation of image quality and radiation dose, and the development of mouse imaging technology combining x-ray and gamma-ray imaging.

The purpose of this investigation was to characterize the performance of a cone-beam CT scanner system custom designed for breast imaging. The breast CT scanner was designed and fabricated using an end-windowed industrial x-ray source and a 30 cm x 40 cm CSI thin-film transistor (TFT) flat-panel x-ray detector. The first prototype scanner (Albion) utilizes 360 acquisitions of 1,000 projection images (768 x 1024) over a 33 second acquisition. The 88 cm source to detector distance and the 48 cm source to isocenter distance allow breasts from 10 cm to 18 cm in diameter to be scanned, and the size-dependent technique factors were determined to allow scanning at the same average glandular dose levels as two-view mammography.

The spatial resolution was characterized using a thin tungsten wire, and the contrast resolution was evaluated using low contrast test objects. Scattered radiation levels were measured as a function of breast diameter, beam energy, and breast composition. The spatial resolution is characterized by a modulation transfer function with 10% modulation at approximately 1.2 inverse millimeters. Contrast resolution was found to be dependent upon breast diameter in the size of the test object in question. Scatter to primary ratio (SPR) at the center of the field of view were measured as 0.25, 0.50, and 0.92 for 50%/50% breast phantoms of 10 cm, 14 cm, and 18 cm in diameter, respectively.

While a number of artifacts proved difficult to remove, the image quality of the scanner based upon its technical performance and subjective analysis of cadaver breast images suggests that the Albion prototype is capable of good performance. A number of technical details in the design of the scanner will be discussed, including the x-ray tube assembly (bow-tie filter and x-ray shutter), rotating gantry system, etc. Validated Monte Carlo techniques were used to assess the average glandular dose of the breast, based upon inferred spectral measurements. Clinical evaluation of the breast CT scanner on volunteers and patients will begin shortly, with initial results should be available in March 2005.

SCV Instrumentation and Measurement

WEDNESDAY JUNE 15

Digital Verification and Design Validation Solutions

Speaker: Rohit Bhasin, Agilent Technologies
Time: Networking at 6:30 PM,
Presentation at 7:00 PM
Place: Cogswell College, Room 197,
1175 Bordeaux Drive, Sunnyvale
Cost: none
RSVP: by June 10 to David Rivkin,
david.rivkin@ieee.org
Web: www.ewh.ieee.org/r6/scv/ims/

Rohit Bhasin is a Senior Technical Sales Engineer for Agilent Technologies. He is responsible for all High-Speed Computer I/O and Memory Analysis solutions in Silicon Valley. He has held several hardware engineering positions at Intel and previously Acterna Corporation. Mr. Bhasin has a Bachelor of Science degree in Electrical Engineering with emphasis in Computer Architecture and Design from The Pennsylvania State University.

This presentation highlights technical advancements in high speed computer and storage interconnects as well the breakthroughs in semiconductor test equipment that are necessary to characterize and validate them.

SCV Solid State Circuits

THURSDAY JUNE 16

Design Challenges for a UWB Radio

Speaker: Sudhir Aggarwal, Philips Semiconductors
Time: Refreshments at 6:30 PM, presentation at 7:00 PM
Place: Cadence Building 5 which is located at: 2655 Seely Ave, San Jose
Cost: donation for food cost requested
RSVP: by June 10, either call 408-894-2646 (leave a message) or by email to ssc_scv_rsvp@yahoogroups.com
Web: www.ieee.org/scvssc/

Sudhir Aggarwal (S'84, M'89, SM'03) received his B.S. degree in Electronics & Communication Engineering with top rank. While working at the Indian Institute of Technology (IIT), Delhi, he obtained his Ph.D. degree in Electrical Engineering in 1988. From 1981 to 1989, he served at the Center for Applied Research in Electronics, IIT Delhi, working on various industrial and defense sponsored projects in the area of MOS analog ICs for signal processing applications. From 1991 to 1995, he was with ST Microelectronics (France and India) where he developed statistical circuit/device models and optimization tools for analog circuits in BiCMOS technology. Since 1995, he is working at Philips Semiconductors, San Jose, currently as a Senior Principal Engineer. At Philips, he has designed and developed transceiver circuits for CDMA and WLAN applications. His current interest includes RF ICs for wireless communication, in particular, for UWB and multi-mode systems. He is the author or coauthor of 15 papers.

Ultra wide band (UWB) is an emerging wireless technology for very high rate data communication. Currently, wireless networking solution are limited to data rate of several tens of Mb/s. UWB holds the promise of providing data rate of as high as 1Gb/s. With these data rates, one can envision a world without cables at the back of PCs or TVs. With the approval of FCC, several new frequency bands have been allocated for UWB applications. Out of these, the band around 3 to10GHz is being exploited mostly as current IC technologies are more suited for implementation in this frequency range. For implementation of a UWB radio, two major approaches are under deliberation in IEEE standardization committee. An industrial consortium known as Multi-Band OFDM Alliance (MBOA) has proposed one of these approaches. The MBOA approach reduces the radio complexity though it requires solution to many challenging implementation issues. In this lecture, after a brief introduction to UWB, a few target applications of UWB will be presented. A comparison of the relative strengths of the two approaches for implementing the UWB physical (PHY) layer will be mentioned. Design challenges for implementing a UWB radio will be discussed. A design implementation of a UWB radio receiver based on MBOA approach will be shown. Results obtained from a test-chip of the UWB receiver fabricated using a 70GHz ft SiGe technology will be presented.

SCV Antennas and Propagation

TUESDAY JUNE 21

Ultrawideband Radar Methods and Techniques of Through-Barrier Imaging

Speaker: Dr. John Chang, Lawrence Livermore National Laboratory
Time: Pizza and soda at 6:00 PM, presentation at 6:30 PM
Place: Cogswell College (Boardroom), 1175 Bordeaux Dr, Sunnyvale
Cost: none
RSVP: none required
Web: ewh.ieee.org/r6/scv/aps/

John Chang received his doctorate degree in Electrical Engineering from Northwestern University with emphasis in electromagnetic theory and techniques. He spent five years as a researcher at Dartmouth College in the Engineering Sciences program focusing on biomedical imaging approaches for hyperthermia treatment of cancer. He is currently in his seventh year at Lawrence Livermore National Laboratory, a US Department of Energy Laboratory managed by the University of California.

His responsibilities at the Laboratory to date include leading and participating in the development of advanced science and technologies for medicine, homeland security, combat casualty care, and first responders. He has participated in projects sponsored by a number of Laboratory Directorates including Engineering, Physics, Chemistry and Material Science, Safety and Environmental Protection, and Homeland Security Organization. He is a scientist within the Medical Physics and Biophysics Division in Physics Directorate. He is the program leader in the Micropower Impulse Radar Program. He is also a group leader for the Advanced Communications and Signal Processing Group in Engineering Directorate. Institutionally, he is a member of the Institutional Review Board for the Laboratory overseeing privacy policies and human subject studies occurring at the Laboratory. He has numerous publications and patents awarded and pending. External to the Laboratory, he is currently the Leader and Chairman on the Board of Directors for the Bay Area Mountain Rescue Unit and the San Mateo County Sheriff's Office of Emergency Services.

The LLNL impulse radar sensor program has been involved with the investigation into the science and technology necessary to enable real-time multi sensor imaging to detect and monitor objects through barriers. This presentation will describe some of the methodologies and recent findings. The typical existing approaches have severe limitations in capabilities. In general, there are extreme tradeoffs between range of detection (especially through obscurants at distance), specificity, data processing time, and portability. As an example, techniques that detect and screen for objects often do not have the capability to monitor in real time targets in motion. LLNL efforts take into account this multi-parametric space and developed potential solutions that can be readily adapted to specific application needs.

The use of field programmable gated arrays integrated with high resolution ultra wide band (UWB) electromagnetic sensors for imaging through barriers will be described. In addition the real-time imaging issues of detecting and tracking of small objects will be described.

Techniques of UWB beam forming and steering will be described. Among other attributes, the UWB system developed at LLNL has been shown to penetrate many materials (wood, some concretes, non-metallic building materials, some soils, etc.) with high range resolution. Further, monostatic and multi static systems will be presented. Results of system characterization based upon current prototype systems will be presented.

SCV Consumer Electronics

TUESDAY JUNE 28

Embedding Small-Form-Factor Hard Disk Drives with CE-ATA

Speakers: From Intel, Marvell
Time: 6:30 - 7:00 Pizza+Drinks, Networking; 7:00 PM Talks
Place: HP Cupertino, 19447 Pruneridge Avenue (Building 48), Cupertino
Cost: IEEE Member $5, non-IEEE member $10
RSVP: by June 10 to scv.ce@ieee.org
Web: www.ieee.org/scvce

A new disk drive interface standard will make integration of embedded hard disk drives into consumer electronics applications easier and less expensive. This event will explore the CE-ATA standard and it's role in consumer electronics with two speakers from Intel and Marvell.

SCV Electron Devices

TUESDAY JULY 12

Dielectric Scaling Challenges And Approaches in Floating Gate Non-Volatile Memories

Speaker: Dr. Stephen Keeney, Intel Corporation
Time: Pizza social at 6:00 PM; Presentation at 6:15 PM
Place: National Semiconductor Corp. Building 31 Large Auditorium, 955 Kifer Road, Sunnyvale
Cost: none
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/eds/announcements/ieee-scv-eds-20050701.html

Dielectric scaling in non-volatile memories (NVM) is approaching the point where new approaches will be required to meet the reliability and performance requirements of future products. For both the tunnel oxide and the inter poly dielectric (IPD), high k materials are being explored as possible candidates to replace the traditional SiO2 and ONO (Oxide/Nitride/Oxide) films used today. New storage node concepts are also becoming attractive as an alternative approach to address some of the dielectric scaling limitations. This presentation will review the current status and discuss the approaches being explored to provide dielectric scaling solutions for future non-volatile memory products.

Stephen Keeney is the Technology Integration Manager at Intel for the 90nm flash technology development program which supports a multi-billion dollar memory business. Stephen obtained his B.E. degree from University College Dublin, Ireland in 1988 and his Ph.D. degree in Microelectronics from the NMRC, Cork, Ireland in 1992. He joined Intel's R&D organization in Santa Clara, CA in 1993 and has worked extensively across many aspects of flash memory and logic development, including device physics innovations, yield analysis, memory test and design architecture, process integration and reliability. Stephen holds six patents and has written over 20 technical papers.

THURSDAY JULY 21

Reliability of Lead-free Solder Joints: Intermetallic Reactions

Speaker: Prof. King-Ning Tu, Materials Science & Engineering, UCLA
Time: 11:45 AM - 1:15 PM, buffet lunch
Cost: $15 (or $20 at the door)
Place: Ramada Inn, 1217 Wildwood Ave (Fwy 101 frontage road, between Lawrence Expy and Great America Pkwy), Sunnyvale
RSVP: Please reserve and pay in advance using our PayPal on-line system or email John Jackson, john.jackson@analog.com
Web: www.cpmt.org/scv/

Professor K.N. Tu holds a B.S., National Taiwan University; M.S., Brown University; Ph.D. in Applied Physics, Harvard University(1968). He worked at IBM's T.J. Watson Research Center for 25 years, managing their Thin Film Science department and as Senior Manager of the Materials Science Department. For the past 12 years he has been on the faculty of the Materials Science & Engineering department at UCLA, including 5 years as chair of the department.

Dr. Tu has been a Science Research Council Senior Research Fellow and The Royal Society Guest Research Fellow at Cavendish Laboratory, UK; Fellow of American Physical Society; Fellow of the Metallurgical Society; Overseas Fellow of Churchill College; Application to Practice Award of the Metallurgical Society; Alexander von Humboldt Research Award for senior US scientists; President of the Materials Research Society in 1981. His research interest is in kinetic processes in thin films, metal-Si interfaces, electromigration, Pb-free solder metallurgy, low dielectric constant thin films, and phase changes driven by high current density and high electric and magnetic fields. In addition to over 300 articles, he has published a book entitled Electronic Thin Film Science.

Reliability of solder joint technology has been a concern throughout the microelectronics industry -- for example, the low-cycle fatigue induced by thermal stress in flip chips. At present, the risk of fatigue problems has been greatly reduced by the invention of underfills applied between a flip chip and its substrate. On the other hand, due to the recent drive toward Pb-free solders, new reliability issues have emerged, such as Sn whisker growth on Cu leadframes finished with eutectic SnCu or matte Sn. Furthermore, because of the demand of added functions in advanced consumer electronic devices, electromigration is now a serious reliability issue because of the increase of current density in each solder joint.

This luncheon talk will focus on solder reaction, spalling of intermetallic compound in thin under-bump metallization (UBM) and Kirkendall void formation in thick under-bump metallizations.

Two additional topics will be covered in the CPMT Chapter's afternoon Seminar, from 1:30 – 4:30 PM:

- Electromigration Effects in Solder Joints
- Tin Whisker nucleation and growth

See the separate registration for the afternoon Seminar (which includes the lunch and lunch talk) at:

www.cpmt.org/scv/

CONFERENCE CALENDAR

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www.e-grid.net/docs/conf-flyer.pdf

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- July 17: Tutorials - July 18-22: Conferences & Exhibits

One registration gets you access to sessions and panels in either conference, with over 40 tracks to chose from. Held at the St. Francis Hotel on Union Square in San Francisco, it is easily accessed via BART and MUNI, with parking nearby.

See **Page 5** for more details

16th Annual Magnetic Recording Conference

"Heads and Systems"

August 15-17, 2005

Held at Stanford University in Palo Alto

See **Page 4** for more details
