Chapter Meetings and Events

SCV-CE - 6/28 | **Embedding Small-Form-Factor Hard Disk Drives with CE-ATA** - new disk drive interface standard for consumer electronics applications ... [more]

SCV-EMS - 6/29 | **Management Tools for Mining Knowledge Retention** - two talks: on managing knowledge web services, and on knowledge-mining tools ... [more]

SCV-IM - 7/6 **| FemLab for Instrumentation & Measurement** [more]

SCV-EDS - 7/12 | **Dielectric Scaling Challenges And Approaches In Floating Gate Non-Volatile Memories** - new approaches to meet reliability and performance requirements ... [more]

SCV-LEOS - 7/12 | **Making a Many-Colored Processing Engine: Signal Processing with Optical Filters** - ... [more]

OEB-Comm - 7/19 | **IEEE 802.16 Wireless Metropolitan Area Networks** - the interface standard for fixed wireless networks for broadband delivery, with the standards committee chair [more]

SCV-Nano - 7/19 | **Molecular-Scale Technologies for Electronics and Life Sciences** - new ways to apply the techniques of electronics technology to the field of life sciences ... [more]

SCV-CPMT - 7/21 | **Reliability of Lead-free Solder Joints: Intermetallic Reactions** - solder reaction, spalling, and Kirkendall void formation (plus a half-day class) ... [more]

Upcoming Conferences in the Bay Area

July 11-12: **Int'l Electronics Manufacturing Technology Symposium**, Moscone Convention Ctr
Focus on *Manufacturing at the Wafer Level* [more]

July 17-22: **Heat-Transfer Conf** co-located with **Integration and Packaging of MEMS, NEMS, and Electronic Systems (InterPACK'05)**
St. Francis Hotel, San Francisco
Sessions, tutorials, panels, exhibits [more]

Aug. 8-11: **Computational Systems Bioinformatics**,
Held at Stanford University; cutting edge research
Discount through August 3 [more]

Aug. 15-17: **16th Annual Magnetic Recording Conference**, Held at Stanford University
Early-bird discount through July 18th [more]

Professional Skills Courses from EMS, CPMT, ETA:

Collaborative Negotiating for Engineers [more]
- July 12 at EMC Software, Pleasanton

Finance for Non-Finance Professionals [more]
- July 21 at Exar Corp, Fremont

Getting Things Done Across Organizational Borders
- July 21 at BEA Systems, San Jose [more]

Managing Time & Multiple Priorities [more]
- July 22 at Sybase, Dublin

Half-Day Tutorials (Monday July 11):

At IEMT Symposium, Marriott Hotel, San Francisco
– Flip Chip Technology: A User's Guide (and others)
– Lead-Free Packaging and Assembly
– Intro to Nanotechnology: Tools, Processes, Applications
– Advanced Packaging Technology Solutions [more]

Full-Day and 2-Hour Tutorials (Sunday July 17):

At InterPACK in San Francisco
– Thermomechanical Reliability of Microsystem Packaging
– High-Power Microelectronics Thermal Management
– Thermal and Mechanical Issues in Three-D Packaging
– Nano Scale Thermal Transport Modeling
– On-Chip Thermoelectric Cooling [more]

Theory and labs in current technologies at San Jose State, *week of Aug 9 or Aug 16:*

- **DSP System Design and Implementations**
- **FPGA DSP System Design**
- **Wireless Transmitters**
- **Embedded Systems and Embedded FPGAs**
- **High-Speed Data Networks**

[more]

IEEE GRID

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IEEE **GRID** is the monthly newsmagazine of the San Francisco Bay Area Council of the Institute of Electrical and Electronics Engineers, Inc. As a medium for both news and opinion, the editorial objectives of IEEE **GRID** are to inform readers in a timely and objective manner of newsworthy IEEE activities taking place in and around the Bay Area; to publish the official calendar of events; to report on IEEE activities of a national and international scope; and to serve as a forum for comment on areas of concern to the engineering community by publishing contributed articles, invited editorials and letters to the editor.

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From the editor . . .

Summer is a great time for completing projects around the house, finding time for some vacation, and generally trying to get caught up. I'm finding, though, that it's hard to find time for everything that I'd wanted to do. Perhaps this is true for you, too.

One of the priorities for working engineers and engineering managers is to learn about new technologies that will be impacting their jobs over the next few years. We know that this can be critical to keeping our company/lab pushing ahead with new products and services – and also for keeping our own jobs at state-of-the-art levels. That's where IEEE comes in.

Several of the local Chapters organize classes for mastering new skills and understanding new technologies. Our local university – San Jose State University – has several concentrated 4-day lab-based classes next month in various new technologies (see page 7). And we are fortunate in our technology-heavy Bay Area, with many international conferences wishing to come here every few years. Most of them have a day of tutorials or professional-development courses, and any of our local engineers can attend the classes (usually without needing to register for the conference itself). Watch for these opportunities, and make a pledge to "pay yourself" by taking a course every year. It's your responsibility to maximize the "useful life" of your career, and spending a day or two in concentrated study of a new field or technique can pay dividends by preserving your own employability.

Another avenue that many engineers use to enhance their employability is to achieve recognition as a Professional Engineer. The SCV PACE group may be organizing courses for the Fundamentals of Engineering and the Professional Engineer tests (see page 11). Get in touch with them if this might help you.

Have a great summer!

Paul Wesling **editor@e-grid.net**

NOTE: This PDF version of the IEEE GRID – the **GRID.pdf** – is a monthly publication and is issued a few days before the first of the month. It is not updated after that. Please refer to the Online edition and Interactive Calendar for the latest information: **www.e-GRID.net**

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TMRC'2005

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Join leading experts in the magnetic recording field

IEEE Magnetics Society

IEEE

16th Annual Magnetic Recording Conference

"Heads and Systems"

August 15-17, 2005

Held at Stanford University in Palo Alto
at the Hewlett Teaching Center Auditorium and Stone Pine Plaza

With utmost pleasure we announce this year's 16th annual TMRC. The main topics for the conference are Heads and Systems. This includes Read heads, Write heads, Perpendicular recording heads and systems, Recording systems, Advanced coding/detection, and Reliability/Mechanics.

With areal density growing at roughly 40% per year, key technologies to be presented at this conference include: new generation of advanced GMR, Tunnel MR, CPP GMR, Perpendicular recording heads and systems, novel coding/detection schemes, and head reliability and mechanics – all technologies that will be playing key roles in the near future.

The oral sessions will be held at the Hewlett Teaching Center Auditorium, and Stone Pine Plaza is to be used for Posters and Bierstube. I am sure you will find time to stroll through the pleasant Stanford campus.

Harry Gill, Hitachi Global Storage Technologies
Conference Chairman, TMRC 2005

Details:

- All Oral Sessions: Hewlett Teaching Center Auditorium (Continental Breakfast each day)
- Poster/Bierstube sessions: Stone Pine Plaza
- TMRC Banquet, 6:00-9:00 PM, Clark Center LinX Café
- Banquet Speaker: Dr. Mark Kryder, CTO, Seagate Technologies, "Magnetic Recording at the Crossroads"

PROGRAM

6 sessions with 36 papers, in the following areas:

- Read Heads - Write Heads
- Perpendicular Recording - Recording Systems
- Advanced Coding, Detection, and ECC
- Reliability and Mechanics

Invited speakers from the following companies and universities will present leading work in the magnetic recording area: Alps, Anelva, Fujitsu, Headway, Hitachi, Hutchinson, Matsushita, Maxtor, SAE, Seagate, Sony, TDK, Toshiba, UC Berkeley, CMU, UCSD/CMRR, Harvard

Plus Poster Sessions

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Center for Magnetic Recording Research (**CMRR**)
University of California, San Diego

Institute for Information Storage Technology (**IIST**)
Santa Clara University

Center for Micromagnetics & Information Technologies (**MINT**) – University of Minnesota

Center for Materials for Information Technology (**MINT**)
University of Alabama

Center for Research on Information Storage Materials (**CRISM**) – Stanford University

Computer Mechanics Laboratory (**CML**)
University of California, Berkeley

Registration:

Lowest fees through July 18th (includes CD-ROM):

- IEEE Member: $260
- Non-Member: $315
- Full-time Student/Life member: $95
- Tuesday evening reception/banquet: $50/person

Parking for Monday – Wednesday:

Free on-campus parking is located at the Galvez Field lot at the corner of Galvez Street and Campus Drive East. The lot is within walking distance of the conference site. From Galvez Street walk to Serra Mall, turn right and walk past the Oval until you arrive to the Hewlett Teaching Center. Disabled parking passes are honored everywhere on campus. Please refer to the maps at the end of the TMRC booklet.

REGISTER TODAY!

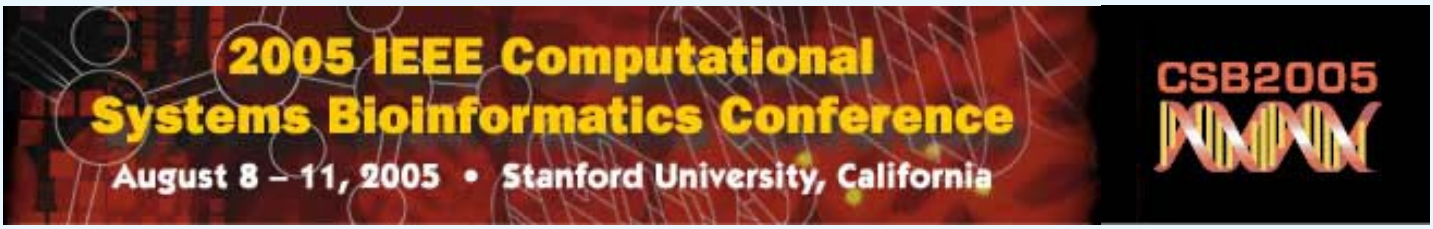
Registration Discount through July 18

Download the Advance Program and Map:

Advance Program CLICK!

More information on the TMRC website:

tmrc.nanointernational.org



CSB2005 brings you cutting-edge research on biological discovery and innovation through multidisciplinary presentations that can change the world of biology, medicine and drug discovery – and by changing this world, change the lives of the people waiting for cures. **CSB2005** provides a broad spectrum of peer-reviewed, bioinformatics-related topics covering the breadth and depth of this dynamically evolving field. Our topic submission procedures, keynote speakers, paper and poster presentations, tutorials and social events have all been designed to cater to bioinformatics' eclectic mix of disciplines. However, attendance is limited so please register early.

KEYNOTE SPEAKERS:

Russ Altman, MD, PhD
Professor of Genetics, Bioengineering, Medicine, Computer Science, Stanford University

Sydney Brenner, PhD
Distinguished Professor of Biological Studies, The Salk Institute, and 2002 Nobel Prize in Medicine and Physiology

Jacob T. Schwartz, PhD
Professor of Computer Science and Genetics, New York University Courant Institute

INVITED SPEAKERS:

Michael Ashburner, PhD, ScD
Prof of Biology, University of Cambridge; Professorial Fellow, Churchill College; Visiting Group Leader, European Bioinformatics Institute

Larry Goldstein, PhD
Professor of Cellular and Molecular Medicine, UCSD School of Medicine; Investigator, Howard Hughes Medical Institute

Ron Kikinis, MD
Director of the Surgical Planning Laboratory, Department of Radiology, Brigham and Women's Hospital and Harvard Medical School

Isaac Kohane, MD, PhD
Associate Professor of Pediatrics and Medicine, Harvard Medical School; Director, Children's Hospital Informatics Program

Srikanta Kumar, PhD
Program Manager, DARPA; Senior Technical Advisor, Information Technology Lab, National Institute of Standards and Technology (NIST)

Daniel Rokhsar, PhD
Professor of Molecular Cell Biology, Physics, UC Berkeley; Program Head, Computational Genomics, JGI

Arthur Toga, PhD
Professor of Neurology, UCLA School of Medicine; Director, Laboratory of Neuro Imaging; The Center for Computational Biology

Bioinformatics - scientific and engineering disciplines bringing new biological discoveries to fields as varied as human health, agriculture, the environment, energy and biotechnology. Find out more at **CSB2005**

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Who should attend:
Bioinformaticists, Biologists, Computer Scientists, IT Professionals, and Engineers who want to quickly learn about the evolving field of bioinformatics.

Location:
Held on the Stanford University campus, **CSB2005** is easily accessible to professionals living in the SF Bay Area and Silicon Valley.

See our website for driving and free parking directions.

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For more Conference details including session titles, technical presentations, and on-line registration, visit:

conferences.computer.org/bioinformatics

Early Registration Discount Thru August 3

Tutorials Offered on Monday, August 8
(as low as $125 – includes one AM and one PM)

MORNING TUTORIALS
Demonstration Projects in Clinical Informatics
Introduction to Factor Graphs and the Sum-Product Algorithm:
Genome Tiling Microarrays and Gene Interaction Networks
Novel Visualization and Analysis Methods in BioImaging
RNA-interference: The Short and Long of It
Computational Methods in MS-based Proteomics
AFTERNOON TUTORIALS
Introduction to the Semantic Web for Bioinformatics
Structure Based Methods for Identifying Protein Function
Pattern Discovery in Sequences and Structures
Understanding the Biological Data Deluge through Phylogenetics
Statistical Approaches to Analyzing Biological Networks

Listing of tutorial descriptions and instructors at

conferences.computer.org/bioinformatics

Friday Workshops – See next page ➔

The Life Sciences Society will be sponsoring **four parallel workshops** to be held on Friday, August 12 at Stanford University, as satellite events of the **CSB2005** Conference.

BioImage Data Mining and Informatics
Chaired by Hanchuan Peng, Lawrence Berkeley National Lab, UC Berkeley
Sponsored by the Life Sciences Society

Controlling Complexity
Chaired by Mike Hinchey, NASA Goddard Space Flight Center
Sponsored by the Life Sciences Society in conjunction with the IEEE Technical Committee on Complexity in Computing

Exploring 3D Molecular Structures Using NCBI Tools
Chaired by Eric Sayers, NCBI
Presented by the National Center for Biotechnology Information (NCBI) and sponsored by the Life Sciences Society

BioSPICE and Use Cases (half-day)
Presented by Quantum Intelligence, Inc.
Sponsored by the Life Sciences Society and BioSPICE Community

Lunch is included

WORKSHOP REGISTRATION includes snacks and lunch on Friday, August 12.

WORKSHOP FEES (US dollars)	ADVANCE	ON-SITE
LSS Member	$100.00	$130.00
Non-member*	$160.00	$190.00

* Fee Includes membership In LSS for One Year

For additional information and to register for these Friday Workshops, please see:

www.lifesciencessociety.org

The goal of the **Life Sciences Society** (LSS) is to foster collaboration among the various research disciplines that have a strong emphasis on the study of LIFE: biology, computer science, physics, engineering: electrical, chemical and mechanical, medicine, mathematics, pharmacology, microarray chip designs, drug discovery, genetic therapies, food production, stem cell analysis, high performance computing, and more.

Show your support for creating the **Life Sciences Society** within IEEE. Sign our petition now:

www.lifesciencessociety.org

IEEE Professional Skills Courses

SCV Chapters, Engineering Management & Components, Packaging and Manufacturing Technology Societies

Finance for Non-Finance Professionals

Date/Time: Thurs, July 21, 8:30AM-12:30PM
Instructor: Roxanna Dunn
Location: Exar Corporation, Fremont
Fee: $275 for IEEE Members; $300 non-members

This half-day course provides non-finance professionals with an understanding of basic financial terms and concepts to enable them to connect their activities and work products with the company's bottom line. The class focuses in three basic areas

- The Income Statement and Balance Sheet
- Investment financials.
- Trends in a company's quarterly report.

Learn how to:
Interpret an Income Statement and Balance Sheet.
Identify the primary areas where your organization contributes to the company's bottom line.
Understand basic financial terms: Revenue - Cost of goods sold - Profit/loss - Bottom line - Inventory turns - Margin - Assets - Liabilities - Equity - Earnings per share - Capital investments versus expensed items - Depreciation - Return on investment, return on assets, return on equity - Growth
Use time value of money to compare investments
Interpret trend analysis in sales, expenses

Collaborative Negotiating

- Date/Time: Tues July 12, 8:30 AM - 4:30 PM
- Instructor: Barry Flicker
- Location: EMC Software, Pleasanton
- Fee: $350 for IEEE Members; $425 non-members

"I enjoyed the different methods and gained excellent skills for negotiating."

Managing Time & Multiple Priorities

- Date/Time: Friday, July 22, 8:30AM-12:30PM
- Instructor: Peter Turla
- Location: Sybase, Inc, Dublin
- Fee: $275 for IEEE Members; $300 non-members

"I enjoyed this class very much. I thought it was very informative and useful. It really made me more aware of how I can organize my time."

Improve your skills – register for one of these classes, or for others coming up in July. Bring a team!

For complete course information, schedule, and registration form, see our website:

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2 Choices the week of August 9-12:

Digital Signal Processing -- 4-day class with labs:

DSP System Design and Implementation

Overview: Today's technology provides DSP processors that can be easily used to design very sophisticated products for instrumentation, control systems, communications, and wireless systems. This course presents DSP system design and implementation using programmable signal processors. Hands-on laboratory exercises are used to present the design and implementation aspects, using hardware and software tools for system implementation. The 5 laboratory sessions follow the lectures, where participants will apply system design concepts by designing, implementing, debugging and evaluating DSP schemes.

Wireless -- 4-day class with labs:

Wireless Transmitters

Overview: There are a number of transmitter architectures developed to satisfy the linearity requirements of modulation techniques employed in short- and long-range communication applications. This exceptional course introduces the modulation techniques and wireless standards, and compares the RF properties and performance of the CMOS, SiGe and GaAs technologies. The laboratory sessions of the course involve using the MATLAB/VerilogA simulators for behavioral characterization of transmitters by generating baseband signals of constant envelope, varying envelope communication systems, and applying transmitter nonlinearities. Throughout the lab projects, one will be able to understand and characterize the mask, the bandwidth and the peak to average ratio of communication signals and measure the distortion and spectral regrowth caused by transmitters.

Come to San Jose State!

Easy access: class starts before most students arrive on campus, so parking in the 7th Street garage is a snap!
Cost: $995 per course (includes student notebook, lunches and refreshments, CDs with class notes and problem solutions for certain classes)

Review the full course Flyer:

www.e-grid.net/docs/sjsu0508.pdf

for course overviews, prerequisites, instructor profiles, registration, map

3 Choices the week of August 16-19:

Digital System Design -- 4-day class with labs:

Embedded Systems and Embedded FPGAs

Overview: This short course is designed to introduce the fundamentals of embedded systems, and embedded FPGA design methodology. The objectives are to give an overview of the technology, the fundamentals and advanced issues, and hand-on experience with embedded FPGAs. The Laboratory modules provide hands-on experience with configuring the processor core, developing IP with VHDL, writing driver, system integration and test routines. Students will be exposed to a learning experience balanced between fundamental and advanced issues, theoretical concepts to hand-on experiments that will help them progress from novice to expert within a short time.

Digital System Design -- 4-day class with labs:

FPGA DSP System Design

Overview: This course provides an in-depth and state-of-the-art coverage of the design and FPGA-based implementation of high-performance DSP systems. After presenting FPGA architectures and design tools by Xilinx and Altera, several hands-on design labs on DSP, digital communications and video/imaging will be covered, including FFT, FIR filters, error detection/correction circuits, modem, color space converter, and DWT (Discrete Wavelet Transform). Contents: Basic DSP/Communication theory, FPGA architecture/design tools, HDL (VHDL and Verilog), DSP-specific arithmetic circuits, hardware design of digital filters, FFT circuits, error detection & correction circuits, encryption/decryption circuits, and video/imaging circuits.

Networking Engineering -- 4-day class with labs:

High-Speed Data Networks

Overview: This course covers architectures, delay modeling, and the latest innovations in broadband computer-communication networks – detailed studies on design and analysis of high-speed switches and routers, design of input/output interfaces for fast routers with quality-of-service provisions, design of multicast switches and networks, delay modeling, bandwidth allocations and congestion control methods for broadband networks, voice compression for higher data rates, voice over IP, and the latest techniques in wireless communication systems. The course starts with a brief overview of high-speed networks and architectures and continues with the design of switching systems and routers and router interfaces with quality-of-service provisioning. The course then addresses delay analysis and congestion control techniques, and then targets some of the most demanded topics such as the design of multicast high-speed networks, voice over IP, and wireless high-speed networks. The labs are hands-on experiments in Computer networking.

2005 Heat Transfer Conference and InterPACK '05 Co-located

July 17-22, 2005 **Westin St. Francis Hotel, San Francisco, CA, USA**

The **ASME Heat Transfer** and **InterPACK Conferences** serve as the premier venues for enabling hundreds of engineers to meet, exchange ideas and technical information, and learn of the latest advances in technology in heat transfer and electronic and photonic packaging technical disciplines and industries. In 2005, these two premier conferences are co-located in beautiful San Francisco, allowing engineers to expand their technical horizons through participation in both conferences under one roof. The InterPACK Conference has expanded to include emerging packaging technologies at the Micro and Nano scales.

The **InterPACK '05 Conference** promotes international cooperation, understanding, and development of efforts and disciplines in Microelectronics, Photonics, Microwave, MEMS and NEMS Systems Packaging and Integration. Emerging knowledge, research results, new developments, and novel thermal, mechanical, electrical, and materials packaging product concepts in Electronic Packaging Engineering will be presented in unique forums.

Focus of InterPACK '05:

- Telecommunications
- Packaging Technology
- Electrical Design, Simulation and Test
- Microelectronic Systems
- Photonics
- Airborne, Space and Defense Electronic Systems
- Microelectromechanical Systems (MEMS) and Nanoscale Phenomena in Electronics

25 Tracks of Session Papers:

- Tracks on Photonic and Electronic Systems, Micro/ Nano Systems, Thermal Management, Reliability, Testing/Characterization of MEMS, Embedded Passives, Fluidics, Electro-Thermal Interactions, more
- Over 300 presented papers

Keynote Speakers:

Bill Holt, VP/GM, Technology & Manufacturing, Intel
Yoshio Nishi, Stanford Nanofabrication Facility
Katherine Frase, VP, Packaging and Test, IBM Corp
Raymond Li, VP, ATI Technologies
Brian Spalding, Managing Director, CHAM (UK)
Hans Stork, Sr VP, CTO, Silicon Dev't, Texas Instruments
Juergen Gromer, President, Tyco Electronics
Joy Crisp, Mars Rover Project Scientist, JPL

Full-Day and 2-Hour Tutorials (Sunday July 17):

(Need not register for HTC or InterPACK to attend)

Selected Topics: Thermomechanical Reliability of Micro-system Packaging – High-Power Microelectronics Thermal Management – Thermal and Mechanical Issues in Three-D Packaging – Nano Scale Thermal Transport Modeling – On-Chip Thermoelectric Cooling – Failure Analysis of PCB Packages – Numerical Methods in Micro- and Nano-Scale Thermal Transport – Design of Experiments for Thermal Engineering – Stress and Thermal Test Chips for Evaluation of Electronic Packaging Reliability – and more (see program)

The **ASME Heat Transfer Summer Conference** addresses issues facing the automotive, aerospace, chemical, nuclear, biotechnology, electronic and energy markets. The exchange of technical information will occur in areas ranging from energy to electronic systems as well as on research from computational and numerical methods to multi-phase phenomena.

Focus of the Heat Transfer Summer Conference:

- Heat transfer in energy systems
- Thermophysical properties
- Heat transfer in multiphase systems
- Heat transfer in manufacturing & materials processing
- Heat transfer in electronic equipment
- Low temperature heat transfer

19 Tracks of Session Papers:

- Tracks on Heat Transfer in Aerospace, Biotechnology, Manufacturing, Gas Turbines; Theory and Fundamental Research; Energy Transfer, Visualization, Modeling; and more
- Over 400 presented papers

Location:

- Held at the beautiful **Westin St. Francis Hotel**, on Union Square in San Francisco, July 17-22, 2005
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School Mission: The School of Engineering at Santa Clara University has as its mission to be known and treasured, in Silicon Valley and beyond, for the impact of our graduates and faculty on improving the human condition through engineering education, practice, and scholarship. Like the University, the School is focused on student learning, educating the whole person, and demonstrating the interconnectedness of disciplines.

Open Position: The Department invites applications for a one year faculty position in the area of **communications**; an emphasis on wireless is desirable but not necessary.

Duties: The person selected for this position would teach the equivalent of **two to three courses per academic quarter**, including both undergraduate and graduate courses in communications and other fundamental electrical engineering topics. Other duties include advising students and supervising senior design projects. Some teaching experience is desirable. For new PhD applicants, teaching assistantship experience is valuable.

Qualifications: Candidates should have a successful track record in teaching electrical engineering at the undergraduate and graduate levels or as a teaching assistant. Candidates should have earned a master's degree or doctorate in electrical engineering.

Application Procedure: Please send a letter of application, curriculum vitae, summary of teaching evaluations (if available), and the names, addresses, and telephone numbers of three professional references to:

Benjamin Greer, Search Coordinator
Department of Electrical Engineering
School of Engineering
Santa Clara University
500 El Camino Real
Santa Clara, CA 95053-0560

Inquiries: For additional information please contact Benjamin Greer, the search coordinator:

Email: **bgreer@scu.edu** Phone: 408-554-5313 Fax: 408-554-5474

For additional information about the department please refer to our web site:

www.scu.edu/engineering/ee

The Department will begin considering applications immediately and continue until the position is filled. Santa Clara University is an equal opportunity affirmative action employer, and welcomes applications from women, persons of color, and members of other historically under-represented US ethnic groups.

Cogswell Polytechnical College
Sunnyvale, CA

The Roy B. Anderson Endowed Chair in Electrical Engineering

Cogswell Polytechnical College invites applications for an endowed full-time faculty position, the Roy B. Anderson Chair in Electrical Engineering. A candidate for this position will lead the development of the electrical engineering program to implement the fusion of art and engineering. He/She will have the desire and knowledge necessary to create devices and systems to support innovation in the Digital Arts.

The ideal candidate will possess a doctorate (Ph.D., Sc.D., or equivalent) in Electrical Engineering by the beginning of the appointment period and have experience in teaching at the undergraduate level and in relevant industry.

Interested individuals should submit a current curriculum vitae, a description of significant background, and three letters of recommendation of professional or academic nature.

Founded in 1888 in San Francisco as an innovative vocational high school, Cogswell Polytechnical College evolved along with society, becoming a two-year college in 1930 and a four year baccalaureate institution in 1971. The College moved to its present location in Sunnyvale, CA, the heart of Silicon Valley, in 1994. Small, but highly focused, Cogswell offers programs leading to B.A. and B.S. degrees in Digital Art and Animation, Digital Motion Picture, Digital Arts Engineering, Digital Audio Technology, Electrical Engineering and Software Engineering.

Deadline open until filled. All applications should be directed to:

Roy B. Anderson Chair in Electrical Engineering,

EEVacancy@cogswell.edu or

Cogswell Polytechnical College
1175 Bordeaux Drive
Sunnyvale, California 94089

SCV Consumer Electronics

TUESDAY JUNE 28

Embedding Small-Form-Factor Hard Disk Drives with CE-ATA

Speakers: From STMicroelectronics, Hitachi, Marvell
Time: 6:30 - 7:00 Pizza+Drinks, Networking; 7:00 PM Talks
Place: HP Cupertino, 19447 Pruneridge Avenue (Building 48), Cupertino
Cost: IEEE Member $5, non-IEEE member $10
RSVP: by June 26 to scv.ce@ieee.org
Web: www.ieee.org/scvce

Gianfranco Scherini is with the Data Storage Division of STMicroelectronics. He has 15 years of experience with silicon manufacturers with STMicroelectronics, and as a member of the CE-ATA marketing team. Current Position: Part of the Data Storage Division, as SoC Marketing Manager and Responsible for new applications. Before joining the Data Storage Division in 2002, Gianfranco had managed the North American Business Development Unit of the Telecom Division to develop several reference designs for ADSL consumer application. In the past Gianfranco spent 6 years working in Europe as Product Marketing for the Telecom Division and as Product Marketing for the Microprocessor Division.

Justin Heindel joined Marvell in 1999 as a Product Marketing Manager for the Storage Business Group and is responsible for the Company's hard disk drive interface and DVD system-on-chip products. At Marvell, Mr. Heindel has spearheaded the Company's leadership role in industry adoption of Serial ATA technology and currently manages Marvell's efforts in storagetechnology for consumer electronics. He is also actively involved in industry standards and has played a key part in the recent formation of the CE-ATA initiative, an industry workgroup focused on optimized hard disk drive technology for handheld consumer electronics applications. Mr. Heindel holds a Bachelor of Science degree from Cornell University.

John Osterhout is Director of Worldwide Retail Business for Hitachi Global Storage Technologies (former IBM). In this role, John manages the global disk drive retail business in partnership with Sales, Supply Chain Management, Finance, Marketing, Strategy and the Business Units. Prior to this assignment, John was Director of Corporate Marketing and Director of Business Management for Hitachi GST's Emerging Business Unit.

A new disk drive interface standard will make integration of embedded hard disk drives into consumer electronics applications easier and less expensive. This event will explore the CE-ATA standard and it's role in consumer electronics with two speakers from Intel and Marvell.

First talk:
CE-ATA Interface for Small Form Factor Drives

Gianfranco Scherini will be talking about the advantage of the CE-ATA interface for Small Form Factor drives. In particular he will tackle cost, performance, power dissipation and flexibility in handheld applications - MP3, JPEG and video application. He is also planning an update on the status of the CE-ATA specifications, with a sense of the industry trends and his views.

Second talk:
Consumer Electronics Disk Drive Innovation

Disk drive manufacturers must innovate to meet new consumer electronics demands, such as: security, cost, reliability, performance, interface, power, acoustics, shock, capacity and portability. Mr. Osterhout will focus his discussion on HDD interfaces, storage capacity and reliability. He will also address the latest advances in small-form-factor disk drives in furthering the exploding CE growth.

IEEE Magnetics Society

16th Annual Magnetic Recording Conference: "Heads and Systems"

- August 15-17
- Held at Stanford University in Palo Alto
- Early-bird discount through July 18th
- Join leading experts in the magnetic recording field

Main topics: Read heads, Write heads, Perpendicular recording heads and systems, Recording systems, Advanced coding/ detection and Reliability/Mechanics.

The oral sessions will be held at the Hewlett Teaching Center Auditorium, and Stone Pine Plaza will be used for Posters and Bierstube. On-campus parking at no cost.

More information: **Page 4**

See the website:

tmrc.nanointernational.org

SCV Engineering Management

WEDNESDAY JUNE 29

Management Tools for Mining Knowledge - of Globalization and for Retention (two talks)

Forum: **Impacts of Global Economy on Technology Business and Tools to Aid Technical Managers**
Speaker: Eric T-S. Pan, founder, Meridian Deployment Corporation

Post-dinner: **Managing Web services - For Organizational Tacit Knowledge Retention, Laboratory Notebook, and Patent Journaling**
Speaker: Dr. David A. Rivkin, Founder and President, Global Consulting & Patents Intl.

Time: Forum at 6:00pm, Dinner at 7:00pm, after dinner presentation at 7:45pm
Place: Country Inn & Suites (former Prime Hotel and Wyndham), 1300 Chesapeake Terrace, Sunnyvale (near Lawrence Expy/Caribbean Dr at Hwy 237)
Cost: by Friday June 24th: $25 (IEEE member), $30 (non member), $5 surcharge for reservations thereafter. (Cash or check at the door)
RSVP: by June 24 through Website
Web: www.ieee-scv-ems.org

Eric T-S. Pan is the founder of Meridian Deployment Corporation (MDC), which provides consulting, publishing, and training services specifically to the scientific and engineering communities. As an engineer and a technical management practitioner with experience leading high-tech organizations over all phases of the business life cycle, Mr. Pan understands the specific business and career challenges technical professionals face. Concerned with various impacts of the new economy on engineers and scientists, Mr. Pan has found a serious lack of insight and information from the perspectives of these technical professionals. It is Mr. Pan's vision and aspiration for MDC to offer an online community (http://www.mdc-learning.com) supported by professionals for professionals, a topical series of books, and other information resources. (Continued ➔)

The Santa Clara Valley Engineering Management Society presents a before-dinner forum on aligning with accelerating globalization. Following networking and a sit-down dinner, the after-dinner topic will be on improving business communications through web-based data repositories.

Impacts of Global Economy to Technology Business and Tools to Aid Technical Managers

The acceleration of globalization has produced unprecedented opportunities, threats, and uncertainties for technical professionals and for business in general. It can be very disconcerting when knowledge, productivity, and money are no longer sure competitive advantages. Don't be discouraged. It just takes a while to find value first and realign oneself and/or one's business into a new value profit chain! Based on his newly released book, Perpetual Business Machines: Principles of Success for Technical Professionals, Eric T-S. Pan will present management tools that will help technical managers discover pointers that are applicable to current situations.

Managing Web services - For Organizational Tacit Knowledge Retention, Laboratory Notebook, and Patent Journaling

Web Service Technologies are advancing not only casual, personal communications but also offering opportunities for businesses to communicate better by providing centralized data repositories which can be used as a multimedia electronic notebook. Such multimedia electronic notebooks offer firms a way of keeping all information, thoughts, experiments, data and even video of the events recorded. These notebooks can be implemented with security, authenticity and other features necessary from an intellectual property perspective as well. They can be integrated with other Web or Desktop-based Product Development Lifecycle automation tools and Integrated Enterprise Management systems. This talk will provide an overview to the various web based technologies currently used, and touch on how two firms implement such note-booking capabilities.

Prior to founding MDC, Mr. Pan was a director of operations at Skyworks Solutions, Inc. He also held senior operations and product management positions

at Network Device, Inc., Spectrian Corporation, and Samsung Semiconductor, Inc.

Mr. Pan began his career in research and development at IBM, Caltech, and Hughes Electronics. In his early career, Mr. Pan authored over twenty technical papers and held several U.S. patents. Mr. Pan received a master's degree in electrical engineering and computer science from MIT and a bachelor's degree in applied physics from Caltech.

Dr. David A. Rivkin, Founder and President of Global Consulting & Patents Intl., has over 20 years experience in management, engineering and patent development in high-technology companies. He has extensive experience in advising companies, venture capital funds, mutual funds and law firms in technology related business, engineering and patent prosecution. He founded SciEssence, LLC in 1998 where he served as its President and CTO. Dr. Rivkin has extensive experience in engineering management, intellectual property, regulatory requirements and technology related matters. He specializes in instrumentation and measurement issues for such fields as Nanotechnology, Biotechnology, Materials Sciences, Semiconductor Test and Manufacturing and Optics.

Dr. Rivkin has been a frequent guest speaker on engineering management and high-technology issues, and is a member of IEEE, ACS, APS, SPIE, ACM, ACT and is currently the Vice-Chairman of the IEEE Silicon Valley Chapter of the Instrumentation and Measurement Society, Vice-Chairman of the Association for Chemical Topology, and Chairman of the Science and Technology Institutes Emerging Technologies Group. He is a holder of several patents and holds certifications in embedded systems and program management. He has received awards for innovation and program management from the Science and Technology Institute. Dr. Rivkin holds a PhD in Engineering Management from Farington University School of Business in the UK. He has done undergraduate work in chemistry and nuclear engineering and graduate work in applied mathematics, biophysics, and electrical engineering/computer science. Dr. Rivkin is a Registered Patent Agent in South Africa and expects to be so in the USA shortly.

SCV Instrumentation and Measurement

WEDNESDAY JULY 6

Beyond Standard Finite Elements: Techniques to make FEA Programs Do What You Never Thought They Could

Speaker: Dr. John Dunec, COMSOL, Inc
Time: Social at 6:30 PM; Presentation at 7:00 PM
Place: Cogswell College, Room 197, 1175 Bordeaux Drive, Sunnyvale
Cost: none
RSVP: by July 3 to David Rivkin, david.rivkin@ieee.org
Web: www.ewh.ieee.org/r6/scv/ims

John Dunec has over 25 years of experience in technology development and analysis. After receiving his Ph.D. from Stanford, Dr Dunec spent 11 years as a product engineer and manager at IBM. He was on the original team that designed what is now Pro/Mechanica, taught numerical methods at UC Santa Cruz, and spent 3 years at Prof Hughes' multiphysics FEA startup, Centric Engineering. Dr. Dunec formed and, for the past 12 years, ran Venture Product, a product development and analysis consulting firm with clients ranging from IDEO, to Xerox PARC, to numerous start-ups in MEMs, microfluidics, biotechnology and advanced optical technology. John has considerable experience with finite element codes and for the past 3 years has taught FEMLAB classes throughout the country. Last April, Dr. Dunec opened COMSOL's Palo Alto office as the Bay Area's FEMLAB sales, support and education center.

Most engineers are very familiar with FEA codes and the results you can expect from them. There are a number of tools on the market, all specializing in some aspect of engineering analysis. Of late multiphysics analysis is becoming more and more important and companies are rising to this challenge. The problem is that the scope of analysis envisioned by the FEA developers is frequently inadequate for today's complex, many-faceted engineering challenges. Some codes allow the user access to programming tools, some as simple as user-defined functions. The more sophisticated tools allow access the underlying mathematics solved by the program. Using these, your finite element package can be adapted to solve problems you never thought you could.

Using COMSOL's FEMLAB, a commercial FEA code that allows such access, the speaker will show a variety of techniques, ranging from the simple to the not-so-simple to show how to accomplish this yourself. These will include linking FEA to lumped mass systems, building in feedback and control, linking 2D to 3D, properly adding viscous loss terms to flatten shallow 3D microfluidics channels into 2D flow, adding Newton's laws of motion to an electromagnetic analysis to simulate a magnetic disk brake, creating mappings that allow a code without moving meshes to simulate a spinning generator, indeed, how to add a moving mesh to such a code and simulate electro-static actuation in MEMs. We will see how to link regimes together to simulate jump conditions (such as the thermal and voltage drop across thin mylar tape) and we will see an easy approach to adding terms to incompressible flow equations to simulate thermally expanding (and thus accelerating) flow.

This will not be a detailed mathematical talk, rather it will be an overview that strives to stretch your view of what can be done with your FEA tool (provided it gives you access to some user-defined features) well beyond what you think are its bounds and limits.

SCV Electron Devices

TUESDAY JULY 12

Dielectric Scaling Challenges And Approaches in Floating Gate Non-Volatile Memories

Speaker: Dr. Stephen Keeney, Intel Corporation
Time: Pizza social at 6:00 PM;
Presentation at 6:15 PM
Place: National Semiconductor Corp. Building 31
Large Auditorium, 955 Kifer Road,
Sunnyvale
Cost: none
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/eds/

Dielectric scaling in non-volatile memories (NVM) is approaching the point where new approaches will be required to meet the reliability and performance requirements of future products. For both the tunnel oxide and the inter poly dielectric (IPD), high k materials are being explored as possible candidates to replace the traditional SiO2 and ONO (Oxide/Nitride/Oxide) films used today. New storage node concepts are also becoming attractive as an alternative approach to address some of the dielectric scaling limitations. This presentation will review the current status and discuss the approaches being explored to provide dielectric scaling solutions for future non-volatile memory products.

Stephen Keeney is the Technology Integration Manager at Intel for the 90nm flash technology development program which supports a multi-billion dollar memory business. Stephen obtained his B.E. degree from University College Dublin, Ireland in 1988 and his Ph.D. degree in Microelectronics from the NMRC, Cork, Ireland in 1992. He joined Intel's R&D organization in Santa Clara, CA in 1993 and has worked extensively across many aspects of flash memory and logic development, including device physics innovations, yield analysis, memory test and design architecture, process integration and reliability. Stephen holds six patents and has written over 20 technical papers.

All IEEE Members:

SCV **PACE** (**P**rofessional **A**ctivities **C**ommittee for **E**ngineers) has the opportunity to put together a PE (Professional Engineer) Review class this Fall for the Electrical Engineering discipline, in cooperation with a strategic partner. There may also be an opportunity to put on an FE (Fundamentals of Engineering) review (usually the first step toward a PE) if we have enough interest.

Please e-mail John Westmoreland at

PE_FE_Review@WestmorelandEngineering.com

if you are interested in:

1) Taking the course - if so, which one (PE review, FE review, or maybe both?)
2) Interested in volunteering - if so:
   a) As an instructor - please specify subject area
   b) As a volunteer

SCV Lasers and Electro Optics

TUESDAY JULY 12

Making a Many-Colored Processing Engine: Signal Processing with Optical Filters

Speaker: Prof. Christi Madsen, Texas A&M University
Time: Pizza social at 7:00 PM; Presentation at 8:00 PM
Place: Cadence, Pebble Beach Auditorium (note the change in location, effective only for this meeting), 2655 Seely Avenue, San Jose
Cost: none
RSVP: to Ram Sivaraman, ramsivaraman@ieee.org
Web: ewh.ieee.org/r6/scv/leos/

Christi Madsen received the Bachelor's degree from The University of Texas at Austin in 1986, the Master's degree from Stanford University, Stanford, CA, in 1987, and the Ph.D. degree from Rutgers University, Piscataway, NJ, in 1996, all in electrical engineering. She joined AT&T Bell Laboratories in 1987 and worked for the submarine systems business unit. After completing her Ph.D., she transferred to the integrated photonics research department at Bell Laboratories. Since then, her research has focused on the application of digital filter and signal processing techniques to optical filters for high-speed, high-capacity optical communication systems. In 1998, Madsen invented a class of tunable, multi-stage optical allpass filters that allow any phase response to be approximated and have application in chromatic dispersion compensation and polarization mode dispersion compensation. She has given a short course on "Optical Filters for WDM Systems: Theory, Technologies, and Applications" at OFC and is the 2004 General Chair for the Integrated Photonics Research (IPR) Conference. She was promoted to Distinguished Member of the Technical Staff at Bell Laboratories in 2002 and achieved Fellow ranking in the Optical Society of America in 2003. She holds 16 U.S. patents and has given over 70 technical talks and papers. She is now a professor at Texas A&M University in College Station, TX.

The ultimate information capacity of optical fibers is far beyond currently deployed systems even with the exponential growth in system capacity over the past 20 years. Even now, the performance of high-capacity, long-distance wavelength-division-multiplexed (WDM) networks depends significantly on reconfigurable optical filters for bandwidth management and adaptive filters for compensating analog impairments. Optical filters are also key elements in optical code generation and detection with applications in optical packet header processing. Whether the end goal is for communications or high-speed signal processing, optical filters that can operate on amplitude, phase and polarization are critical to unleashing the full potential of optical systems. To be practical, a cost-effective implementation that can scale in optical circuit integration density and functionality is required. This talk addresses optical filters in the context of their analog and digital relatives. I will show how well-known filter types are related to the underlying interference mechanisms and how digital filter theory concepts are beneficially translated to the optical domain. Then, the present capabilities of integrated optics for implementing adaptive optical filters and an overview of some challenges ahead will be discussed. Adaptive filters implemented using high-index-contrast silica-on-silicon planar waveguides with applications to tunable chromatic dispersion compensation and polarization monitoring, control and polarization mode dispersion compensation will be used as examples. With state-of-the-art integrated optical filters, we have the ability to realize a many-colored, high-speed and cost-effective processing engine that truly harnesses the power of photonics.

OEB Communications

TUESDAY JULY 19

IEEE 802.16 Wireless Metropolitan Area Networks

Speaker: Roger B. Marks, National Institute of Standards and Technology, and Chair of 802.16
Time: Pizza social at 6:30 PM; Presentation at 7:00 PM
Place: Bishop Ranch 1, 6101 Bollinger Canyon Road, San Ramon
Cost: none
RSVP: Please send an email by July 18 to oeb@comsoc.org to allow us to order the correct number of pizzas
Web and map: www.comsoc.org/oeb/

Roger B. Marks is with the National Institute of Standards and Technology (NIST) in Boulder, Colorado, USA. In 1998, he initiated the effort that led to the IEEE 802.16 Working Group on Broadband Wireless Access, chairing it since inception and serving as Technical Editor of IEEE Standards 802.16 and 802.16.2. He also serves actively on the IEEE 802 Executive Committee. Dr. Marks received his A.B. in Physics in 1980 from Princeton University and his Ph.D. in Applied Physics in 1988 from Yale University. Author of over 80 publications, his awards include the 2003 Individual Governmental Vision Award from the Wireless Communications Association and a 1995 IEEE Technical Field Award. He developed the IEEE Radio and Wireless Conference and chaired it from 1996 through 1999. A Fellow of the IEEE, he has served as an IEEE Distinguished Lecturer since 1999.

While the world's data transmission capacities are growing at an enormous rate, relatively few users have broadband access to them. Wired solutions, including fiber, cable modems, and digital subscriber lines, have limitations that prevent ubiquitous deployment. Broadband wireless access (BWA) is an alternative that offers quick build-out at a low cost. A key issue for the success of these systems is global standardization. Within the IEEE 802 LAN/MAN Standards Committee, the 802.16 Working Group on Broadband Wireless Access, with hundreds of participants worldwide, has completed the WirelessMAN air interface standard for fixed wireless metropolitan area networks. Supporting industry groups, such as the WiMAX Forum, have blossomed, and the 802.16 WG is nearly finished with an extension of the standard to address mobile terminals as well. This talk provides an overview of the 802.16 technology, which is based on a QoS-oriented, scheduled point-to-multipoint medium access control layer and OFDM/OFDMA physical layers.

We will continue our feature at the meeting of providing some networking time for those that want to stand and make a brief announcement. If you're looking for a new position, have a position to fill, want to let us know that your new start-up is ready for business or have a similar announcement, bring your resumes, job descriptions or company brochures and be prepared to make a match. Please keep your statements brief, so we'll have time for everyone. There will be time before and after the formal meeting for one-on-one discussions.

SCV Nanotechnology

TUESDAY JULY 19

Molecular-Scale Technologies for Electronics and Life Sciences

Speaker: Dr. Jim Hollenhorst, VP and Director of Molecular Technology Laboratory, Agilent Laboratories
Time: Light lunch at 11:45 AM, Presentation at 12:00 noon
Place: National Semiconductor Building 31, 955 Kifer Road, Santa Clara
Cost: $5 IEEE members, $10 non-members
RSVP: Please register on-line on our website
Web: ewh.ieee.org/r6/san_francisco/nntc/

Dr. Jim Hollenhorst serves as Vice President and Director of the Molecular Technology Lab within Agilent Labs. He leads Agilent's research in life sciences, nanotechnology, and MEMS. Formerly, he was responsible for electronics research at HP and Agilent Labs. Before joining HP in 1990, he was with Bell Laboratories, where he worked on high-speed electronics and optoelectronics. Dr. Hollenhorst serves on advisory boards for the Stanford Center for Integrated Systems, the California Nanosystems Institute, and the American Institute of Physics Corporate Associates. He is a member of the AIP Governing Board, a Fellow of the IEEE, and received a doctorate in physics from Stanford University.

We are living through two unprecedented technological revolutions. Advances in electronics are fueled by the relentless pursuit of ever smaller devices embodied in the infamous "Moore's Law", leading to multi-million-fold improvements in performance, size, and cost. The life science revolution is fueled by our increasing understanding and ability to measure and manipulate the fundamental molecules of life. These revolutions are converging at the molecular scale. The techniques of electronics are now being married with those of chemistry and biology to enable the engineering and measurement of structures at the molecular or nanoscale. This talk will describe work in Agilent Laboratories on new devices and measurement techniques enabled by applying the techniques of electronics technology to the field of life sciences, or by novel ways of building and measuring nanoscale structures

August 8-11 on the Stanford University campus
Plenty of free parking

IEEE **Computational Systems Bioinformatics Conference**

Come to CSB'05 for a broad spectrum of peer-reviewed papers covering the breadth and depth of the dynamically evolving field of bioinformatics. Our keynote speakers, paper and poster presentations, tutorials and social events have all been designed to cater to bioinformatics' eclectic mix of disciplines. The low registration fees make it possible for everyone to attend - it's especially easy for "locals" from the Bay Area.

What is "Bioinformatics"?

Bioinformatics - scientific and engineering disciplines bringing new biological discoveries to fields as varied as human health, agriculture, the environment, energy and biotechnology. Find out more at **CSB'05**, where this year's theme is "Connectivity Matters."

Tutorials on Monday:

Demonstration Projects in Clinical Informatics - Novel Visualization and Analysis Methods in BioImaging - Introduction to the Semantic Web for Bioinformatics - The Biological Data Deluge through Phylogenetics - Statistical Approaches to Analyzing Biological Networks - and more

See the one-page flyer on **Page 5**

Visit **conferences.computer.org/bioinformatics**

THURSDAY JULY 21

Reliability of Lead-free Solder Joints: Intermetallic Reactions

Speaker: Prof. King-Ning Tu, Materials Science & Engineering, UCLA
Time: 11:45 AM - 1:15 PM, buffet lunch
Cost: $15 (or $20 at the door)
Place: Ramada Inn, 1217 Wildwood Ave (Fwy 101 frontage road, between Lawrence Expy and Great America Pkwy), Sunnyvale
RSVP: Please reserve and pay in advance using our PayPal on-line system or email John Jackson, john.jackson@analog.com
Web: www.cpmt.org/scv/

Professor K.N. Tu holds a B.S., National Taiwan University; M.S., Brown University; Ph.D. in Applied Physics, Harvard University(1968). He worked at IBM's T.J. Watson Research Center for 25 years, managing their Thin Film Science department and as Senior Manager of the Materials Science Department. For the past 12 years he has been on the faculty of the Materials Science & Engineering department at UCLA, including 5 years as chair of the department.

Dr. Tu has been a Science Research Council Senior Research Fellow and The Royal Society Guest Research Fellow at Cavendish Laboratory, UK; Fellow of American Physical Society; Fellow of the Metallurgical Society; Overseas Fellow of Churchill College; Application to Practice Award of the Metallurgical Society; Alexander von Humboldt Research Award for senior US scientists; President of the Materials Research Society in 1981. His research interest is in kinetic processes in thin films, metal-Si interfaces, electromigration, Pb-free solder metallurgy, low dielectric constant thin films, and phase changes driven by high current density and high electric and magnetic fields. In addition to over 300 articles, he has published a book entitled Electronic Thin Film Science.

Reliability of solder joint technology has been a concern throughout the microelectronics industry -- for example, the low-cycle fatigue induced by thermal stress in flip chips. At present, the risk of fatigue problems has been greatly reduced by the invention of underfills applied between a flip chip and its substrate. On the other hand, due to the recent drive toward Pb-free solders, new reliability issues have emerged, such as Sn whisker growth on Cu leadframes finished with eutectic SnCu or matte Sn. Furthermore, because of the demand of added functions in advanced consumer electronic devices, electromigration is now a serious reliability issue because of the increase of current density in each solder joint.

This luncheon talk will focus on solder reaction, spalling of intermetallic compound in thin under-bump metallization (UBM) and Kirkendall void formation in thick under-bump metallizations.

Two additional topics will be covered in the CPMT Chapter's afternoon Seminar, from 1:30 – 4:30 PM:

- Electromigration Effects in Solder Joints
- Tin Whisker nucleation and growth

See the separate registration for the afternoon Seminar (which includes the lunch and lunch talk) at:

www.cpmt.org/scv/

CONFERENCE CALENDAR

The **CONFERENCE CALENDAR** is a service to our IEEE Members. It outlines upcoming IEEE workshops and conferences in the Bay Area. Please submit items to the GRID Editor: editor@e-grid.net.

Conferences are also encouraged to purchase display space in the **GRID.pdf** and publicize their events on our website and in our **e-GRID** email notification service. For the Conference Publicity flyer, please download:

www.e-grid.net/docs/conf-flyer.pdf

July 17-22: ASME Summer Heat Transfer Conference co-located with InterPack – Integration and Packaging of MEMS, NEMS, and Electronic Systems

- July 17: Tutorials - July 18-22: Conferences & Exhibits

One registration gets you access to sessions and panels in either conference, with over 40 tracks to chose from. Held at the St. Francis Hotel on Union Square in San Francisco, it is easily accessed via BART and MUNI, with parking nearby.

See **Page 8** for more details

July 24-28: IEEE/ASME Int'l Conference on Advanced Intelligent Mechatronics

Theme:

Intelligent Mechatronics in Micro/Nano Technologies

Held in beautiful Monterey

The purpose of this biennial conference is to promote activities in various areas of mechatronics by providing a forum for exchange of ideas, presentation of technical achievements, and discussion of future directions. **Mechatronics** is the synergistic integration of precision mechanical engineering with advanced electronics and computer control in the design and manufacture of intelligent products and processes. The conference is returning to the USA for the second time.

See: www.aim2005.mtu.edu/

16th Annual Magnetic Recording Conference

"Heads and Systems"

August 15-17, 2005

Held at Stanford University in Palo Alto

See **Page 4** for more details

August 8-11: IEEE Computational Systems Bioinformatics Conference

- August 8: Tutorials - August 9-11: Sessions
- At Stanford University (plenty of free parking)

CSB2005 brings you cutting-edge research on biological discovery and innovation through multidisciplinary presentations that can change the world of biology, medicine and drug discovery – and by changing this world, change the lives of the people waiting for cures. **CSB2005** provides a broad spectrum of peer-reviewed, bioinformatics-related topics covering the breadth and depth of this dynamically evolving field.

See Page 5 for more details
