Chapter Meetings and Events

SF-IAS - 9/27 | **Overview: IEEE Standard 1015 ("Blue Book")** - Applying low-voltage circuit breakers in Industrial Systems ... [more]

SCV-WIE - 9/27 | **Primer on MEMS** and **Optical MEMS** - two talks on nanotechnology and MEMS ... [more]

SCV-CE - 9/27 | **Video Compression: Principles, Practice and Standards** - overview, plus current and emerging image and video coding standards ... [more]

SCV-Rel - 9/28 | **Built-In Soft Error Resilience for Robust System Design** - radiation-induced logic soft errors … [more]

SCV-EMS - 9/28 | **Who the Engineering Manager Is and Isn't** and **Managing in the Wireless Sensing Industry** - skills and characteristics for great managers, and "smart dust" ... [more]

SCV-Nano - 9/30 | **Investing in Nanotechnology** - doing nanotech deals, emerging business models, perception of opportunities ... [more]

SF-IAS - 10/1 | **Full-day Seminar: 2004 California Electrical Code** - for Electrical Facility Engrs and Design Consultants ... [more]

SF-PES - 10/4 | **Annual Banquet: The Future of California Energy** - re-examining reliability standards and the adequacy and security of system infrastructure ... [more]

SCV-CPMT - 10/12 | **Imprint Patterning: An Alternative Circuit Fabrication Process**- ... a microreplication operation [more]

OEB-IAS - 10/13 | **AC Control Power and Digital Protective Relays: Avoiding the Pitfalls** - issues and techniques for digital relays requiring a separate control power source ... [more]

SCV-MTT - 10/13 | **The CloudSat Experimental Satellite 94 GHz High-Efficiency Radar Antenna** - shaped offset high-efficiency tri-reflector antenna ... [more]

SCV-Mag - 10/18 | **A Process View of Recording Head Technology** - feature sizes down to 100 nm in just a decade ... [more]

SCV-EMB - 10/19 | **Neural Basis of Reach Preparation and Communication Prosthetics** - cortically-controlled prosthetic systems based on how the brain helps execute movements ... [more]

SCV-SSC - 10/20 | **A Single-Chip Quad-Band GSM/GPRS Transceiver in 0.18um Standard CMOS** - fully integrated, with high sensitivity and low phase error ... [more]

SCV-CNSV - 10/22 | **One-Day Consultants' Business Seminar** - low-cost educational seminar about Consulting as a career ... [more]

SCV-CPMT - 10/27 | **Drop Testing of Components in Portable Applications** - portable devices (cell phones, PDAs) are more likely to be dropped than affected by changes in thermal condition ... [more]

SCV-IM - 11/2 | **Blackfin: A Combined RISC/Signal Processing Architecture for a New Era** - embedded processor for audio, video, and communications applications ... [more]

SCV-CPMT - 11/9 | **Carbon Nanotubes: Enhancing Conductivity of Conductive Plastics** - ... [more]

Upcoming Conferences in the Bay Area

Oct 24-27: **Fall Processor Forum: The Road to Multicore** in San Jose - seminars, sessions, new-product announcements - early-bird rates thru Sept 30th [more]

Oct 24-27: **GSPx'05: Pervasive Signal Processing Conference and Expo**, at Santa Clara Convention Center; special **GRID** discounts for our readers [more]

Call for Papers: ISQED'06
Int'l Symposium on Quality Electronic Design
San Jose … Manuscripts due Oct. 14th [more]

Nov 6-10: **ISTFA: Int'l Symposium on Testing and Failure Analysis**, at San Jose Convention Center; Workshops, Sessions, User-Group meetings [more]

Full-day Seminar: 2004 California Electrical Code
Oct 1 ... for facility engineers, design consultants [more]

Full-day: Consultants' Business Seminar –
Oct. 22 Learn about Engineering Consulting as a career [more]

Professional Skills Courses from EMS, CPMT, ETA:

Clear Business, Technical, and E-mail Writing
Oct 6 at Cypress Semiconductor, San Jose [more]

Leadership Skills for Engineers
Oct 19 at LSI Logic, Milpitas [more]

Communication & Conflict Management Using Myers-Briggs Oct 20 at Cypress, San Jose [more]

Memory Power
Oct 27 at Exar Corporation, Fremont [more]

Finance for Non-Finance Professionals
Nov 1 at Cypress Semiconductor, San Jose [more]

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Conference Calendar page 26

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IEEE **GRID** is the monthly newsmagazine of the San Francisco Bay Area Council of the Institute of Electrical and Electronics Engineers, Inc. As a medium for both news and opinion, the editorial objectives of IEEE **GRID** are to inform readers in a timely and objective manner of newsworthy IEEE activities taking place in and around the Bay Area; to publish the official calendar of events; to report on IEEE activities of a national and international scope; and to serve as a forum for comment on areas of concern to the engineering community by publishing contributed articles, invited editorials and letters to the editor.

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From the editor . . .

The local IEEE – as seen by most members – consists of perhaps 30 different Chapters organizing lunch or evening meetings, instructional seminars and workshops, and assisting all local technologists with an interest in each of these specialties. Together, they give us a myriad of interesting and provocative topics each month.

The task of the **GRID** Magazine is to make it as easy and painless as possible to link each member up with the information needed to find, register for and attend the one (or two) that will assist that particular engineer or manager in learning about some new area of our technology and in networking with similar professionals (remember: the **GRID** is "your networking partner!")

This month we're trying something new. I've created a one-page PDF that is a small enough file that it can be attached to the e-GRID email. This single page serves as an index to all the upcoming events, with hyperlinks that allow you to quickly access the individual **GRID** page for a particular meeting. With one click, you can download a profile of the topic (and a bio of the speaker), see where the meeting will be held, and find out whether there is a fee and how to reserve one or more seats.

Not only that – once you've accessed the PDF page for a particular event, you can easily attach it to an email to co-workers, inviting them to consider attending that meeting in their technical specialty. Everybody's career is advanced when we are all mastering new technologies and techniques!

Yes, it takes me more time to set this up. Let's see how it works, for you, after trying it for a month or two. If you have reactions or suggestions, please send me a note.

Paul Wesling **editor@e-grid.net**

NOTE: This PDF version of the IEEE GRID – the **GRID.pdf** – is a monthly publication and is issued a few days before the first of the month. It is not updated after that. Please refer to the Online edition and Interactive Calendar for the latest information: **www.e-GRID.net**

Professional Services Marketplace – editor@e-GRID.net for information

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Full-day Seminars: Monday and Thursday
Keynotes and Sessions: Tuesday–Wednesday
Doubletree Hotel, San Jose (plenty of free parking)

Integrating two or more processor cores on a single chip is the hottest trend in high-performance microprocessor design. And it's not just for PCs and servers -- embedded processors are actually setting the pace, with some new designs boasting more than a hundred cores.

If you design chips or systems, you simply can't avoid multicore technology. If you're a programmer or system-software engineer, soon you'll face the challenge of writing or acquiring software for a multicore processor. The one conference where anyone interested in multicore integration can ramp up their knowledge is the **Fall Processor Forum**. **FPF 2005** will focus on three key topics:

- announcements of new multicore processors
- technical presentations about products and technologies for multicore chip designers
- technical presentations about multicore software

Much of this information will be relevant to cutting-edge single-core designs, too.

Technical Sessions:

Bring your laptop – use our wireless LAN access to download any/all presentations. Also available on a CD ROM.

- Multicore Processors
- Innovative IP
- Processor IP for Multicore
- Building Systems with Multicore Processors
- High-Performance Digital Signal Processing
- On-Chip Interconnect for Multicore

Register for technical sessions only – or a Seminar – or the full FPF'05. Register by September 30th for Early-Bird specials:

- **Save $500 on Forum registration**
- **Save $700 on full FPF'05 admission**

FPF 2005 focuses on multicore processors, including new product introductions and other dimensions of multicore processing, such as system software and on-chip interconnects. It is the **one-stop shop** for engineers, engineering managers, project leaders, strategic planners, and marketers who need to quickly ramp up their knowledge about this fast-breaking technology.

- ARM will reveal the first technical details about the microarchitecture of **Tiger**, its first superscalar embedded-processor core.
- IBM will deliver three blockbuster presentations: Software development for the Cell processor in Sony's next-generatio **PlayStation 3**, the microarchitecture of the triple-core PowerPC chip in **Microsoft's XBox 360**, and a new dual-core **PowerPC G5-class processor**.
- P.A. Semi will emerge from stealth mode to announce its first microprocessor by former designers of the DEC Alpha and MIPS-compatible SiByte families.
- StarCore and Texas Instruments will introduce sophisticated new **DSP cores and chips**.

One-Day Seminars at FPF'05:

Monday: Implementing Low Power SoC Configurations

A brief tutorial on the latest strategies used in design for low power, and trends for sub-90nm processes; analysis of more than 25 core, chip and SoC products including the latest introductions aimed at cellular telephones, digital cameras, PDAs and other power-aware systems.

Thursday: A Briefing on DSP Technology

The most recent key information on DSP technology will be presented straight from the source – the technical experts of Analog Devices, CEVA, Starcore, and Texas Instruments and moderated by Max Baron, Microprocessor Report's authority on DSP's.

Additional information is on the FPF web site:

www.in-stat.com/fpf/05/ CLICK!

31st International Symposium for Testing and Failure Analysis

November 6-10, 2005 • San Jose, CA USA

Exposition: Tuesday-Wednesday, Nov 8-9

Held this year for the first time at the San Jose Convention Center, ISTFA'05 combines technical sessions, tutorials, an exhibition, and user group meetings with a focus on making the full experience a strong benefit for the attendee. The limited number of selected, high-quality papers only requires two tracks throughout the program, for good access.

Technical Sessions:

• Die Level Fault Isolation • Package Level Analysis
• System Level Analysis • Advanced Techniques
• Optical Techniques • Optoelectronic Devices
• Failure Analysis Process • Circuit Edit for FA, FI, and Debug • Case Histories • SPM Techniques
• Sample Preparation • Nanotechnology Analysis
• Yield Enhancement • Discretes, Passives, and MEMS • Metrology and Materials Analysis • Test
• plus Poster Papers

Panel Discussions:

- Strategic Development in FA. What Can We Get From Other Technical Sources?
- Can Competitors Build Some Common FA Facilities To Improve ROI And Efficiency?

Tutorials:

• Failure Analysis Basics • Device and Packaging
• Microscopy Tools • Yield • Sample Preparation
• Fault Isolation • MEMS • Failure Mechanisms
• Failure Analysis Laboratory Management

.... plus **User Group meetings** on Tuesday and Wednesday evenings, to provide a convenient forum for users of a specific technique to meet, share ideas, and discuss relevant issues in a non-commercial environment. Planned topics this year:

- Scanning Optical Microscopy (SOM)
- Scanning Probe Microscopy (SPM)
- Focused Ion Beam (FIB)
- Chip Access/Delayering
- Nano Probe

Luncheon Address:

Dr. Johannes Stork, Senior Vice President and Chief Technology Officer, Texas Instruments

As Director of the Silicon Technology Development organization, Dr. Stork's primary responsibilities are the development of advanced CMOS, packaging and mixed signal process technologies.

ISTFA is the best venue for learning new failure analysis techniques, challenges and directions. It also provides ample opportunities for you to participate and network through the question-and-answer periods, the user groups, the panel discussions, the exhibition, and the networking poster luncheon.

Additional information is on the ISTFA web site:

www.ISTFA.org CLICK!

- Online conference registration begins Sept. 15th. Download the registration form at:

  www.e-grid.net/conf/istfa-reg.pdf

- Discounted fees for EDFAS and ASM Members. Non-Members of EDFAS receive a full year's membership with their registration.

Tutorials-only and Exhibits-only registrations are available. To exhibit at ISTFA, please contact **Mr. Charles Dec:**

charles.dec@asminternational.org

EDFAS General Membership Meeting

Tuesday, November 8, 4:40-5:30 pm

The **E**lectronic **D**evice **F**ailure **A**nalysis **S**ociety (EDFAS) will hold its annual General Membership Meeting on Tuesday at ISTFA. It is open to all current members, as well as interested prospective members.

Call for Papers

www.isqed.org

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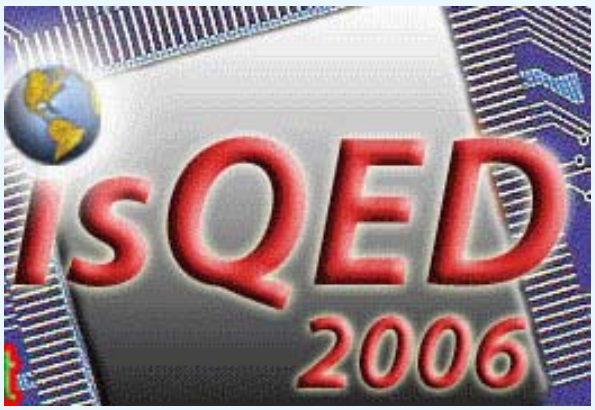

March 27-29, 2006
San Jose, CA, USA

Design for Quality in the Era of Uncertainty

ISQED is the pioneer and leading international conference dealing with the design for manufacturability and quality issues front-to-back. ISQED spans three days, Monday through Wednesday, in three parallel tracks, hosting near 100 technical presentations, six keynote speakers, two-three panel discussions, workshops/tutorials and other informal meetings. Conference proceedings are published by the IEEE Computer Society and hosted in the IEL/XPLORE digital library. Proceedings CD ROMs are published by ACM. In addition, continuing the tradition of reaching a wider readership in the IC design community, ISQED will continue to publish special issues in leading journals. The authors of high quality papers will be invited to submit an extended version of their papers for the special journal issues.

Papers are requested in the following areas

- **Design for Manufacturability & Quality**
- **Package - Design Interaction & Co-Design**
- **Design Verification and Design for Testability**
- **Embedded Test Methodologies**
- **Robust Device, Interconnect, and Circuits**
- **EDA Tools & IP Blocks; Interoperability and Implications**
- **Physical Design, Methodologies & Tools**
- **Effect of Technology on IC Design, Performance, Reliability & Yield**
- **Design Quality Definitions, Metrics, and Standards**
- **Quality Driven Design Flows; SoC, ASIC, FPGA, RF, Memory, etc.**
- **Quality of Modeling Abstractions and Methods (Device, Interconnect, Micro and Macro Cells, IP Blocks, ...)**
- **System-level Design, Methodologies & Tools**
- **Redundancy & Self Correction Design Techniques**
- **Management of Design Process, and Design Database**
- **Global, Social, and Economic Implications of Design Quality**
- **Quality based EDA Tools, Design Techniques, and**
- **Methodologies dealing with issues such as:**
  - **Timing Closure**
  - **R, L, C Extraction**
  - **Ground/Vdd Bounce**
  - **Signal Noise/Cross-Talk /Substrate Noise**
  - **Voltage Drop, Power Rail Integrity**
  - **Metal Migration, Hot Carriers**
  - **High Frequency Effects**
  - **Thermal Effects**
- **Power Estimation**
- **Plasma Induced Damage, and yield limiting effects**
- **EMI/EMC**
- **Proximity Correction & Phase Shift Methods**
- **Verification (Layout, Circuit, Function, etc.)**
- **EOS/ESD**
- **Packaging Modeling and Simulation**

IMPORTANT DATES:

Paper Submission Deadline	**October 14, 2005**
Acceptance Notification	**November 22-24, 2005**
Final Camera-Ready Paper	**January 3, 2006**

Submission Process

The guidelines for the final paper format are provided on the conference web site at **www.isqed.org**. Authors should submit FULL-LENGTH, original, unpublished papers (Minimum 4, maximum 6 pages). To permit a blind review, do not include name(s) or affiliation(s) of the author(s) on the manuscript and abstract. Submit your papers using the on-line paper submission procedure available on the ISQED web site. Please check the as-printed appearance of your paper before submitting the paper. Address all other inquiries to **publication@isqed.org**.

IEEE Professional Skills Courses

SCV Chapters, Engineering Management & Components, Packaging and Manufacturing Technology Societies

Clear Business, Technical, and E-mail Writing

- Date/Time: Thursday, October 6, 8:30AM-4:30PM
- Instructor: Kathleen Mohn
- Location: Cypress Semiconductor, San Jose
- Fee: $375 for IEEE Members; $425 non-members

This workshop provides a step-by-step process for designing and writing a clear engineering document, e-mail message, or report. You will learn by doing, the only legitimate way to improve writing skills! The training involves writing, revising, and editing exercises; critiquing documents; games; and lecture. You will walk away with confidence in writing and editing skills and with a consciousness about international writing.

Leadership Skills for Engineers

- Date/Time: Wed, October 19, 8:30AM-4:30PM
- Instructor: Dr. Andrew Oravets
- Location: LSI Logic, Milpitas
- Fee: $350 for IEEE Members; $425 non-members

The challenges of leadership in high-tech companies have never been greater. Today's manager must be fully aware of his/her style and be able to adjust to fit the needs of others and the demands of the situation. In addition, obtaining relevant information and sharing it appropriately requires skills in phrasing questions, listening and speaking for results. This high-impact, one-day workshop provides technical managers with analytical tools and cultivates "street smarts".

Finance for Non-Finance Professionals

- Date/Time: Wed, November 1, 8:30AM-12:30PM
- Instructor: Roxanna Dunn
- Location: Cypress Semiconductor, San Jose
- Fee: $275 for IEEE Members; $300 non-members

Communication & Conflict Management using Myers-Briggs (MBTI)

- Date/Time: Thursday, October 20, 8:30AM-4:30PM
- Instructor: Linda Price
- Location: Cypress Semiconductor, San Jose
- Fee: $350 for IEEE Members; $425 non-members

The Myers-Briggs Type Inventory (MBTI) is the most widely used instrument in the world to gain a deeper understanding of self, others and interpersonal relationships. It provides insights on the four basic "people patterns" that hold the key to leadership styles, effective communication, conflict, team building and productivity.

Key Topics: Discover your Myers-Briggs Type – Understand four basic "people patterns" and how they think and act – Discover your preferred communication and conflict style – Build trust and rapport through communication – Practice how to communicate and influence each type – Learn how to use questions that gain quality information – Separate facts from emotions – Speak with clarity and commitment

Memory Power (half-day)

Date/Time: Thursday, October 27, 8:30AM-12:30PM
Instructor: Linda Price
Location: Exar Corporation, Fremont
Fee: $275 for IEEE Members; $300 non-members

You'll learn how to easily remember names, numbers, events, faces, and facts; this course is packed with practical ideas that you can use every day of your life.

Improve your skills – register for one of these classes, or for others coming up this fall. Bring a team!

For complete course information, schedule, and registration form, see our website:

www.effectivetraining.com

Consultants' Network of Silicon Valley

Consultants' Business Seminar

CBS-2005 is an educational seminar about Engineering Consulting as a career. This event has important information for both new and experienced consultants. **CBS-2005** covers the basics with topics including Rate Surveys, Best Use of Contract Broker Agencies, Contracts & Negotiations, how to use the internet to get leads, and more. Plus "Weather Reports" about What's Hot and What's Not, "What the IEEE National and IEEE AICN are up to" these days, and Current Events Issues including the realities of Off-Shoring and the opportunities for Consultants.

Saturday, October 22, 2005
8:30 AM – 4:30 PM
at Keypoint Credit Union
2805 Bowers Ave, Santa Clara

The Program is a mix of panels and speakers, with dual tracks for several one-hour sessions in morning.
**** Low Cost, High Value ****

	Early Reg'n by Oct 13, 05	Regular Reg'n after Oct 13, 05
Members	$45.00	$57.00
Non-Members	$60.00	$72.00

Includes Continental Breakfast and Sandwich-Buffet Lunch

Information: **www.e-grid.net/docs/0510-scv-cnsv.pdf**

SCV Product Safety Engineering

TUESDAY SEPTEMBER 27

Changes in What We Know about Circuit Protection: Is it a Circuit Breaker or Not?

Speaker: Ashley Harknes, eti Conformity Services
Time: dinner at Bowers Cafe at 5:45 PM, Presentation at 7:00 PM
Cost: no-host dinner; no cost for presentation
Place: Applied Materials (Bowers Cafe), 3090 Bowers Ave, Santa Clara
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/pses

Ashley Harkness comes to us from, eti Conformity Services, a division of Electrical Reliability Services (formerly Electro-Test, Incorporated) of San Ramon, California. eti Conformity Services is the largest independent testing company in the United States servicing the commercial and industrial electrical market.

On assignment in Japan, Mr. Harkness was presented with what looked like a circuit breaker, but was not listed as such. He had to determine whether it was acceptable and under what circumstances. What followed was an extensive "What are You Protecting and Why?" discussion with the manufacturer. Surprisingly, the answers have been altered by changes in new products, requirements, and system capabilities. This discussion will clarify several issues regarding Circuit Protection changes.

TUESDAY SEPTEMBER 27

Overview of IEEE Standard 1015-1997 ("Blue Book")-- "Recommended Practice for Applying Low-Voltage Circuit Breakers Used in Industrial and Commercial Power Systems"

Speaker: David D. Roybal, Eaton Corporation
Time: Social at 5:30 PM, Presentation at 6:00 PM, Dinner at 7:00 PM
Cost: $25 (at the door)
Place: Sinbad's Restaurant, Pier 2 The Embarcadero, San Francisco (415.781.2555)
RSVP: Please preregister by email at jlin@sfwater.org to qualify for the drawing
Web: www.ewh.ieee.org/r6/san_francisco/ias

This presentation will be an overview of the IEEE Blue Book which provides information for selecting the proper circuit breaker for a particular application. This information helps an engineer specify the type of circuit breaker, ratings, trip functions, accessories, acceptance tests, and maintenance requirements required. It will include a discussion of circuit breakers for special applications, application at different points in the power system, and selective coordination, as well as a comparison between the standards of low-voltage power circuit breakers and molded-case circuit breakers.

David D. Roybal received the Bachelor of Science degree in electrical engineering from Santa Clara University in 1969. He is a Fellow Application Engineer with Eaton Corporation in Livermore. He previously was an engineer with Westinghouse for more than 24 years. Mr. Roybal is a Senior Member of the IEEE who has served as an officer of the San Francisco chapter of the IEEE-IAS, the IEEE San Francisco Section, and the IEEE Bay Area Council. He is a member of NFPA, NSPE, and chairman of the NEMA California Safety Regulations Advisory Committee. He is chapter secretary for the International Association of Electrical Inspectors (IAEI), a member of the Executive Board of the California Electrical Inspectors (CEI), and a registered professional engineer. He has had three papers published by IEEE on the subject of circuit breakers.

SCV Women in Engineering

TUESDAY SEPTEMBER 27

Primer on MEMS *and* A Large-scale Integrated Mirror Array for Optical Communications

Speakers: Alissa Fitzgerald, A. M. Fitzgerald & Assoc, and Anthony F. Flannery Jr., Director of Development - MEMS Gyroscope, Invensense, Inc.
Time: Social at 6:00 PM, First presentation at 6:30 PM, Second presentation at 7:30 PM
Cost: none
Place: Stanford University's CISX Auditorium (Center for Integrated Systems Extension)
RSVP: Please preregister by email at k.chin@ieee.org
Web: www.ewh.ieee.org/r6/scv/wie

Driven by the dot-com era's need for communications bandwidth, Micro-Optical Electrical Mechanical Systems (MOEMS) promised new advantages for telecommunication companies. While market conditions caused many of the ventures in this area to fall short of investor expectations, many new advances were made in the area of MEMS fabrication and design during the optical MEMS bubble. Presented here is the large-scale integration of electronics with MOEMS mirrors. A novel design was conceived in which integrated electronics driving 1200 mirrors dissipate only 2W, or under 400 µW for each electrode. The process includes a novel bulk micromachining process and electronic integration through wafer bonding.

Dr. Alissa Fitzgerald has interests that include mechanical design and analysis for advanced applications; sensor systems; MEMS design and fabrication; materials science; and reliability testing. She has worked on projects as diverse as MEMS sensors for spacecraft and medical applications, condition-based maintenance systems for military helicopters, and the study of hot electron injection into PECVD dielectrics. She has been employed by the Jet Propulsion Laboratory, Orbital Sciences Corporation, Signal Processing Associates, and Sensant Corporation. Dr. Fitzgerald received her bachelors and masters degrees from MIT and her doctorate from Stanford University, all in the discipline of Aeronautics and Astronautics.

Anthony Flannery received his B.A. in chemistry from Princeton University. He received his MSEE at Stanford University. At Stanford his research focused on the development of PECVD silicon carbide for environmentally hardened chemical and pressure sensors. Other significant accomplishments include the use of dry film lithography for non-planar substrates, stress control in deposited films, and laser ablation for patterning on MEMS substrates. In June of 2003 he joined the founding team of Invensense. Invensense successfully raised $8 million. As Director of Development, he was co-inventor of a novel silicon bulk micromachining process which included a hermetic seal achieved by wafer bonding with a custom ASIC. Prior to Invensense, he was with Transparent Networks where he managed the successful development of the world's largest integrated mirror array for optical communications.

SCV CONSUMER ELECTRONICS

TUESDAY SEPTEMBER 27

Video Compression: Principles, Practice and Standards

Speaker: John Apostolopoulos, Streaming Media Systems Group, HP Labs
Time: Pizza and Networking at 6:3 PM, presentation at 7:00 PM
Cost: IEEE Member $5, non-IEEE member $10
Place: Oak Room at HP, 19447 Pruneridge Avenue (Building 48 - Wolfe and Pruneridge), Cupertino
RSVP: Please preregister by email at scv.ce@ieee.org
Web: www.ewh.ieee.org/r6/scv/ce/

This talk will provide an overview of image and video coding, discussing both the basic principles of how compression is achieved as well as how these principles are applied in practice. We will also highlight the current and emerging image and video coding standards, including the recent H.264 / MPEG-4 Advanced Video Coding (AVC) standard. By the end of this informal talk, the audience will know the basics of the JPEG and MPEG family of compression standards, as well as how these standards are used in applications such as Digital TV, DVDs, and video streaming over the Internet. This talk is designed for an audience with EE or CS background, but without requiring any prior compression expertise.

John Apostolopoulos received his B.S., M.S., and Ph.D. degrees from MIT. He joined HP Labs in 1997 where he is currently a principal research scientist and project manager for the Streaming Media Systems Group. He also teaches a graduate course on video signal processing at Stanford, where he is a Consulting Assistant Professor of electrical engineering. He received a best student paper award for part of his Ph.D. thesis, the Young Investigator Award (best paper award) at VCIP 2001 for his paper on multiple description video coding and path diversity for reliable video communication over lossy packet networks, and in 2003 was named "one of the world's top 100 young (under 35) innovators in science and technology" (TR100) by Technology Review. John contributed to the U.S. Digital Television and JPEG-2000 Security (JPSEC) standards, and currently serves as HP's primary representative to MPEG. He served as an Associate Editor of IEEE Transactions on Image Processing and of IEEE Signal Processing Letters, and is a member of the IEEE Image and Multidimensional Digital Signal Processing (IMDSP) technical committee, and he is currently co-organizing a special issue of IEEE Network on "Multimedia over Broadband Wireless Networks". His research interests include improving the reliability, fidelity, scalability, and security of media communication over wired and wireless packet networks.

WEDNESDAY SEPTEMBER 28

Built-In Soft Error Resilience for Robust System Design

Speaker: Subhasish Mitra, Intel Corporation
Time: 6:30 PM - refreshments;
7:00 PM - presentation
Cost: none
Place: H-P Oak Room, Bldg 48, Cupertino, just North of Fwy 280 (Wolfe Rd Exit) at the corner of Pruneridge Ave. and Wolfe Rd.
RSVP: not required
Web: ewh.ieee.org/r6/scv/rs/

Dr. Subhasish Mitra is a Principal Engineer at Intel Corporation where he is responsible for developing enabling technologies for robust system design -- Design for Reliability, Testability and Debug -- in advanced technologies. He is also a Consulting Assistant Professor in the Electrical Engineering Department of Stanford University, and the Associate Director of the Stanford Center for Reliable Computing. Before joining Intel, he led the Stanford project on "Reliability Obtained by Adaptive Reconfiguration" sponsored by DARPA as part of the Adaptive Computing Systems program. He also consulted for several companies including Agilent Technologies Laboratories. His research interests include robust system design, VLSI design and test, CAD, fault-tolerant computing and computer architecture. He received Ph.D. in Electrical Engineering from Stanford University.

Dr. Mitra has published more than 70 technical papers in leading conferences and journals, and invented design and test techniques that have seen wide-spread proliferation in the industry. He has received several awards, including the 2005 IEEE Circuits and Systems Society Donald O. Pederson Award for the Best Paper published in the IEEE Transactions on CAD, and the 2004 Intel Achievement Award, Intel's highest corporate award, "for the development and deployment of a breakthrough test compression technology."

Radiation-induced logic soft errors in flip-flops and combinational logic pose a major challenge in the design of robust systems for enterprise computing and networking applications. In the past, soft errors were of concern especially for space applications. Increasing system-level soft error rates in advanced technologies, and stringent system data integrity requirements demand special design techniques to protect systems from logic soft errors. This talk will discuss the impact of technology scaling on soft error rates, evaluation of run-time behaviors of systems in the presence of soft errors, and design of robust architectures incorporating Built-in-Soft-Error-Resilience (BISER) techniques. Design-for-test and debug resources are reused for soft error protection during normal system operation, resulting in 20-fold reduction in flip-flop soft error rate, with negligible area and speed impact, and 3-5% system-level power overhead. In comparison, classical redundancy techniques introduce 40-100% power, performance and area overheads.

SCV Engineering Management

WEDNESDAY SEPTEMBER 28

Who the Engineering Manager Is and Isn't

and

From Smart Dust to Reliable Sensor Networks

Speakers:	Gregory West, Quality Manager, Sipex Corporation; and Kris Pister, Founder and CTO, Dust Networks
Time:	Forum at 6:00; Dinner at 7:00 PM; Second presentation at 7:45 PM
Cost:	$25 (IEEE member), $30 (non member), $5 surcharge after Sept. 23
Place:	Country Inn & Suites (former Prime Hotel and Wyndham), 1300 Chesapeake Terrace, Sunnyvale - off Lawrence Expressway/Caribbean Drive at Hwy 237
RSVP:	through link on website; info from Rich Henderson, (408) 203-3462
Web:	www.ieee-scv-ems.org

Gregory J. West is a 25 year industry veteran with more than 20 years in engineering supervision and management roles forming and leading high performance product development and operations teams in some of the biggest and best known companies including Texas Instruments, National Semiconductor, Philips Electronics, and Samsung Semiconductor, as well as in community based, volunteer, and government organizations. Greg founded Jonathan Byrnes Associates, a management consulting firm in 2003 and currently is the Quality Assurance Manager at Sipex Corporation, a company that designs and produces analog interface, power management, and optical storage integrated circuits. Greg earned his BSEE from Milwaukee School of Engineering, and his MS Engineering Management from Santa Clara University. He is also a registered Professional Engineer in the State of Wisconsin.

Kris Pister coined the phrase Smart Dust as an assistant professor at UCLA in 1995, and wrote the DARPA proposal of the same name in 1997 as a professor at UC Berkeley. From 1998 to 2002 his students set records for the lowest-power 8bit ADC, lowest-power 900MHz radio, and smallest mote, all of which still stand today. Kris is the founder of Dust Networks, raising roughly ten million dollars in private and venture investment.

(Forum talk)

In his article, "Who the Engineering Manager Is Not" published in the IEEE Engineering Management Society Newsletter, Greg claims that truly successful engineering managers are not great leaders, motivators, or technical experts. In fact, he claims that if a person uncontrollably excels in any one of these characteristics, he or she will detract from optimizing the organization's overall success, and will, thereby, fail as a manager. Greg will facilitate an open forum discussion based on these concepts in an effort to come to consensus on what skills and characteristics make great engineering managers.

(Second talk)

The DARPA-driven concept of low-cost ubiquitous sensor networks that took shape in the early to mid 90s is now widely recognized as having a multi-billion dollar potential in markets such as building and industrial automation. Following a brief history of the Smart Dust project and an overview of current industrial sensor network markets, an architecture for enterprise-class reliable low power sensor networking will be presented. To address industrial requirements for reliability in the presence of severe RF interference, this approach implements a time-synchronized frequency-hopped fully-meshed network. In low-rate data gathering applications, measured performance of this architecture is 99.999% end-to-end network reliability, with average current consumption of all motes in the network below 100microAmps. A simple predictive model for network performance will be presented, which allows accurate simulation of network capacity, latency, energy consumption, noise sensitivity, etc. The talk will conclude with some mild pontification about technology directions in the next few years.

Returning to Berkeley in 2005, Kris remains Chief Technical Officer (CTO) at Dust Networks..The inventor of Smart Dust and a longtime leader in the academic wireless sensor networking community. Kris is the chief architect of Dust Networks' patent pending SmartMesh™ technology, and also provides a strong technology vision for the company and for the wireless sensing industry. Previously, Kris successfully commercialized or licensed micro-machine technologies with Tanner Research, OMM Inc., Xactix, and Sony. Kris holds a PhD and MS in electrical engineering and computer sciences from UC Berkeley and a BS from UC San Diego.

SCV Nanotechnology Council

FRIDAY SEPTEMBER 30

Investing in Nanotechnology

Speaker: Alexei A. Andreev, Ph.D., Executive Vice President/Managing Director, Harris & Harris Group
Time: 11:30 AM registration; 11:45 AM light lunch; Noon Presentation
Cost: $5 (IEEE member), $10 (non member) cash or check at door
Place: National Semiconductor, Building 31, 955 Kifer Road, Santa Clara
RSVP: by email to krsmurthy2005@yahoo.com
Web: www.ieee.org/nano

This unique talk will cover the following:

- Specificity of doing nanotech deals
- Novel emerging business models
- Investor's perception of near term and medium term investment opportunities in the field

Dr. Alexei A. Andreev is Vice President/Managing Director at Harris & Harris Group. Prior to that he was an associate with Draper Fisher Jurvetson, a venture capital firm, where he was exclusively focused on nanotechnology and material science investment opportunities. While at DFJ, he played an integral role in sourcing and funding of Solicore, D-Wave Systems, Intematix and EoPlex, where he served as an active Board Director or Observer. Previously, he worked for TLcom Capital Partners, a London-based venture capital fund backed by Morgan Stanley. Prior to that, he was employed by Renaissance Capital Group/Sputnik Funds, a venture capital fund in Moscow, Russia. Before he started his business career, Mr. Andreev was a researcher at the Centre of Nanotechnology, ISAN (RAS), in Troitsk, Russia where he was focused on optical and electrical properties of Quantum Dot heterostructures in strong magnetic fields. Mr. Andreev received his Ph.D. degree from the Department of Theoretical Physics of Moscow Steel and Alloys Institute led by Alexei A. Abrikosov (recipient of the Nobel Prize in Physics 2003), where he was a recipient of the Scholorship for Outstanding Young Scientists of Russian Academia of Sciences, the Scholarship from the International Center of Fundamental Physics and Soros Scientific Foundation. Mr. Andreev also received a B.S. with honors in Engineering/Material Sciences from Moscow Steel and Alloys Institute and with an M.B.A. from Stanford Graduate School of Business. He is a director of the American Business Association of Russian Expatriates.

SF Industry Applications

SATURDAY OCTOBER 1

Full-day Seminar:
Analysis of the Changes in the 2002 National Electrical Code and the 2005 California Energy Efficiency Regulations

Instructor:	Tim Owens, Senior Electrical Inspector, City of Santa Clara
Time:	Registration - 7:30 AM; Seminar - 8:00 AM to 4:00 PM
Cost:	$225 (Early Bird Special by Sept 22: free copy of the Code)
Place:	Wyndham Garden Hotel, 5990 Stoneridge Mall Road, Pleasanton
RSVP:	See details on the website
Web:	www.ewh.ieee.org/r6/san_francisco/ias/

Tim Owens, Senior Electrical Inspector for the City of Santa Clara, is a professional code instructor, past president of the International Association of Electrical Inspectors, and a member of NEC Code Making Panel 18.

The 2004 California Electrical Code became effective August 1 and is based on the 2002 National Electrical Code. The 2005 California Energy Efficiency Regulations (Title 24, Part 6) are effective October 1. An understanding of the changes is important to consulting engineers, facilities engineers, contractors, and others active in the electrical industry.

SF Power Engineering

TUESDAY OCTOBER 4

Annual Banquet: The Future of California Energy

Keynote Speaker: Yakout Mansour, CEO, Ca-ISO
Time: Social at 5:00 PM, Dinner at 6:00 PM, Presentation at 7:00 PM
Cost: $30 Early Bird Special before September 23rd, $35 afterward; , Students - $15, group/table rates available
Place: Sinbad's Restaurant, 2 Embarcadero (Pier 2), SF -- free validated parking on Pier 2
RSVP: Please fill out and return the Reservation and Dinner Choice form
Web: www.e-grid.net/docs/0510-sf-pes.pdf

Recent actions by Congress and other developments in FERC policies have raised questions about the future of the California energy industry. The recently passed Energy Bill and the 2003 NE Blackout have triggered the need to re-examine and mandate NERC reliability standards and evaluate the adequacy and security of system infrastructure. How will these issues affect the California Independent System Operator (CA-ISO), and how is their reorganization positioning them for the future?

Yakout Mansour, CEO of the California Independent System Operator (Ca-ISO), will discuss these issues in detail as the keynote speaker for this event. SF PES will host a short annual awards ceremony during this event. Awards will be presented to notable contributors to the IEEE and the Power Engineering Society. In addition, attendees will enjoy fine dining at Sinbad's Restaurant. Dinner is subsidized by the SF PES ADCOM committee, so that all attendees can enjoy this great memorable evening at a reasonable price. This will be an enjoyable evening for engineers and non-engineers alike, so invite a friend or family member. All are welcome!

SF PES is offering a group discount to this event. Purchase a table for 10 attendees at a price of $250. Corporate Sponsorships are available for $100. Call for details.

Please make your dinner selections using the form at this location:

www.e-grid.net/docs/0510-sf-pes.pdf

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WEDNESDAY OCTOBER 12

Imprint Patterning: An Alternative Circuit Fabrication Process

Speaker:	Dr. Craig Davidson, Dimensional Circuits
Time:	Seated dinner at 6:30 PM; presentation at 7:30 PM
Cost:	$25 if reserved by Oct. 9; $30 at the door; presentation-only is free
Place:	Ramada Inn, 1217 Wildwood Ave (Fwy 101 frontage road, between Lawrence Expy and Great America Pkwy), Sunnyvale
RSVP:	Please reserve and pay in advance using our PayPal on-line system or email Janis Karklins at Karklins@ieee.org
Web:	www.cpmt.org/scv/

A new approach to fabricating printed circuits named Imprint Patterning™ will be described. In conventional printed circuit fabrication two major process elements -- photolithography and laser drilling -- contribute significantly to performance constraints and cost. Imprint Patterning replaces these two steps with a single cost-effective microreplication operation that results in huge cost and performance advantages. These same techniques are used today to fabricate CDs and DVDs with high quality and low cost. And they are on the semiconductor technology roadmap for the sub-40 nm nodes. Dimensional Imprint Technology, Inc. is commercializing Imprint Patterning for the printed circuit industry.

Dr. Craig Davidson is Sr. VP and Chief Technology Officer of Dimensional Imprint Technology, Inc. He has expertise in various high technology industries including electronics and aerospace. Dr. Davidson was previously the VP of Technology for Multilayer Technology, Inc. (Multek) the 12th largest PCB supplier in the world and a wholly owned subsidiary of Flextronics International. His career spans printed circuit fabrication, semiconductor packaging, and card-level assembly processes. Dr. Davidson's degrees are in Chemistry and Materials Science. He holds 7 patents and is widely published in the technical literature.

OEB Industry Applications

THURSDAY OCTOBER 13

AC Control Power and Digital Protective Relays: Avoiding the Pitfalls

Speaker:	Gary Fox, GE Industrial
Time:	No-host social at 5:30 PM; Presentation at 6:15; Dinner at 7:15; Presentation continues at 8:00
Cost:	$22 for IEEE members; $25 for non-members
Place:	Marie Callender's Restaurant (Garden Room); 2090 Diamond Blvd in Concord near the Concord Hilton Hotel
RSVP:	by October 12, by email to Gregg Boltz at gboltz@brwncald.com or call (925) 210-2571
Web:	www.e-grid.net/docs/0510-oeb-ias.pdf

Gary H. Fox received his BSEE from California Polytechnic State University, San Luis Obispo in 1978. He became a Member of IEEE in 1989, and a Senior Member in 2001. He has been employed by General Electric Company for 27 years. His current assignment is a Systems Engineer for GE Industrial in Concord, providing application and technical support for power distribution and control equipment. Mr. Fox is a member of the IEEE Industry Applications and IEEE Power Engineering Societies. He has held several IEEE officer positions including Chair for the San Francisco Chapter, IAS; Chair, San Francisco Section; and Chair, San Francisco Bay Area Council. In addition, he has lectured at several local IEEE workshops covering the subjects of high voltage substation design, short circuit calculations, and power system protection. He has been a Professional Engineer licensed in California since 1982.

The October IAS meeting features a talk entitled "AC Control Power and Digital Protective Relays: Avoiding the Pitfalls." The speaker will be Gary H. Fox, P.E., Systems Engineer with GE Industrial.

Batteries are considered to be the most reliable control power source used in medium voltage switchgear. But applying batteries can cause headaches for the design professional, or owners simply don't like the amount of space they use up. So ac control power is often used as an alternative. This would be fine if we were still using electromechanical relays for protection. But digital relays have become the default choice for protection on modern switchgear and most digital relays require a separate control power source for their operation. If that control power is an ac source derived from the primary circuits, the voltage to the protective relays cannot be considered to be reliable and compromises the protection of the circuit. At this chapter meeting, an IEEE paper originally presented at the 2005 IAS Pulp and Paper Industry Conference will be discussed that explores the issues surrounding ac control power, and techniques that can be applied to mitigate those issues.

THURSDAY OCTOBER 13

The CloudSat Experimental Satellite 94 GHz High-Efficiency Radar Antenna

Speaker: Prof. Aluizio Prata, Jr, University of Southern California
Time: Social at 6:00 PM; Presentation at 6:30 PM
Cost: none
Place: SC12-Auditorium, Intel Corp., 3600 Juliette Lane, Santa Clara
RSVP: not required
Web: www.e-grid.net/docs/0510-scv-mtt.pdf

CloudSat is a NASA experimental satellite that will use a 94 GHz 1.5 KW pulsed radar to measure the vertical structure and properties of clouds from space. Launch is currently planned for the end of September from Vandenberg AFB in California, where the spacecraft is already located. Among the several technological advances carried aboard CloudSat, there is a large 94 GHz shaped offset high-efficiency tri-reflector antenna that was designed and measured at the Jet Propulsion Laboratory. This presentation will discuss this antenna from the perspective of its electrical designer. The talk is geared to an engineering audience that is not necessarily overly familiar with reflector-antenna design.

Dr. Aluizio Prata, Jr. was born on 18 March, 1954 in Uberaba, Brazil. He received his Ph.D. from the University of Southern California, in 1990 and holds an M.S.E.E. degree from the California Institute of Technology, 1984. Currently he is an Associate Professor at the University of Southern California, working with applied electromagnetics. Dr. Prata is co-author of the widely used PC interactive reflector-antenna design software RASCAL, currently with more than 1000 free copies distributed worldwide. He has been a consultant for numerous aerospace companies, and has authored or co-authored over eighty articles, patents, and symposium papers.

Dr. Prata was a member of the steering committee of the 1995 IEEE Antennas and Propagation Society (APS) International Symposium, was the 1996 Chair of the Los Angeles Chapter of the IEEE APS (the Chapter won the 1996 Best Worldwide Chapter Award), was the Vice Chair of the 2000 IEEE International Conference on Phased Array Systems and Technology, and is the Technical Program Chair for the 2008 IEEE Antennas and Propagation Society (APS) International Symposium.

CloudSat antenna and Dr. Prata

SCV MAGNETICS

THURSDAY OCTOBER 18

A Process View of Recording Head Technology

Speaker: Rick Dill,
Hitachi Global Storage Technology
Time: Cookies & Conversation at 7:30 PM,
Presentation at 8:00 PM
Cost: none
Place: KOMAG, 1710 Automation Parkway,
San Jose
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/mag/

Since 1958, when he joined IBM Research Division then in Poughkeepsie NY, **Frederick (Rick) Dill,** the inaugural recipient of the IEEE Jun-ichi Nishizawa Medal, has done seminal work in a remarkable range of fields. Dr. Dill's early achievements include essential contributions to semiconductor lasers, and to building high-speed integrated circuits using germanium. In the 1970s he spearheaded research that led to pioneering process models and materials characterization for photolithography, transforming device lithography from an art to an engineering science. His papers are still referenced today; the parameters used to describe photoresist exposure are called "The Dill Parameters." In the 1980s Dr. Dill was lead inventor of the video RAM, and he currently works on disk drive recording heads to improve disk drive capacity. Today's disk drive heads are built with processes he pioneered. An IEEE Life Fellow, Dr. Dill has served on the IEEE Board of Directors, as president of the IEEE Electron Devices Society, and on the society's Administrative Committee. He helped establish several IEEE journals including the IEEE Journal of Technology Computer Aided Design, the first all-electronic journal. Dr. Dill was inaugurated into the National Academy of Engineers in 1990, and he subsequently chaired the Academy's Engineering Electronics Engineering section. Dr. Dill was also one of the early president's of IBM's Academy of Technology. A recipient of the IEEE Centennial Medal and the IEEE Third Millennium Medal, Dr. Dill has more than 30 patents, including fundamental patents on automated tools for thin film measurements. IBM promoted him to Distinguished Engineer in 2002. He joined Hitachi Global Storage Technologies in 2003 following IBM's sale of the disk drive business, where he is now executive engineer solving manufacturing process problems.

The technologies used to make recording heads have a strong linkage to those used for VLSI. There are differences, of course, because people working with silicon give no thought to the spin of electrons and many of the materials used in magnetics are exquisitely difficult to pattern into ever smaller sizes. The author first worked on thin film recording heads in the 1970 era when he did the layout and produced masks for the first thin film inductive heads of Dave Thompson and Luby Romankiw. Then dimensions were in 20's of microns, although lithographic capability even then was about two microns. This talk will look at some elements of processing from then to present day. A decade ago, a glimpse into building recording heads showed the technology in trouble. In defining a 3 micron pole tip there was 12 microns of topography present and the critical feature was placed roughly five microns above the base plane. A little lithographic modeling showed that this was possible (agreeing with the fact that it was being achieved in manufacturing), but also showed that one could never get to one micron pole tip dimensions without reducing the topography. This lead to a project developing alumina fill and CMP planarization to allow critical lithography to be done on a flat surface. This has enabled us to reduce minimum feature size to the 100 nm range in just a decade. There is a constant need to either push our technologies another increment or to define new processes when the existing ones run out of steam. This isn't an easy or welcome task as everyone hopes to use the current technology for another generation. Process innovation is seldom welcomed until the need is desperate. Since process people seldom talk about what they are currently doing, this talk will be no exception. Instead I will talk about the kinds of issues dealt with in process evolution and innovation and the surprises that arise from innovative approaches. There are many lessons to be learned, particularly when you use materials and processes in new ways.

WEDNESDAY OCTOBER 19

Neural Basis of Reach Preparation and Communication Prosthetics

Speaker: Krishna Shenoy, Department of EE & Neurosciences Program, Stanford University
Time: optional dinner with the speaker in the Stanford Hospital cafeteria at 6:15 PM (no reservation needed). Formal meeting is 7:30 PM
Cost: none
Place: Clark Center Auditorium (South-West end of the Stanford Hospital and Medical School); see map on website
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/embs/

Professor Krishna Shenoy heads the Neural Prosthetic Systems Laboratory at Stanford University. His research group conducts neuroscience (systems & cognitive neuroscience) and neuroengineering (electrical, bio, and biomedical engineering) research. The group investigates the neural basis of sensorimotor integration and coordination, and designs neural prosthetic systems to assist disabled patients. Professor Shenoy teaches EE101B Circuits II and EE418 Topics in Neuroengineering.

Professor Shenoy received the B.S. degree in Electrical Engineering from the University of California at Irvine in 1990 (Summa Cum Laude), the S.M. degree in Electrical Engineering from MIT in 1992, and the Ph.D. degree in Electrical Engineering from MIT in 1995. He was a postdoctoral fellow in the Division of Biology at Caltech from 1995-2001. In 2001 Professor Shenoy joined the Department of Electrical Engineering at Stanford University, where he is also a member of the Neurosciences Program (School of Medicine) and is affiliated with Stanford's Bio-X Program, Biodesign Program, and NIS (Neurosciences Institute at Stanford). Honors and awards include NSF and Hertz Foundation graduate fellowships, the 1996 Hertz Foundation Doctoral Thesis Prize, an NIH postdoctoral fellowship, a Burroughs Wellcome Fund Career Award in the Biomedical Sciences, the William George Hoover Faculty Scholar in Electrical Engineering at Stanford University, the Robert N. Noyce Family Scholar in the Stanford University School of Engineering, an Alfred P. Sloan Research Fellowship, and Defense Sciences Research Council (DSRC/DARPA) fellow and member. Dr. Shenoy is a member of the IEEE (Engineering in Medicine and Biology Society, EMBS), Eta Kappa Nu, Tau Beta Pi, Society for Neuroscience and Neural Control of Movement Society.

Our seemingly effortless ability to reach out and swat a fly or grab a cup belies the sophisticated neural computations at work in our nervous system. It has long been recognized that, before moving, we somehow prepare neural activity such that, when called upon, the desired movement unfolds. But the goals of movement preparation and the underlying neural mechanisms remain poorly understood. I will describe our recent electrophysiological investigations of how cerebral (pre-motor) cortex prepares and helps execute movements. Our results suggest that the brain is attempting to optimize preparatory neural activity and can delay movement until this activity is sufficiently accurate.

With an increased understanding of movement planning, it is also possible to design real-time electronic systems capable of translating neural plans into prosthetic movements. I will also describe our recent electrophysiological investigations aimed at establishing the fundamental, neurobiologically dictated performance limits of communication prostheses. Our results suggest that at least a factor of four performance improvement is possible, which is essential for starting to assess the potential benefits of clinical cortically-controlled prosthetic systems.

SCV SOLID STATE CIRCUITS

THURSDAY OCTOBER 20

A Single-Chip Quad-Band GSM/GPRS Transceiver in 0.18um Standard CMOS

Speaker: Julian Tham Vice President, IC Design Engineering, Berkana Wireless
Time: Refreshments at 6:30 PM; Presentation at 7:30 PM
Cost: donation for food costs
Place: Cadence Building 5, 2655 Seely Ave, San Jose
RSVP: not required
Web: www.ieee.org/scv/ssc

J.L. Julian Tham is currently with Berkana Wireless where he is the Vice President of Engineering, RF and Mixed Signal Design. He has been instrumental in helping to bring Berkana's family of RF CMOS Transceivers to production. Mr. Tham holds 11 patents and is recognized as an industry authority on wireless transceiver architectures for applications including 900MHz DSS, WLAN 802.11b/g/a and multiband cellular RFIC chipsets. The products he designed and developed have resulted in cumulative revenue in excess of $350 million.

A 0.18um CMOS single-chip fully integrated quad-band GSM/GPRS transceiver is presented. The low-IF receive section achieves -110dBm sensitivity at the antenna and -15dBm IIP3. The offset PLL transmitter achieves 1.2 degrees RMS phase error, -65dBc modulation level at 400kHz offset, and -165dBc/Hz output noise level at 20MHz offset. The chip draws 95uA and 112mA respectively in receive and transmit modes.

THURSDAY OCTOBER 27

Drop-Testing of Components in Portable Applications

Speaker: Dr. Luu Nguyen, National Semiconductor
Time: buffet lunch at 11:45 AM; presentation at 12:15 PM
Cost: $15 if reserved by Oct. 23; $20 at the door
Place: Ramada Inn, 1217 Wildwood Ave (Fwy 101 frontage road, between Lawrence Expy and Great America Pkwy), Sunnyvale
RSVP: Please reserve and pay in advance using our PayPal on-line system or email John Jackson at john.jackson@analog.com
Web: www.cpmt.org/scv/

Dr. L. T. Nguyen is a Senior Engineering Manager in the Package Technology Group at National Semiconductor Corp, working on various aspects of wafer-level packaging, lead-free and halogen-free, thermal measurement and modeling, and design-for-manufacturability. He co-edited two books on packaging, and has over 190 publications. He has over 50 patents and invention disclosures. He is a Fellow of IEEE and ASME, and a Fulbright Scholar (Finland 2002). He is currently an Associate Editor for the CPMT Transactions on Advanced Packaging and a Guest Editor for the CPMT Transactions on Components and Packaging Technologies. He received two Best of Conference Awards (27th IEMT 2002 and InterPack 2005) and eight IMAPS and IEMT Best of Session Conference Awards. Other awards include the 2003 Mahboob Khan Outstanding Mentor Award from the Semiconductor Research Corporation in recognition of contributions to student mentoring, research collaboration, and technology transfer, and the 2004 IEEE CPMT Society's Outstanding Sustained Technical Contributions Award.

Portable devices such as cell phones and PDAs are more likely to be dropped than affected by changes in thermal conditions. As a result, current reliability research has shifted from studying the effects of typical thermomechanical cycling to mechanical shock. Technical challenges arise from the complexity of lead-free solder metallurgies, printed wiring board finishes, and component metalizations.

Earlier studies have shown that intermetallic layers between lead-free solders and component metalizations are prone to fail in drop tests. Reactions between Ni(P)/Au coated pads on PWBs and solder alloys have been studied extensively. However, much less is known about the effects of component UBM (Under Bump Metalization) with different finishes and pad structures on lead-free and tin-lead assemblies under shock loading.

This talk will discuss the behavior of two UBMs used in wafer level chip scale packages on drop test performance, namely, (Al)Ni(V)/Cu metalization and electroless Ni(P)/Au metalization. A significant difference in the reliability performance of the components was observed: those with (Al)Ni(V)/Cu UBM were more reliable than those with electroless Ni(P)/Au UBM, regardless of the solder bump type, the solder paste, the surface finish of the boards, or the pad structure on the boards. The primary failure mode in the component side is the cracking of the interconnections along a brittle NiSnP layer between the electroless Ni(P) of high P-content and the solder alloy. Components with (Al)Ni(V)/Cu, on the other hand, fail by cracking along the [Cu,Ni]6Sn5 layer. On the board side, cracking happens in the porous NiSnP layer formed between the electroless Ni(P) metalization and the [Cu,Ni]6Sn5 intermetallic layer. Cracking happens predominantly on the component side due to three factors:

- high stresses on the component side;
- brittleness of the reaction layers; and,
- strain-rate hardening of the solder interconnections.

It will be shown that such failure mode differs from that typically observed in thermally cycled devices, where the nucleation and propagation of cracks are strongly enhanced by the recrystallization of the solder interconnects.

SCV Instrumentation and Measurement

WEDNESDAY NOVEMBER 2

Blackfin: A Combined RISC/Signal Processing Architecture for a New Era

Speaker: Tim Wilkerson, Analog Devices
Time: Networking at 7:30 PM, Presentation at 8:00 PM
Cost: none
Place: Cogswell College, Room 197, 1175 Bordeaux Drive, Sunnyvale
RSVP: Please reserve by email with David Rivkin, david.rivkin@ieee.org
Web: www.ewh.ieee.org/r6/scv/ims/

The presentation describes the salient architectural features of the Blackfin Processor from Analog Devices as well as some of the larger applications areas. Multiple single core and dual core proliferations of the blackfin family are described as well as peripheral mix, and benchmark information showing strengths of the architecture as well as unique capabilities in such application areas as multimedia, networking, automotive and instrumentation. In addition, some C level compiler strategies are briefly described which are applicable to Blackfin.

- ARM's **Tiger** microarchitecture
- IBM's **CELL** for **PlayStation 3**
- IBM's **PowerPC** in MS **XBox 360**
- P.A. Semi's first uP by former designers of Alpha and SiByte
- StarCore and TI's sophisticated new **DSP cores** and chips

CONFERENCE CALENDAR

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www.e-grid.net/docs/conf-flyer.pdf

Oct 24-27:

FPF'05 Fall Processor Forum: The Road to Multicore

- San Jose DoubleTree Hotel
- Keynotes & Sessions: Tues–Wed, October 25-26
- Full-day Seminars: Mon & Thurs, October 24 & 27

Integrating two or more processor cores on a single chip is the hottest trend in high-performance microprocessor design. FPF 2005 focuses on multicore processors, including new product introductions and other dimensions of multicore processing..

See Page 4 for more details

Oct 24-27:

GSPx: Pervasive Signal Processing Conference and Expo

- Santa Clara Convention Center
- Workshops: Monday, October 24
- Sessions & Expo: Tuesday – Thursday

This major event focuses on embedded signal processing and the myriad of applications that the technology is spawning.
Note that there are substantial GRID & Early-bird discounts through September 15th.

See www.e-grid.net/conf/gspx.html for more details

Nov. 6-10 – ISTFA'05:

Int'l Symposium on Testing and Failure Analysis

- Technical Sessions, Panel Discussions, Tutorials
- Exposition: Tuesday-Wednesday, Nov 8-9

Held this year for the first time at the San Jose Convention Center, ISTFA'05 combines technical sessions, tutorials, an exhibition, and user group meetings with a focus on making the full experience a strong benefit for the attendee. The limited number of selected, high-quality papers only requires two tracks throughout the program, for good access.

See Page 5 for more details