Chapter Meetings and Events

SCV-LEOS - 11/1 | **Solid State Light Sources -** Addressing the barriers that limit their application to general illumination ... [more]

SCV-IM - 11/2 | **Blackfin: A Combined RISC/Signal Processing Architecture for a New Era** - embedded processor for audio, video, and communications applications ... [more]

SCV-Mag - 11/3 | **Toggle MRAM Performance and Outlook** - magnetoresistive random access memory integrated with silicon-based microelectronics ... [more]

SCV-EMC - 11/8 | **BPL Emissions Compliance Guidelines** - controversy has surrounded the deployment and testing, requiring means for assessing compliance and mitigating interference ... [more]

SCV-CPMT - 11/9 | **Carbon Nanotubes: Enhancing Conductivity of Conductive Plastics** - better interconnect materials, thermal spreaders, and even sensors and display structures ... [more]

SCV-EDS - 11/7 | **A Survey of Semiconductor Devices** - from the old and sometimes obsolete types to the recent quantum-well devices, organized into groups ... [more]

SCV-GOLD - 11/9 | **Challenges and Innovations for Development of SOCs** - for everyone, but especially those in the first decade of their careers ... [more]

SCV-MTT - 11/10 | **On the Use of Artificial Intelligence in Microwave Hardware Design** - use of Artificial Intelligence Optimizer ("AIO") antenna design software for real-time optimal solutions ... [more]

SCV-Nano - 11/15 | **Nanotech: Imagine the Opportunities** - half-day symposium showcasing university graduate research ... [more]

SCV-EMB-11/16 | **High Frequency Ultrasound Imaging of the Anterior Segment of the Eye** - in-vivo intra-operative visualization of the Schlemm's canal for diagnosis and surgical guidance ... [more]

OEB-IAS - 11/17 | **Arc Flash Studies using Electrical Engineering Software** - a focus on how to perform an arc flash study using electrical engineering software ... [more]

SCV-SSC - 11/17 | **PLL History: A Personal Viewpoint** - from the extremely narrow-band systems of years ago to the wide-band applications of today ... [more]

SCV-CAS - 11/21 | **A Digital Clock and Data Recovery Architecture for Multi-Gigabit/s Binary Links** - a general architecture and a small-signal model ... [more]

SCV-CE - 11/29 | **Distributed HD IPTV and Audio over Powerline** - no new wires and it works throughout the whole house ... [more]

Upcoming Conferences in the Bay Area

Nov 6-10: **ISTFA: Int'l Symposium on Testing and Failure Analysis**, at San Jose Convention Center; Workshops, Sessions, User-Group meetings [more]

Mar 6-8: **Internationalization and Unicode Conference** Hyatt Regency Hotel, Burlingame [more]

Calls for Papers – Spring Conferences

Society for Information Display International Symposium, Seminar, & Exhibition [more]
- Paper Summary Deadline: **December 1**, 2005
- Location & Dates: San Francisco, June 11-13, 2006

IEEE Radio Frequency Integrated Circuits Symposium [more]
- Paper Summary Deadline: **January 2**, 2006
- Location & Dates: San Francisco, June 11-13, 2006

Professional Skills Courses from EMS, CPMT, ETA:

Finance for Non-Finance Professionals
Nov 1 at Cypress Semiconductor, San Jose [more]

Clear Business, Technical, and E-mail Writing
November 3 in Santa Clara [more]

Transitioning from Individual Contributor to Manager
November 8 in Dublin [more]

Presentation Skills for Engineers
- November 18 in San Jose [more]

Getting Things Done Across Organizational Borders
- November 30 in San Jose [more]

Short Courses from SVTI, San Jose:

Innovation and Creativity for High Tech Professionals
Nov. 3-4 [more]

Power Management for ICs with Focus on Linear Drop Out (LDO) Regulators Nov. 11 [more]

The Dynamic Leader's Toolbox & Applications For Management in the 21st Century Dec. 1-2 [more]

Support our advertisers

IEEE GRID

Your Networking Partner®

November 2005 • *Volume 52 • Number 11*

IEEE-SFBAC
PO Box 2110
Cupertino, CA 95015-2110

IEEE **GRID** is the monthly newsmagazine of the San Francisco Bay Area Council of the Institute of Electrical and Electronics Engineers, Inc. As a medium for both news and opinion, the editorial objectives of IEEE **GRID** are to inform readers in a timely and objective manner of newsworthy IEEE activities taking place in and around the Bay Area; to publish the official calendar of events; to report on IEEE activities of a national and international scope; and to serve as a forum for comment on areas of concern to the engineering community by publishing contributed articles, invited editorials and letters to the editor.

IEEE GRID is published as the **GRID** Online Edition residing at www.e-GRID.net, and in a handly printable **GRID.pdf** edition, and also as the **e-GRID** sent by email twice each month to more than 24,000 Bay Area members and other professionals.

Editor: Paul Wesling
IEEE **GRID**
12250 Saraglen Dr.
Saratoga CA 95070
Tel: 408 331-0114 / 510 500-0106 /
415 367-7323

Fax: 408 904-6997
Email: editor@e-grid.net
www.e-GRID.net

From the editor . . .

Getting well-known in your field is a great way to increase your networking reach – and remember, it's networking that is the key component in career vitality these days. There are a number of benefits in preparing and delivering a paper at a conference.

First, the discipline of researching and writing a paper is good for your analytical abilities and writing skills. If your abstract about your recent work is accepted by the conference, you'll need to do a literature search for prior art, then write up what you did and what you learned. The objective is to give the listener/reader enough information that they can avoid any problems you found and understand the implications of your work on their own work.

But there are several other benefits that aren't directly related to the paper itself. First, you are required to attend the conference itself, which gives you a great chance to rub elbows with other practitioners in your field. You might get a chance to talk with a keynote speaker, an executive of a company in your field, or academic staff working on advanced developments. All of these can help you in your work – and also set up contacts that may prove valuable in future years. Secondly, your name is now in print – six months following the conference, type your name into Google and see this paper pop up. It never hurts to list a few papers on your resume, should you find yourself looking for a job at some point.

There are two Calls for Papers in the current issue of the GRID.pdf: one for the Information Display Symposium, and the other for the RF Integrated Circuits Symposium – both happen to be the same week in June, but someone interested in one probably wouldn't attend the other. And last month we published the CFP for the International Symposium on Quality Electronic Design. Any of these (and lots of others) would be good choices.

Paul Wesling **editor@e-grid.net**

NOTE: This PDF version of the IEEE GRID – the **GRID.pdf** – is a monthly publication and is issued a few days before the first of the month. It is not updated after that. Please refer to the Online edition and Interactive Calendar for the latest information: **www.e-GRID.net**

Professional Services Marketplace – editor@e-GRID.net for information

Say you found them in our GRID MARKETPLACE

TEA

Device Thermal Characterization
Package Thermal Characterization
Thermal Test Boards
Thermal Test Equipment & Fixtures

Bernie Siegal

Thermal Engineering Associates, Inc.

650-961-5900

info@thermengr.com www.thermengr.com

SHAX Engineering and Systems

Electronics Design Services

- Analog and Digital circuit design
- VHDL/Verilog coding and synthesis
- ASIC/FPGA from concept to production

(650) 966-1835

ishakour@shax-eng.com www.shax-eng.com

Digital Chip Design Services

ASIC Design • EDA Evaluation • Verilog HDL • Synthesis • Design for Visibility • Timing • Scan • Verification • Low Power techniques • Power Analysis • BIST • DFT • ATPG • Silicon Debug

Testable logic for high-volume production with low DPM

Contact Mahesh Siddappa

ME (CS, India), MS (EE, SUNY at Stony Brook)

m.siddappa@ieee.org 408-981-6612

OZEN ENGINEERING, INC.

ANSYS Channel Partner

- Multiphysics, Multidisciplinary Engng
- CFD, Stress, Heat Transfer, Fracture
- Fatigue, Creep, Electromagnetics
- Dynamics, Design Optimization
- Linear/Nonlinear Finite Element Analyses

Ozen Engineering (408) 732-4665

info@ozeninc.com www.ozeninc.com

Mixed-Signal IC Development

- From Inception to Production Transfer
- Turnkey, Design Services & Consulting
- Design Reviews & TroubleShooting

Mixel, Inc.

Excellence in Mixed Signal Design

(408) 274-2736

sales@mixl.com www.mixl.com

OPS ALACARTE™

(408) 472-3889
info@opsalacarte.com
www.opsalacarte.com

Professional Consulting Services to assist clients in developing and executing any elements of Reliability throughout the Organization and Product Life Cycle.

•Goal Setting • MTBF Predictions • HALT • HASS/ESS
•Assessments • FMECA • DVT/V&V • EOL Assessment
•Program Plans • DoE • Rel Demos • Training/teaching
•Gap Analysis • CAPA/CLCA • Life Tests ...and more

OPS ALACARTE pioneered Reliability Integration℠ – using multiple tools together to increase the power and value of any Reliability Program.

Board Logic Systems

Complete Product Solutions Provider ™

Experienced consultants in the fields of:

- Board & Verilog Design • Debug and Test
- Signal Integrity • EMI
- Power Electronics • Layout
- Software Development • Documentation

www.boardlogics.com

info@boardlogics.com (650) 867-0869

Patent Agent

Jay Chesavage, PE
MSEE Stanford
3833 Middlefield Road, Palo Alto 94303

info@file-ee-patents.com

www.File-EE-Patents.com

TEL: 650-619-5270 FAX: 650-494-3835

GRID.*pdf*
e-GRID

Do you provide a service?
Would you like more inquiries?

- Access 25,000 engineers and managers
- IEEE Members across the Bay Area
- Monthly and Annual Rates available

Visit our Marketplace (page 3)

Download Rates and Services information:
www.e-grid.net/docs/marketplace-flyer.pdf

31st International Symposium for Testing and Failure Analysis

November 6-10, 2005 • San Jose, CA USA

Exposition: Tuesday-Wednesday, Nov 8-9

Held this year for the first time at the San Jose Convention Center, ISTFA'05 combines technical sessions, tutorials, an exhibition, and user group meetings with a focus on making the full experience a strong benefit for the attendee. The limited number of selected, high-quality papers only requires two tracks throughout the program, for good access.

Technical Sessions:

• Die Level Fault Isolation • Package Level Analysis
• System Level Analysis • Advanced Techniques
• Optical Techniques • Optoelectronic Devices
• Failure Analysis Process • Circuit Edit for FA, FI, and Debug • Case Histories • SPM Techniques
• Sample Preparation • Nanotechnology Analysis
• Yield Enhancement • Discretes, Passives, and MEMS • Metrology and Materials Analysis • Test
• plus Poster Papers

Panel Discussions:

- Strategic Development in FA. What Can We Get From Other Technical Sources?
- Can Competitors Build Some Common FA Facilities To Improve ROI And Efficiency?

Tutorials:

• Failure Analysis Basics • Device and Packaging
• Microscopy Tools • Yield • Sample Preparation
• Fault Isolation • MEMS • Failure Mechanisms
• Failure Analysis Laboratory Management

.... plus **User Group meetings** on Tuesday and Wednesday evenings, to provide a convenient forum for users of a specific technique to meet, share ideas, and discuss relevant issues in a non-commercial environment. Planned topics this year:

- Scanning Optical Microscopy (SOM)
- Scanning Probe Microscopy (SPM)
- Focused Ion Beam (FIB)
- Chip Access/Delayering
- Nano Probe

Luncheon Address:

Dr. Johannes Stork, Senior Vice President and Chief Technology Officer, Texas Instruments

As Director of the Silicon Technology Development organization, Dr. Stork's primary responsibilities are the development of advanced CMOS, packaging and mixed signal process technologies.

ISTFA is the best venue for learning new failure analysis techniques, challenges and directions. It also provides ample opportunities for you to participate and network through the question-and-answer periods, the user groups, the panel discussions, the exhibition, and the networking poster luncheon.

Additional information is on the ISTFA web site:

www.ISTFA.org CLICK!

- Online conference registration begins Sept. 15th. Download the registration form at:

  www.e-grid.net/conf/istfa-reg.pdf

- Discounted fees for EDFAS and ASM Members. Non-Members of EDFAS receive a full year's membership with their registration.

Tutorials-only and Exhibits-only registrations are available. To exhibit at ISTFA, please contact **Mr. Charles Dec:**

charles.dec@asminternational.org

EDFAS General Membership Meeting

Tuesday, November 8, 4:40-5:30 pm

The **E**lectronic **D**evice **F**ailure **A**nalysis **S**ociety (EDFAS) will hold its annual General Membership Meeting on Tuesday at ISTFA. It is open to all current members, as well as interested prospective members.

2006 IEEE Radio Frequency Integrated Circuits Symposium
San Francisco, California
June 11-13, 2006

RFIC-2006 Call for Papers

The **2006 IEEE Radio Frequency Integrated Circuits Symposium (RFIC-2006)** will be held in San Francisco, California on June 11-13, 2006. For the latest information, visit: **www.rfic2006.org**

Electronic Paper Submission/Communication: Technical papers must be submitted in an electronic form via the RFIC-2006 web site **www.rfic2006.org** - **Hard Copies are not accepted.**

Technical Areas: Papers are solicited describing original work in RFIC design, system engineering, system simulation, design methodology, RFIC circuits, fabrication, testing and packaging to support RF applications in areas such as, but not limited to:

- **Cellular System IC's and Architectures:** GSM, EDGE, TDMA, CDMA, 3G, WCDMA, GPS
- **Wireless Data System IC's and Architectures:** WLAN, Bluetooth, 802.1x, Telemetry, RFID
- **Wide Band Communication System IC's and Architectures:** UWB, MMDS, CATV, TV Tuners
- **Optical System IC's and Architectures:** OC-48, OC-192, OC-768, Gigabit Transceivers
- **Small-Signal Circuits:** LNA's, Mixer's, VGA's, Active Filters, Modulators
- **Large-Signal Circuits:** Power Amplifiers, Drivers, Advanced TX circuits
- **Frequency Generation Circuits:** VCO's, PLL's, Synthesizers
- **RFIC & Device Technology:** IC Technologies, Packaging, Modules, RF Test & Characterization
- **RFIC Modeling and CAD:** Device and behavioral modeling, Design Methodology

Technical Format: The technical sessions will be held for three days from Sunday through Tuesday. Workshops will be on Sunday. Several invited sessions and talks will take place during the conference.

Microwave Week 2006: The RFIC 2006 will be in conjunction with the IEEE MTT-S International Microwave Symposium (IMS). Microwave Week 2006 will continue with the International Microwave Symposium and Exhibition, and the Microwave Historical Exhibit.

Electronic Submission Deadlines

Technical Paper Summaries in PDF format:	**2 January 2006**
Final Manuscripts for the Digest and CD-ROM:	**6 March 2006**
All submissions must be made through the RFIC2006 portal:	**www.rfic2006.org**
ALL SUBMISSIONS MUST BE IN PDF FORM	**Hard copies not accepted**

Sponsored by the
IEEE MTT-S, EDS, and SSCS
www.rfic2006.org

CALL FOR PAPERS

Society for Information Display

INTERNATIONAL SYMPOSIUM, SEMINAR & EXHIBITION

JUNE 4-9, 2006

MOSCONE CENTER, SAN FRANCISCO

Submission Deadline: Dec. 1, 2005

The Society for Information Display encourages the submission of original papers on all aspects of research, engineering, application, evaluation, and utilization of displays for **SID '06**. An abstract and technical summary are solicited in the following broad areas:

Active-Matrix Devices: Advances in the innovative development & implementation of active-matrix electronics into displays.
Applications: Unique & innovative applications of display technologies in consumer, industrial, commercial, and military fields.
Applied Vision/Human Factors: All aspects of vision, perception, and human factors for design, image quality, and usability.
Display Electronics: Circuits for displays, circuits-related image-processing algorithms, and electronic components.
Display Manufacturing: All aspects of display manufacturing.
Display Measurement: Characterization and measurements of displays and display components.
Display Systems: Novel integration of displays into specialized devices, as well as systems-level aspects of electronic displays.
Emissive Displays: New developments in emissive displays such as PDPs, inorganic EL, and advances in materials, phosphors, etc.
FEDs and CRTs: Design and design methods utilized in cathode-ray tubes and FEDs, their components, and materials.
Organic Light-Emitting Diodes: All aspects of organic light-emitting-diode displays, both small molecule and polymer types.

SID '06 will have 250^{+} exhibitors and 7,500^{+} attendees – display scientists, engineers, manufacturers, entrepreneurs, marketers and end-users.

Projection Displays: Projection-display systems, key components, and materials used in applications such as consumer television, game systems, electronic cinema, computer desktop monitors, business presentations and training, commercial and military simulation, and medical imaging.
Liquid-Crystal and Other Non-Emissive Displays: Advances in the development of liquid-crystal materials, electro-optical effects, and devices, including materials development in other non-emissive display technologies.

For **complete information** on SID '06 topics, abstract preparation, and other details, please see:

Call for Papers: **www.e-grid.net/docs/sid.pdf**

The SID'06 website: **www.sid2006.org** CLICK!

Authors will be notified by Jan 20; full papers are due Mar 3, 2006

UNIVERSITY OF CALIFORNIA, SANTA CRUZ

COMPUTER ENGINEERING

Assistant and Associate Professor

The Computer Engineering Department, UC Santa Cruz, invites applications for **two faculty positions**.

Position #488: Tenure track (Assistant Professor): applicants whose research interests are in the area of Assistive Technology including sensory augmentation, human-machine interface, wearable computers, prosthetic devices, and technology for the elderly and the disabled.

Position #63/63T: Tenure track (Assistant Professor) or tenured (Associate Professor): applicants in Computer System Design, including VLSI design, FPGA design, VLSI CAD, system-on-a-chip design, and related areas.

The campus is especially interested in candidates who can contribute to the diversity and excellence of the academic community through research, teaching, and service. UCSC is the UC campus nearest to Silicon Valley and has close research ties with this local industry. Submit: CV, statement of research and teaching plans, URLs of selected reprints, and ensure that at least 3 confidential letters of recommendation are sent directly to the search committee by **Jan. 2, 2006**. We prefer electronic applications: www.soe.ucsc.edu/jobs/faculty/apply. All letters will be treated as confidential documents (www2.ucsc.edu/ahr/policies/confstm.htm). Alternatively, applications may be mailed to: Computer Engineering Search Committee, University of California, 1156 High Street MS: SOE3, Santa Cruz, CA 95064.

Clearly indicate position: #488 (Assistant Professor, Assistive Technology), #63 (Assistant Professor, Computer System Design) or #63T (Associate Professor, Computer System Design).

For further details about the Baskin School of Engineering at UCSC, see www.soe.ucsc.edu

Internationalization & Unicode Conference 29

March 6-8, 2006
Hyatt Regency Hotel
Burlingame
(S.F. Airport)
Tutorials 3/6; Sessions 3/7-8

If you are involved in implementing the Unicode Standard or working on internationalization, this is a must-attend conference – the only industry event focused on the Unicode™ Standard. The conference features a variety of tutorials and conference sessions that cover current topics related to Unicode, the web, software and internationalization. Unicode experts, implementers, clients and vendors are invited to attend this unique conference. Exchange ideas with leading experts, find out about the needs of potential clients, or get information about new and existing Unicode-enabled products.

Visit the website to sign up for email updates about Unicode'06 and its tutorials and sessions.

Organized by the Object Management Group, a not-for-profit consortium that produces and maintains computer industry specifications for interoperable enterprise applications, including MDA®, UML®, CORBA®, MOF™, XMI® and CWM™.

Conference topics:

- Web internationalization
- Text and data mining
- Security and phishing
- New and upcoming technologies
- Enterprise software in a global environment
- Web services, SOA and Internationalization
- Language tags and locales: implications for developers
- Making scripts and languages accessible
- Global development best practices
- What's new with Unicode 4.0; Successful Implementations
- Internationalized Domain Names/Resource Identifiers
- Tips, tricks and traps in developing international software
- Globalizing your product: business cases and technical issues

Early-bird registration rates through January 23 – multi-attendee discounts. For more information and to register:

www.unicodeconference.org/ieee

For information on exhibiting or other questions, visit the website or contact Kevin Loughry at loughry@omg.org, +1-781-444 0404

The Unicode Consortium is a non-profit organization founded to develop, extend and promote use of the Unicode Standard and related globalization standards.

SCV Lasers and ElectroOptics

TUESDAY NOVEMBER 1

Solid State Light Sources: Addressing the Barriers that Limit Their Application to General Illumination

Speaker: Steve Johnson, Lawrence Berkeley Laboratories
Time: Pizza Social at 7:00 PM, Presentation at 8:00 PM
Cost: none
Place: National Semiconductor Credit Union, 955 Kifer Road, Sunnyvale
RSVP: Please reserve by email to rsvp-scv-leos@ieee.org
Web: www.ewh.ieee.org/r6/scv/leos/

Dr. Steve Johnson is Group Leader for the Lighting Research Group at Lawrence Berkeley National Laboratory in Berkeley, California. The Lighting Research Group performs research into light sources and ballasts, lighting controls, light distribution systems, and human factors. Research at LBNL is principally focused on technologies that will improve the efficiency of current practice for both residential and commercial applications of lighting. Since joining LBNL in 1996, Dr. Johnson has shifted! the emphasis in light source development at the laboratory from discharge lamps to solid state devices. He directs research in the area of both LEDs and OLEDs. Prior to joining LBNL, Dr. Johnson that spent 20 years working in the lighting industry.

The potential of LEDs and OLEDs as light sources for general illumination will be discussed relative the technical barriers that must be overcome before these sources can replace the ubiquitous incandescent and fluorescent light sources we use daily. Of the two sources, LEDs have the greatest near term opportunity, hence the presentation will focus more on this source. The discussion will start at the LED die level and progress through the development of a lighting system, addressing the issues of extraction efficiency, thermal management and optical control. LEDs are a wonderful point source for lighting applications, where OLEDs are a much larger diffuse source. This major difference in optical performance makes the two technologies complementary rather than competitive. OLEDs are being aggressively developed for the display market and it is expected this will have! a synergistic effect in speeding their development as a light source. The technical barriers for OLEDs of lifetime, encapsulation, and extraction efficiency will again be discussed briefly in context of developing a lighting system.

SCV Instrumentation and Measurement

WEDNESDAY NOVEMBER 2

Blackfin: A Combined RISC/Signal Processing Architecture for a New Era

Speaker: Tim Wilkerson, Analog Devices
Time: Networking at 7:30 PM, Presentation at 8:00 PM
Cost: none
Place: Cogswell College, Room 197, 1175 Bordeaux Drive, Sunnyvale
RSVP: Please reserve by email with David Rivkin, david.rivkin@ieee.org
Web: www.ewh.ieee.org/r6/scv/ims/

The presentation describes the salient architectural features of the Blackfin Processor from Analog Devices as well as some of the larger applications areas. Multiple single core and dual core proliferations of the blackfin family are described as well as peripheral mix, and benchmark information showing strengths of the architecture as well as unique capabilities in such application areas as multimedia, networking, automotive and instrumentation. In addition, some C level compiler strategies are briefly described which are applicable to Blackfin.

SCV Magnetics

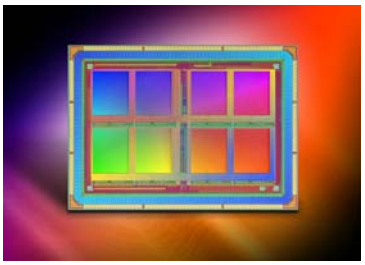
THURSDAY NOVEMBER 3

Toggle MRAM Performance and Outlook

Speaker: Jon Slaughter,
Freescale Semiconductor, Inc.
Time: Cookies & Conversation at 7:30 PM,
Presentation at 8:00 PM
Cost: none
Place: KOMAG, 1710 Automation Parkway,
San Jose
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/mag/

Dr. Jon Slaughter is a Distinguished Member of the Technical Staff and Manager of the Magnetic Materials and Structures Group, part of the Technology Solutions Organization, at Freescale Semiconductor. He and his team are responsible for developing materials and processes for the magnetic tunnel junction (MTJ) film stack that is at the heart of a new memory technology called Magnetoresistive Random Access Memory (MRAM). Prior to joining Motorola in 1996 to work on MRAM, Dr. Slaughter was an Associate Research Professor at The University of Arizona's Optical Sciences Center, specializing in the effects of film growth and microstructure on the properties of ultra-thin metallic films and multilayers. He earned a Ph.D. in physics from Michigan State University in 1988 where he was awarded the Sherwood K. Haynes Award for his research on the structure and electron transport properties of magnetic multilayers. He has 21 issued patents and over 80 publications in scientific/technical journals and proceedings. Dr. Slaughter has been active in a variety of international organizations and conferences, serving many times as conference chair, program committee member, session chair, and invited speaker.

Magnetoresistive random access memory (MRAM) employs a magnetoresistive device integrated with standard silicon-based microelectronics, resulting in a combination of qualities not found in other memory technologies. For example, MRAM is non-volatile, has unlimited read and write endurance, and has demonstrated high-speed read and write operations. This presentation will include an overview of the characteristics of our 4Mb Toggle-MRAM circuit based on magnetic tunnel junction (MTJ) devices, and outline paths for improving performance and scaling to higher densities. This 4Mb circuit is currently being qualified for production and is expected to be the first MRAM in volume production. Specific technology demonstrations for improving both the read and write operations in future generations of MRAM will be presented. For example, high-MR, MgO-based tunnel junction material has been integrated with 180nm and 90nm CMOS circuitry to improve the read performance. As an example of a path toward significantly reduced write currents, a demonstration of a new enhanced permeability dielectric material will be presented.



Freescale 4MB MRAM Device

SCV Electromagnetic Compatibility

TUESDAY NOVEMBER 8

BPL Emissions Compliance Guidelines

Speaker: Jerry Ramie, ARC Technical Resources
Time: Social 5:30 PM, Presentation 7:00 PM
Cost: none
Place: Applied Materials Bowers Cafeteria, 3090 Bowers Ave., Santa Clara
RSVP: not required
Web: www.scvemc.org

Access Broadband over Power Lines is a new type of carrier current technology that provides high-speed broadband Internet access using electric utility companies' power lines. Controversy has surrounded the deployment and testing of BPL systems since they were introduced. The Certification requirements outlined in this Presentation are the required means for assessing compliance and mitigating interference complaints. Understanding their unique features will be necessary for EMC, Power and Radio Communications engineers to ensure BPL compatibility with existing radio services.

Jerry Ramie has authored an August, 2005 article on BPL Certification testing requirements, which can be viewed at http://www.conformity.com/0508/0508review.html . Jerry serves on the Power Engineering Society's P1775 committee on BPL Electromagnetic Compatibility and the EMC Society Ad Hoc Working Group on BPL. Jerry has over 23 years of experience in the field of EMC. He is an IEEE – EMC Society Member and NARTE-certified EMC technician. He founded ARC Technical Resources Inc. in 1989.

The Presentation describes the various system architectures, and details the Certification requirements of the FCC Report and Order 04-245 that took effect on February 7, 2005. This work is from the Electric Power Research Institute's publication # 1011663, and is now available to the public by calling 1-800-313-3774 (option 2).

WEDNESDAY NOVEMBER 9

Carbon Nanotubes: Enhancing Conductivity of Conductive Plastics

Speaker: Dana Hammer-Fritzinger, NanoDynamics
Time: Seated dinner at 6:30 PM; presentation at 7:30 PM
Cost: $25 if reserved by Nov. 6; $30 at the door; presentation-only is free
Place: Ramada Inn, 1217 Wildwood Ave (Fwy 101 frontage road, between Lawrence Expy and Great America Pkwy), Sunnyvale
RSVP: Please reserve and pay in advance using our PayPal on-line system or email Janis Karklins at karklins@ieee.org
Web: www.cpmt.org/scv/meetings/cpmt0511.html

Carbon nanotubes have some unique properties that can allow us to extend or even replace CMOS, improve the properties of interconnect materials and thermal spreaders and even create sensor and display structures. Challenges still include economics and processing as well as a lack of hard performance data. This talk outlines the challenges and opportunities and illustrates with real examples from NanoDynamics' experience.

Dana Hammer-Fritzinger: Before joining NanoDynamics as a Product Manager, Ms. Hammer-Fritzinger has had a broad background in industry including a stint in the Finnish pulp and paper industry as well as several years with ATOFINA's Global Organic Peroxides R&D where she was nominated for an Elf Aquitaine Innovators Award for her work in process NIR. More recently, Dana spent eight years with DuPont as the Manager of Analytical Technology and Competitive Testing for the Surfaces business, providing technical support to sales, product development and acquisition teams, and ultimately establishing a technical marketing and services function.

Ms. Hammer-Fritzinger holds a Bachelor's Degree in Chemistry from the State University of New York at Geneseo, her Master's Degree in Analytical Chemistry from the University of Helsinki and an M.B.A. from Canisius College in Buffalo NY.

.

SCV Grads of the Last Decade (GOLD)

WEDNESDAY NOVEMBER 9

Challenges and Innovations for Development of SOCs

Speaker: Dr. Sung-Mo "Steve" Kang, Professor and Dean, Baskin School of Engineering, University of California at Santa Cruz
Time: 7:00 PM
Cost: none
Place: TBD (see website)
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/gold

This event is open to ALL (not JUST Grads of the Last Decade), so feel free to bring your friends and colleagues along.

Dr. Sung-Mo "Steve" Kang is Professor and Dean, Baskin School of Engineering, University of California at Santa Cruz. While at AT&T, Dr. Kang led the development of world's first full 32-bit CMOS microprocessor chips and their peripheral chips as supervisor of high-end microprocessor design group. He has served as a member of Board of Governors, Secretary and Treasurer, Administrative Vice President, and 1991 President of IEEE Circuits and Systems Society. He was the Founding Editor-in-Chief of the IEEE Transactions on Very Large Scale Integration (VLSI) Systems. He has served on the editorial boards of IEEE Transactions on Circuits and Systems, International Journal of Circuit Theory and Applications, and Journal of Circuits, Signals and Systems, and currently serves on editorial board of Proceeding of the IEEE.

SCV Electron Devices

MONDAY NOVEMBER 7

A Survey of Semiconductor Devices

Speaker: Dr. Kwok Ng, MVC
Time: 6:00 PM Pizza; 6:15 PM Presentation
Cost: none
Place: National Semiconductor, Building 31 Large Auditorium, 955 Kifer Road, Sunnyvale
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/eds

Kwok Ng received his B.S. from Rutgers University in 1975 and Ph.D. from Columbia University in 1979, both in Electrical Engineering. He joined AT&T Bell Labs in 1980 in Murray Hill, New Jersey. After working in AT&T spin-offs-- Lucent Technologies and Agere Systems, he is currently a Director in MVC, working on flash nonvolatile memories. His experience also includes Si CMOS and LDMOS devices, SiGe HBT, and III-V FET. Dr. Ng has held positions as Editor of IEEE Electron Device Letters and Liaison to IEEE Press. He is the author of "**Complete Guide to Semiconductor Devices**", and is currently working as a co-author with Simon Sze on the new edition of the well-known "**Physics of Semiconductor Devices**".

This talk is based on the materials I had collected for my book (**Complete Guide to Semiconductor Devices**, Wiley/IEEE Press, 2002). My search had identified close to 100 semiconductor devices, ranging from the old and sometimes obsolete to the recent quantum-well devices. These devices are organized into groups and subgroups for a better overview, and the justification for such classification is discussed. Emphasis is put on qualitative understanding, and the use of equations is kept to minimum. It is the goal that the audience gains a better perspective on this broad field, and some familiarity with the large variety of names of semiconductor devices. Besides presenting the list of devices, I will also offer some comments and observations.

CLICK!

THURSDAY NOVEMBER 10

On the Use of Artificial Intelligence in Microwave Hardware Design

Speaker: Dr. John R. Sanford, CTO, Cushcraft Corporation Inc.
Time: 6:00 PM Refreshments and Social Hour; 6:30 PM Presentation
Cost: none
Place: Intel Corp. SC12-Auditorium, 3600 Juliette Lane, Santa Clara
RSVP: not required
Web: www.mtt-scv.org/nov_mtg.html

The development and use Artificial Intelligence Optimizer ("AIO") antenna design software will be discussed. AIO algorithms solve Maxwell's Equation real time to rapidly develop optimal solutions within the constraints of physical antenna design. This capability substantially expands the ability to quickly design manufacturable, engineered-to-order, and optimal performance antennas, filters and various microwave structures. In addition, the technique has been applied to analysis of the relative tradeoffs of various Smart Antenna and MIMO configurations.

Dr. John R. Sanford, is currently CTO of Cushcraft Corporation. In July of 2004, Cushcraft acquired Optimal RF, a startup company active in the area of next generation antenna design where Dr. Sanford served as President. Prior to this he was Chief Technical Officer of REMEC, Inc. where he oversaw the company's technology roadmap, IP development and strategic partnerships. At REMEC, Dr. Sanford held a number of positions including head of engineering of Northern California operations and GM of the Fixed Wireless Group. Prior to that, he was founder and President of Smartwaves International, which was acquired by REMEC in February, 1999. At both locations Dr. Sanford developed microwave transceivers and related products including antennas, filters and amplifiers. Prior to that he was a Professor at Chalmer's University of Technology where he taught courses and conducted research related to Electromagnetics, Antennas and Array Signal Processing. From 1988 through 1993 Dr. Sanford headed the Mobile Tower Top Group at Huber & Suhner AG. There he introduced the first base station patch antenna, switched beam antenna along with a variety of unique filters, EMP and optical products. From 1985 to 1988 he was a research engineer and group manager with the Georgia Tech Research Institute where he designed military radar and communication systems.

OEB Communications

THURSDAY NOVEMBER 10

Broadband Powerline Communication -- Alternative or Synergy for Wireless

Speaker: Victor Dominguez, Co-Founder and Vice President of Strategy and Standardization, DS2
Time: 6:30 PM Pizza and drinks; 7:00 PM Presentation
Cost: none
Place: Bishop Ranch 1, 6101 Bollinger Canyon Road, San Ramon (just off I-680)
RSVP: by Nov. 9 via email to oeb@comsoc.org to allow us to order the correct number of pizzas
Web: www.comsoc.org/oeb

Victor Dominguez is the Chairman of ETSI PLT (Powerline Telecommunications) committee and Chairs or contributes to several other key industry groups including, IEEE, ETSI, Cenelec, UPLC, CISPR, PLCforum and UPA. He is a Co-founder and Vice-President of Strategy & Standardization at DS2. He also participated in product development, including the PHY and MAC layers. Prior to DS2, Victor was involved in several research and lecturing positions at the leading technical institution in Spain, the Polytechnic University of Valencia, and also as a consulting expert to the European Commission.

Powerline Communications (PLC) and Wireless communications have different strengths: wireless has mobility; powerline has high quality coverage. For backbone applications and high quality video and audio distribution where mobility does not apply – displays are seldom moved, require a power cord to operate and demand error free communications – then PLC offers the only widely viable solution. This presentation will begin with an overview of the State-of-the-Art of Powerline Communications for Access, In-Building distribution and Home Networking applications followed by a discussion of how PLC competes with, complements and co-exists with wireless technologies for both Wide Area and Local Area Networks.

We will continue our feature at the meeting of providing some networking time for those that want to stand and make a brief announcement. If you're looking for a new position, have a position to fill, want to let us know that your new start-up is ready for business or have a similar announcement, bring your resumes, job descriptions or company brochures and be prepared to make a match. Please keep your statements brief, so we'll have time for everyone. There will be time before and after the formal meeting for one-on-one discussions.

SCV Nanotechnology Council

TUESDAY NOVEMBER 15

Nanotech: Imagine the Opportunities – Half-Day Seminar showcasing University Graduate Research

Time: Noon - 5:30 PM
Cost: $35 for IEEE members; $55 for non-members ($10 higher at door) – includes light lunch
Place: National Semiconductor Building 31, 955 Kifer Road, Santa Clara
RSVP: Prepay online at Nano Council's website, or RSVP to dhavaljb@aol.com
Web: ewh.ieee.org/r6/san_francisco/nntc/11_15_05.html

TALKS:

DNA-Templated Nanoparticle Assembly: Programmable Scaffolds for Nanoscale Devices Shelley A. Claridge, Department of Chemistry, UC Berkeley

Single Nanotube Nanofluidic Transistors, Rong Fan, Department of Chemistry, UC Berkeley

Modified Viral Capsids as Targeted Delivery Vectors for Anticancer Agents, Jacob M Hooker, Department of Chemistry, UC Berkeley

The Impact of University Graduate Research in the United States, Professor Arun Majumdar, Almy & Agnes Maynard Chair Professor Department of Mechanical Engineering, UC Berkeley

Enzyme Catalyzed Metallic Nanoparticle Synthesis, Daniel M. Scott, Department of Chemistry, UC Davis

Self-assembled Ferromagnetic alpha-Fe Nanowires for High-density Recording Media Applications. Laden Mohaddes-Ardabili, MSE UC Berkeley

Semiconductor Nanostructures as Subwavelength Optical Elements for Photonics and Sensing, Donald J. Sirbuly Ph.D. Department of Chemistry, UC Berkeley

Plasma-enhanced CVD Carbon Nanofiber for Interconnect Via Applications, Quoc Ngo, Center for Nanostructures, Santa Clara University

See the frontier in Nanotechnology and help shape it.

Novel features of this Symposium include:

- Pre-publication briefs of university graduate research topics in nanotechnology.
- Challenge to the attendees to contribute imagined potential applications and opportunities that may transcend the present scope of the presented work.
- Ample opportunity for networking with the graduates and other attendees.

Graduate research topics to be presented include:

- Nanoscale optical devices on DNA scaffolds
- Nanotube nanofluidic transistors and circuits
- Anti-cancer drug delivery using viruses
- Ferromagnetic nanowires and high density storage
- Nanowire-based photonics and sensing
- Fabrication of nano-devices through biological catalysts.

SCV Engineering in Medicine and Biology

WEDNESDAY NOVEMBER 16

High Frequency Ultrasound Imaging of the Anterior Segment of the Eye: Imaging Schlemm's Canal for Diagnosis and Surgical Guidance

Speaker: Ron Yamamoto, Chief Scientific Officer and Director, iScience Surgical Corp.
Time: optional dinner with the speaker in the Stanford Hospital cafeteria at 6:15 PM (no reservation needed). Formal meeting is 7:30 PM
Cost: none
Place: Clark Center Auditorium (South-West end of the Stanford Hospital and Medical School); see map on website
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/embs/

A new, high-frequency (80 MHz) ultrasound imaging system (iView) for in-vivo intra-operative visualization of anterior microstructures of the eye, and its application in Schlemm's canal for glaucoma management, will be described.

Non-invasive medical imaging of the eye typically involves B mode ultrasound imaging at frequencies of 10 to 30 MHz for general imaging of the macroscopic structures, or an ultrasound biomicroscope (UBM) operating at 50 MHz for higher resolution. More recently, optical coherence tomography (OCT) has been used to image the posterior retina regions of the eye at very high resolution. However, none of the existing imaging systems for the eye are useful in imaging Schlemm's canal of the eye, an approximately 150 micron diameter channel for aqueous humor involved in glaucoma that is in the front of the eye. Also the existing imaging systems are not designed for intra-operative use to guide surgery.

iScience Surgical Corporation and collaborators have developed an ultrasound imaging system operating at a center frequency of approximately 80 MHz to visualize Schlemm's canal. The imaging system utilizes a mechanically scanned high frequency transducer coupled to a PC with software to control the transducer motion, RF and display the image. The handpiece housing the transducer incorporates a replaceable sterile interface to allow images to be taken in the operating room to assess patient anatomy and to guide microsurgery. In particular, the imaging system is currently being used to guide a micro-catheter developed by iScience Surgical to perform minimally invasive surgery of the eye.

SCV Solid State Circuits

THURSDAY NOVEMBER 17

PLL History: A Personal Viewpoint

Speaker:	Dr. Floyd Gardner, IEEE Fellow and author of the book Phaselock Techniques
Time:	Refreshments at 6:00 PM; Presentation at 6:30 PM
Cost:	donation for food costs
Place:	National Semiconductor, Building 31 Auditorium, 955 Kifer Road, Sunnyvale
RSVP:	not required
Web:	www.ieee.org/scv/ssc

Dr. Gardner, a Fellow of the IEEE, has been an independent consulting engineer since 1960. He is the author of *Phaselock Techniques* (recently issued in an expanded third edition), of *Simulation Techniques*, and of numerous articles in the professional journals.

Floyd Gardner has worked with phaselock loops since the late 1950s. A PLL, unimaginably exotic in those early days, has become a standard item, familiar today to most electronics engineers. Dr. Gardner will reminisce over the evolution of PLLs as seen through his own experiences. He will discuss how emphasis has changed from the extremely narrow-band systems of years ago to the wide-band applications of today. Key inventions and technology improvements will be reviewed.

THURSDAY NOVEMBER 17

Arc Flash Studies using Electrical Engineering Software

Speaker: Michael Nakamura, P.E., East Bay Municipal Utility District
Time: No-host social at 5:30 PM; Presentation at 6:15 PM: Dinner at 7:15 PM; Presentation continues at 8:00 PM
Cost: $22 for IEEE members; $25 for non-members
Place: Marie Callender's Restaurant (The Garden Room); 2090 Diamond Blvd, Concord (near the Concord Hilton Hotel)
RSVP: Please reserve by email to Gregg Boltz or telephone (925) 210-2571
Web: ww.e-grid.net/docs/0511-oeb-ias.pdf

Michael Nakamura has been with East Bay Municipal Utility District (EBMUD) for nearly seven years and holds the position of Senior Electrical Engineer. Prior to joining EBMUD, he worked for various local engineering consulting firms almost exclusively in the municipal water/wastewater industry. Mr. Nakamura has performed numerous short circuit, load flow, transient motor starting, protective device coordination, and arc flash studies for systems up to 21 kV. He is an active participant in EBMUD's electrical safety workgroup. Mr. Nakamura's experience includes design of electrical, controls, and instrumentation systems for wastewater treatment plants, water treatment plants, pumping plants, and hydroelectric plants. He is experienced in the programming, testing, startup, and commissioning of power distribution equipment, protective relays, and PLC control systems.

Mr. Nakamura received the B.S.E.E. degree from California Polytechnic State University at San Luis Obispo. He is a past chairman of the IEEE Oakland/East Bay Power Engineering Society, and is a current member of IEEE, IAS, and PES. Mr. Nakamura holds a Certificate in Project Management from UC Berkeley Extension, and is a Registered Professional Engineer in the State of California.

Recently, there have been numerous presentations regarding arc flash that provided a general overview of the topic. This presentation will go deeper and focus on how to perform an arc flash study using electrical engineering software. The presenter will first provide a brief review of the basics - what is arc flash, what are the Codes and Standards related to arc flash, and how does one determine the required PPE. The presenter will then follow this with a live demonstration of how to perform an actual arc flash study using electrical engineering software, such as SKM Power*Tools for Windows. A basic example will be discussed, constructed, and analyzed. Following the demonstration, there will be a discussion of the lessons learned from actual arc flash studies performed at EBMUD facilities.

No matter what your level of experience as an electrical professional, this meeting promises to be very informative, so don't miss it.

SCV Circuits and Systems

MONDAY NOVEMBER 21

A Digital Clock and Data Recovery Architecture for Multi-Gigabit/s Binary Links

Speaker: Jeff Sonntag, Synopsis
Time: 6:30 PM for Fast Food & drinks,
7:00 PM for Presentation
Cost: none
Place: Cadence Design Systems, Building 5,
2655 Seely Avenue, San Jose
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/cas

Jeff L. Sonntag received the B.S.E.E. degree from Carnegie-Mellon University in 1982, and the M.S.E.E. degree from Cornell University in 1983. He joined Bell Labs in 1982, where he spent 18 years developing high performance mixed signal integrated circuits, focusing on applications in disk drive read channels while his employer evolved into AT&T Microelectronics and Lucent Technologies. In recognition of his contributions in 1998, he was named a "Bell Labs Fellow". In 2002, he joined Accelerant Networks in the development of high speed serial transceivers, serving variously as mixed signal circuit designer, system architect, and Chief Technical Officer. Since the acquisition of Accelerant by Synopsys in 2004, he continues to develop SerDes IP in his role as Senior Member of Technical Staff.

Multi-Gigabit per second (Gbps) serial binary links are fast replacing traditional parallel data links in many applications. Examples include PCI moving towards PCIexpress and ATA moving towards SATA. Additionally, there exist many other applications with multi-Gbps serial links such as XAUI, FibreChannel and RapidIO. Thus the problem of architecting an effective Clock and Data Recovery (CDR) for multi-Gbps rates is becoming increasingly common. At the same time, the trend is for the serial link to become a peripheral function at the edge of a large ASIC, rather than the core function of a mixed signal ASSP. For this reason, effective solutions must be extremely low in power, implementable in the cheapest of digital process technologies, and easily ported across multiple technologies and speed targets.

The presentation will cover a general architecture for digital Clock and Data Recovery (CDR) for high speed binary links. The architecture is based on replacing the analog loop filter and VCO in a typical analog PLL-based CDR with digital components. A linearized analysis of the bang-bang phase detector and CDR loop including the effects of decimation and self-noise is included. Finally, measured results are presented that corroborate the modeled results.

SCV Consumer Electronics

TUESDAY NOVEMBER 29

Distributed HD IPTV and Audio over Powerline

Speakers: Victor Dominguez, Chair of ETSI PLT and a founder of DS2 and Director of Strategy and Standardization; and
Chano Gomez, VP of Technology and Strategic Partnerships, ETSI PLT
Time: 6:30 PM for pizza and drinks; 7:00 PM for Presentation
Cost: none
Place: Maple room at HP Cupertino, at Wolfe and Pruneridge (off 280)
RSVP: by email to scv.ce@ieee.org
Web: www.ewh.ieee.org/r6/scv/ce

Chano Gomez is Vice President for Technology and Strategic Partnerships for DS2 and heads the North America operations. He joined DS2 in 1999 as a Design Engineer in the System Architecture Group. His pioneering work in Powerline Technology has led to several patents. He holds a degree in Telecommunication Engineering from Valencia, Spain.

200 Mbps Powerline Communications (PLC) transceivers have been in production since 2004 and are in commercial deployments for both in-home video distribution of IPTV and Broadband over Powerline (BPL) access services. Competition between Telcos and Cable operators together with the arrival of HD TV in thinner flat-panel formats is driving the demand for in-home video (and audio) distribution with whole-house coverage. PLC technology implements both these applications and more with many advantages of performance and convenience.

CONFERENCE CALENDAR

The **CONFERENCE CALENDAR** is a service to our IEEE Members. It outlines upcoming IEEE workshops and conferences in the Bay Area. Please submit items to the GRID Editor: editor@e-grid.net.

Conferences are also encouraged to purchase display space in the **GRID.pdf** and publicize their events on our website and in our **e-GRID** email notification service. For the Conference Publicity flyer, please download:

www.e-grid.net/docs/conf-flyer.pdf

Nov. 6-10 – ISTFA'05:

Int'l Symposium on Testing and Failure Analysis

- Technical Sessions, Panel Discussions, Tutorials
- Exposition: Tuesday-Wednesday, Nov 8-9

Held this year for the first time at the San Jose Convention Center, ISTFA'05 combines technical sessions, tutorials, an exhibition, and user group meetings with a focus on making the full experience a strong benefit for the attendee. The limited number of selected, high-quality papers only requires two tracks throughout the program, for good access.

See Page 4
for more details

Internationalization and Unicode Conference

- March 6-8, 2006
- Hyatt Regency Hotel, Burlingame (SF Airport)
- Tutorials: Monday, March 6
- Sessions: Tuesday-Wednesday, March 7-8

Unicode experts, implementers, clients and vendors are invited to attend this unique conference on the Unicode Standard and internationalization. Exchange ideas with leading experts, find out about the needs of potential clients, or get information about new and existing Unicode-enabled products.

See www.unicodeconference.org/ieee
for more details

Calls for Papers

June 11-13, 2006 – SID '05:

Society for Information Display International Symposium, Seminar, & Exhibition

- - Paper Summary Deadline: **December 1, 2005**
- - Location: San Francisco, June 11-13, 2006

SID'06 will have 250^{+} exhibitors and 7,500^{+} attendees - display scientists, engineers, manufacturers, entrepreneurs, marketers and end-users with original papers on all aspects of research, engineering, application, evaluation, and utilization of displays.

Go to www.e-grid.net/docs/sid06.pdf
to download the Call for Papers

June 11-13, 2006 – SID '05:

IEEE Radio Frequency Integrated Circuits Symposium

- Paper Summary Deadline: **January 2, 2006**
- Location: San Francisco, June 11-13, 2006

RFID'06 is part of Microwave Week in San Francisco. Check out the Call for Papers for topics.

Go to www.e-grid.net/docs/rfic06.pdf
to download the Call for Papers