SESSION IX: STATIC AND NONVOLATILE MEMORIES

THAM 9.6: A 256-Bit Nonvolatile Static RAM

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A 32 X 8 STATIC CMOS nonvolatile RAM with pin compatible features* will be covered. The memory state of the RAM can be stored in a nonvolatile manner at any time by merely applying a high voltage pulse to the memory power supply. In effect, the device is a dual memory consisting of a volatile RAM coexistant with a nonvolatile ROM structure. This device may be used as a scratchpad memory with a fixed pattern stored in the nonvolatile portion of the memory. The contents of the nonvolatile memory are retrieved by sequentially removing and applying dc power to the chip. The RAM will power up in the nonvolatile state. Also, if a high voltage pulse is applied to the power supply, the current contents of the RAM is written into the nonvolatile portion of the memory.

As can be seen from Figure 1, the memory cell is a standard six-transistor latch in which the N-channel devices include a floating polysilicon gate. For chip power in the normal range of +5 to +10V, the RAM functions conventionally. To memorize the state of the latch nonvolatilely, the chip power is pulsed to 20V for approximately 10μs. This action causes the stored charge on the buried silicon gate to change in accordance with the information stored in the RAM cell and thus will alter the threshold of the N-channel devices. The threshold of the N-channel device that is conducting will increase and the other will decrease. When the power is removed and reapplied, the cell will power up with the complement of the memory state that existed during the nonvolatile write. This effect can be rendered transparent by utilizing an extra RAM bit and exclusive or logic in the input and output buffers.

A block diagram of the circuit is shown in Figure 2, and the photomicrograph of the fabricated circuit appears in Figure 3. The chip is organized as four blocks of 8 X 8 bits. A negative going $\overline{CE}$ enables the chip functions for memory read (MRD) and memory write (MWR). The row decoder selects one of thirty-two lines to be read or written, while each sense amplifier detects the memory state of the cell on the selected column and row. The BUS line is bi-directional for input and output.

The key element of the nonvolatile structure is the N-channel device with the floating polysilicon gate. A cross sectional view of this device is shown in Figure 4. The structure over the channel consists of 1000Å of SiO_2, 3000Å of polysilicon, less than 200Å of SiO_2, 400Å of Si_3N_4 and 10,000Å of aluminum. The key element in the structure is a small area of thin SiO_2 located over the drain. It is across this region that charge transport occurs through tunneling[1,2] when a high voltage is applied between gate and drain. The cell is structured so that the metal to poly capacitance is approximately ten times higher than the combined poly to drain, channel and source capacitances. With this structure 90% of the applied voltage will initially appear across the thin tunneling region. When a positive voltage pulse is applied between gate and drain and then removed, the net effect is to increase the negative charge on the buried gate and therefore increase the threshold of the device. A pulse applied in the opposite direction has the effect of decreasing the device threshold.

Figure 5 shows typical nonvolatile read and write waveforms. In the time slot t_0 to t_1 the RAM is used normally as a volatile device. In the period t_1 to t_2 a high voltage pulse is applied to the chip supply. During this time the thresholds of the conducting N-channel devices decrease and the nonconducting N-channel devices increase. During the time period t_2 to t_3 the state of the memory cell may be altered nonvolatilely. The time period t_3 to t_4 is a power down condition necessary for a nonvolatile read. Time period t_4 to t_5 is a ramped power on condition which enables sufficient time for the skewed thresholds to cause the RAM cells to power up in the complement of the state that existed during the t_1 to t_2 time period.

The nonvolatile RAM device affords a virtually unlimited number of read and write cycles before the need for refresh, approximately 10^6 nonvolatile storage cycles, 700ns read times and 300ns write times, 10μs nonvolatile write times at 20V, and operation at either +5 or +10V with no clocks required.

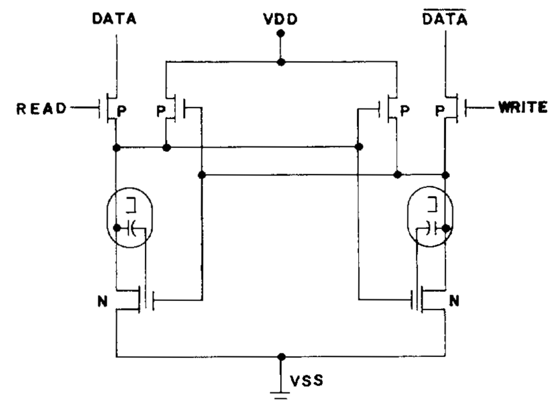

FIGURE 1—Schematic of nonvolatile RAM cell.

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*Compatible with RCA1824.

[1] Lenzlinger, M. and Snow, E.H., "Fowler-Nordheim Tunneling into Thermally Grown SiO_2", *Journal of Applied Physics 40*, p. 279; 1969.

[2] Harari, E., "Conduction and Trapping of Electrons in Highly Stressed Ultrathin Films of Thermal SiO_2", *Applied Physics Letters 30, 11*, p. 601; 1977.

CONTROL LOGIC
INPUT/OUTPUT
32X8 MEMORY
POWER ON RESET
SENSE AMPLIFIERS
ADDRESS INPUT BUFFERS
INPUT/OUTPUT
DECODER

FIGURE 3—Photomicrograph of the nonvolatile RAM.

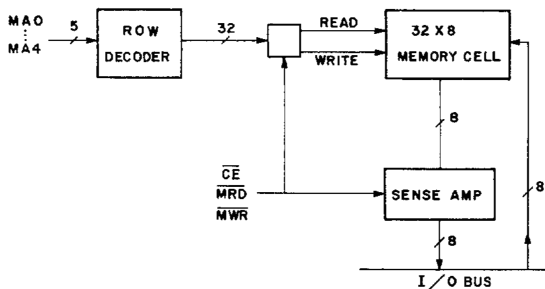

FIGURE 2—RAM block diagram.

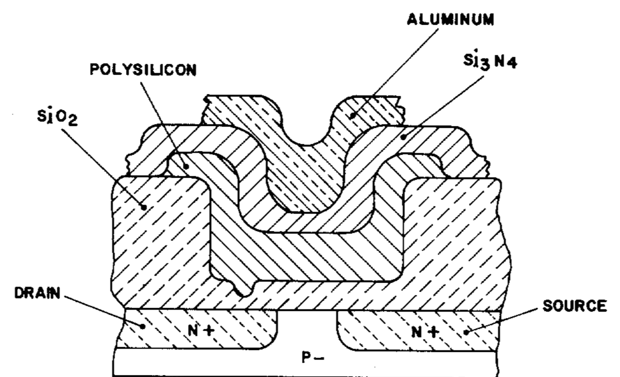

FIGURE 4—Cross sectional view of the floating gate N-channel memory device.

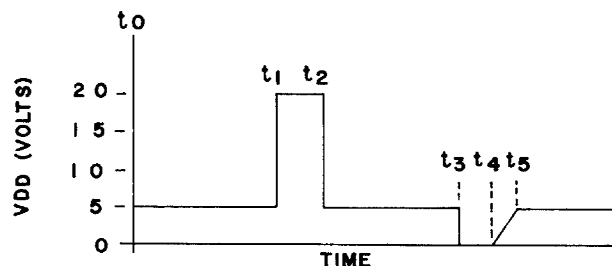

FIGURE 5—Nonvolatile write and read waveforms.