Reliability Society

NEWSLETTER

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IEEE

CONTENTS

Editor:
Bruce Bream

President's Report

I was pleased to see that we have already received three nominating petitions for the six Reliability Society Administration Committee positions for the class of 1995, carrying twelve (or more) names of Society members, excluding students. Lowering the required number of members required on a petition from 25 to 12 has resulted in more petitions this year than we have received in the history of the Society.

This shows that our decision to reduce the number was a sound one, and it also shows that we have a number of members who are interested in becoming more active in Society affairs.

You will receive a ballot in the mail (probably in August). I would like to encourage each of you to review the candidates' qualifications and to vote for those you feel are most qualified to represent your interests.

The Reliability Society is planning to participate in the IEEE Video Conferencing Program during 1995.

The IEEE Videoconferencing program provides live interactive telecasts of timely topics in electrical engineering. The programs are telecast to participating corporations, universities and IEEE organizations. Video tapes are also available for use at later dates.

The current plan, which will be discussed at the July Administrative Committee Meeting, is to develop a three hour telecast for presentation early in 1995. The topic under consideration is "Developing Reliable Software," with Sam Keene, Ted Keller, and John Musa making the presentation.

W. Thomas Weir
President, IEEE Reliability Society

Editor's Column

A well known fictional short story once made the point that the "clothes makes the man". In the pitch of a bank robbery, one of the robbers, disguised as a policeman, unwittingly arrests his cohorts. Unfortunately it's not always that simple to assume a role requiring technical skills. Training, experience, and selection of the right people are the keys to good R&M analyses. Just like any other highly technical task, it's not just the mechanics of the tasks at hand that one needs to know; it's also understanding. Picking up a textbook on a subject and then launching into an analysis is a laudable effort, but it's also fraught with potential traps from unknown errors in application. Its the assumptions that get you. And it's these hidden or non-communicated assumptions that cause managers and engineers to sometimes squirm when they see the results of an R&M analysis. Both managers and engineers need to gain an understanding of the benefits and limitations of R&M analyses. The offerings of IEEE and others should be utilized to their fullest. Training classes should take up the challenge to be more than just cookbook courses going beyond the lure of the calculator and n-digit precision. Training also needs to be augmented with mentoring to pass on experience. And not the least concern, organizations need to pick the right people for the job. Needless to say, interest and enthusiasm in the task at hand is important to a job well done. As a result, the best aspects of the R&M craft can be applied by knowledgeable specialists who can add value to the organization and its products.

Bruce Bream
Editor, Reliability Society Newsletter

Reliability Society Newsletter Inputs

All RS newsletter inputs should be sent to:
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The schedule for submittals is:

Newsletter	Due Date
January	November 19
April	February 26
July	May 28
October	August 27

ADVERTISING RATES

All copy that contains graphics or special fonts must be camera-ready or delivered on computer disk and be received by the due dates indicated.

Ad Size	One Time	2-3	4+
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Third Page (vertical)	$240	225	210
Quarter Page	$205	190	180
Eighth Page	$120	110	100

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RELIABILITY SOCIETY OFFICERS

Chapter Activities

Cleveland Chapter

The Cleveland Chapter has had three meetings over the last few months. Our March meeting was a "Engineering Workstations Operating Systems: a comparative analysis of Windows NT and UNIX Solaris." This meeting was from the Learning Center Live Satellite Videoconference Seminars. Five experts, Dan Candy, et al, talked about requirements for Engineering Workstations of the Future and use of Windows NT and UNIX Solaris as solutions. This meeting had a full house. Some could only get the notes.

Our April meeting wa on "Outreach Strategies: Visibility, Partnership and Education". John Hairston, NASA/Lewis Chief External Programs, took some time out of his busy schedule to bring us up to date on current events at Lewis Research Center to interact with the Cleveland community; an airport display and an improved Visitor's Center in our IX Center were discussed. Total quality efforts are being implemented. Many other changes are being discussed. Progress is being made on our Journey to Excellence. A timely, well received topic with another full house.

Out last meeting was a tour of the Federal Reserve Bank. The group enjoyed seeing how the bank system operates here in Cleveland. Money is a complex commodity closely controlled and monitored. Banks are carefully regulated to control inflation. A nice lunch at Stouffer's on the Town was a big hit; a good once in a while treat.

We are working to put together a local publicity committee for RAMS '95. We would like to get one member in the Washington area from each sponsoring society to work on this committee. Publicity can make or break a symposium. Can you help? How can we inform the people of the Washington area about our symposium? If you are interested in working on this committee, please contact Vince Lalli at (216) 433-2354.

Our community outreach project has made some progress. Dr. Cath, Program Committee chairperson, has had two meetings. After the smoke cleared, four sessions are the top contenders: Controls, Instrumentation, Biomedical and Professional Advisers. This should cover the hot topics in Cleveland for our one day workshop.

All-in-all here in Cleveland we are having fun staying active and trying to serve our membership.

Vince Lalli
Cleveland Chapter Chairperson

Philadelphia Chapter

At the May 17th meeting the following topics were presented:

- Ethics - Good, Bad and? by Mr. William W. Middleton
- Navy Command and Control System Design by Mr. Charles J. Smith

Fulvio E. Oliveto
Chairman, Philadelphia Section

Los Angeles Chapter

On March 31, Dr. Bruce Krell, Independent Consultant, spoke on "Commercial vs. DoD Development: A Comparison". His presentation focused on recent speeches by DoD officials indicating the aerospace and defense contractors should make better usage of commercial software development practices. This was a joint meeting with the Los Angeles Chapter of ACM.

In May, we heard Bruce Moor, of Hughes Aircraft discuss Electric Vehicles. California has set the clean air standard by mandating that 2% of automobiles sold in 1998 shall be zero emission vehicles, and the Federal Government is assisting with funding for a Hughes Aircraft Company's involvement in electric vehicle propulsion systems and explained the technology in electric vehicle propulsion systems and the technology advances that have been made which enable the industry to meet the performance needs of today's market.

Meetings in planning: In June, Larry Stern, IEEE Congressional Fellow, will brief us on where Aerospace will be in the next 5 years. In July, Charles Finnila will discuss Combining Data Compression and Encryption. Other presentations include Software Safety and Quickring Controller.

Our Bulletin Board is very active with over 400 subscribed members. Member-

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ship is free. We offer meeting information, Jobline, E-Mail, Video Tape Exchange Information, Shareware and Demos. Phone is (818)768-7644, 300-2400 baud.

Our Videotape Exchange program currently has over 150 videotapes available. The latest listing can be viewed and downloaded through the bulletin board.

Loretta Arellano
Los Angeles Chapter

Singapore

The Singapore Joint Rel/CPMT Chapter main activity so far has been the organization of a Failure Analysis and Reliability conference every 2 years. Our first one was in 1987 and our most recent one in November '93. Since the start of this year we have been holding tutorial courses — once a month, 3 days each on various aspects of reliability and failure analysis. We plan to have a total of 11 tutorials this year and hopefully be able to sustain this on a yearly basis. We source our lecturers from the local university and the industry in Singapore. We also have looked at and invited prominent people from the U.S. I have included a description of our just completed FA & Reliability conference, called IPFA for short.

Report for IPFA 93
4TH IPFA
1st-5th November 93

The 4th International Symposium of Physical and Failure Analysis of Integrated Circuits was held at the West Inn Stamford from the 1st to 5th November 1993 in Singapore. A total of over 170 people from 12 countries from all over the world attended. In all 50 papers were presented covering many areas for application and research in Failure Analysis and Reliability Physics. The Conference started with an invited paper entitled " Construction Analysis of DRAMs by Atomic Force Microscopy: A New Approach" by Dr E. Druet of IBM France. This was among one of the number of papers that used Atomic Force Microscopy techniques in imaging or surface characterisation. In addition to the symposium there was a parallel exhibition where the latest in failure analysis equipment was displayed. There was a strong presence of Microprobe suppliers in this exhibition. Wentworth, Mircomanipulators, and Alessi brought along their eight inch systems for this exhibition along with CAD navigation and motorised probes for display. A total of 4 tutorials were given. The tutorials were well attended and attracted more then 100 participants. Tutorial topics were on Failure Analysis of Si Device Chip using EMMS, OBIC, LCM, EBP, FIB and CAE by Dr Kiyoshi Nikawa from NEC, Flip Chip Solder Bump Technology by Dr Paul Totta and Dr Karl Puttlitz from IBM, System Reliability by Professor A. C. Brombacher from Philips and Characterisation of ULSI/VLSI by Dr George TT Sheng from ITRI ERSO Taiwan. Highlights on the papers presented at this conference showed the following trends - increasing use of Atomic Force Techniques and the use of TEM, Electron Beam testing, and Focussed Ion Beams as standard techniques as part of regular failure analysis activities. Up till 4 years ago these were considered exotic techniques and available only at a selective few well known research laboratories in the world. This reflects the fast pace of change and progress in the semiconductor IC business. This conference is organized once every 2 years and the organizing committee comprises people from the industry and the university who form the Failure Analysis Special Interest Group. This conference is organized in conjunction with the IEEE Singapore Section Reliability/CHMT Chapter, Centre of Failure Analysis and Reliability NUS and the Institute of Microelectronics NUS.

Best regards

Swee Yong Khim
Reliability/CPMT Chairman
1994 Singapore Section
Texas Instruments Singapore
Failure Analysis Lab Mgr

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(continued from page 3)

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Please help us keep our list of chapter chairpersons current. Send your changes/updates to the Newsletter Editor or the Society Secretary (see page 2 for addresses).

ADCOM Meeting Summary

The Reliability AdCom met was held during IRPS on 11 April 1994 at the Fairmont Hotel in San Jose. Dick Kowalski presented the Society budget and informed us that he is in the process of drafting the 1995 budget. There was a request to increase the page count of the Transactions to reduce the backlog which will impact the budget. Dick proposed not increasing member dues but in light of the anticipated increase in postage, we may consider a dues increase next year.

The next AdCom meeting is scheduled for July at the IEEE Headquarters in Piscataway. Henry took the action to determine how many people would like to go on a tour of the headquarters. The Fall meeting will be held at the University of Maryland once again on October 1st. This date does not conflict with a University home football game. Dick Doyle will hold his Technical Operations meeting on the Friday preceding the AdCom.

Henry Hartt and Marv Roush are working on a draft policy/procedures for awards. Draft should be available for review at the July AdCom.

Tom Weir presented a listing of new Society members sorted by country for a total of 464 in 1993 and 186 in 1994 (so far). Fifty four countries are represented.

Jim Colvin, of the Santa Clara chapter, presented their chapter activities.

There was discussion that since we now have direct election of AdCom membership, we need to have a job description for each job. Tom took the action to contact each officer for input. Dick Kowalski has a treasurer's job description that can be used as a template.

Field of Interest is up for vote at the next TAB meeting (June).

Tom reported that the IEEE fellows board has never had a Reliability Society representative. He reported that Val Monshaw is our representative.

Tom submitted a report and viewgraph presentation from Mike Cushing on Process Action Team for Specification and Standards - Final Report. It was recommended that Mike give a presentation on its status at the next meeting.

Marv Roush reported that the listing of Distinguished Lecturers is being updated.

Sam Keene reported that he is coordinating the list of AdCom candidates. IEEE needs three months to do balloting.

Sam reported that we are on schedule for the video conference. Bob Kahrman is to provide us with at target date. Sam is to provide status in July where we are to vote on a full commitment. We must have a quorum for this vote, therefore Henry has the action to create a form (for proxy vote) if AdCom members cannot attend the July AdCom meeting.

Loretta Arellano
Secretary, Reliability Society

IEEE Metric Policy

All IEEE Organizational Units shall:

A. Actively support the use of the International System of Units (Le Systeme International d'Unites, or SI), the modernized metric system;

B. Follow SI-based metric practices as detailed in IEEE Standard 268, American National Standard for Metric Practice, to express measured and calculated values of quantity in all IEEE publications, including standards;

C. Promote the understanding and use of SI in education at all levels, both within the profession and in society at large.

Plans for the implementation of this policy by January 1, 1998, at the latest, shall be developed by the major boards of the Institute and reported to the Board of Directors no later than January 1, 1995. Necessary exceptions to this policy, such as whether a conflicting world industry practice exists, must be evaluated on an individual basis and approved by the responsible major board of the Institute for a specific period of time. The major board responsible for the publication or activity will be responsible for monitoring compliance.

Adopted by the IEEE Board of Directors
November 21, 1993

Reliability ADCOM Meeting Schedule

The following Reliability Society ADCOM meetings and discussion topics are scheduled. Any Reliability Society member wishing to attend a meeting is cordially invited as a guest. However, please notify either Dick Doyle at (619)459-6504 or Henry Hartt at (202)646-6339, if you plan to attend. The first two ADCOM meetings each year are held in conjunction with the RAMS and IRPS conferences. These conferences are scheduled for Washington, DC and Las Vegas in 1995.

Saturday, 16 July 1994
8:00 AM to 4:00 PM
IEEE Service Center
Piscataway, New Jersey

- Methods of improving the Reliability Society Transactions
- Finalizing the contract for IEEE TV presentation on Software Reliability
- Improving our Awards Presentation for RAMS 1995
- Society Position Guides
- All Committee Reports
- Other topics

Saturday, 1 October 1994
8:30 AM to 4:00 PM
University of Maryland
Conference Center
University Park, Maryland

- Voting on the suggested improvements to the Reliability Society Transactions
- Finalizing our Awards Presentation for RAMS 1995
- All Committee Reports
- Other topics

MIL-HDBK-217 Status

Rome Labs is currently responding to comments on the draft Notice 2 to MIL-HDBK-217F. A publication date in late summer is expected. The main changes are in the models and data for passive components and surface mounted components.

Wanted! A Few Good People to Serve on the RAMS Management Committee

A few energetic volunteers are needed to fill openings on the management committee of the Reliaibility Symposium. It's a great group of people, its educational and it can be career enhancing.

The management of the symposium is accomplished by sponsor member volunteers, with the concurrence and support of their corporate, government or academic employers. The Advisory Board, which is composed primarily of senior corporate and military management individuals, provides guidance on management of the symposium.

This is an opportunity to work with other professionals in the reliability (and associated) fields and meet senior management from both military and corporate sectors that are concerned with the analytic and practical techniques necessary to improve the reliability/competitiveness of our products.

If you can secure the necessary support to attend 3 or 4 one day meetings a year, attend the symposium in January each year, are a member of IEEE Reliability Society and are interested in further details on how to join this select group on the management committee, please contact: V. R. Monshaw, 1768 Lark Lane, Cherry Hill, NJ 08003, (609)428-2342.

Free Proceedings

Your Reliability Society has a large number (over 300) of surplus copies of the 1992 IRPS and the 1993 RAMS proceedings on hand. We also have a small number (less than 30) of 1992 RAMS Proceedings.

Reliability Society members who did not get a copy of any of these and want one, may request a copy by writing the following address. Requests should identify the proceedings desired and confirm that the requester is a member of the Reliability Society. Requests will be filled only so long as supplies last. We have only the proceedings listed. Send to: Anthony Coppola, IITRI, 201 Mill Street, Rome, NY 13440-6916.

The Reliability Society will also honor requests by Academic Institutions for multiple copies of any of these proceedings for educational purposes, so long as supplies last. (e.g. We would be happy to provide a copy of a proceedings for every member of a class on reliability, if we have enough.) Individual Reliability Society member requests will have priority.

Electronic Bulletin Boards

Los Angeles IEEE Chapter
(818) 768-7644 300-2400 Baud (8N1)
Free Membership — (400+ members)
Meeting information, Jobline, Email, Video Tape Exchange Information, Shareware an Demos

Statistics Bulletin Board System
(316) 265-3036 1200-2400 Baud (8N1)
Free Membership
Statistics, Reliability

Computer Aided Logistics System (CALS)
(703) 321-8020 300-9600 baud 8N1
The CALS BBS is reached through this number to the National Technical Information Service (NTIS) BBS. Membership is free.

JPL/NASA Radiation Effects Data Bank
Test data on Single Event Effects and total-dose for electronic parts
BBS: (818) 393-4156, 1200 baud, 8N1
(818) 306-6920, 1200 baud, 8N1
FTP: radata.jpl.nasa.gov (137.79.11.2), Enter userid 'radata' & password 'guest'.
Sysop: Keyvan Eslami, (818)354-1715, email: keyvan_eslami@jpl.nasa.gov
After logon hit return and type RADATA in response username, no password required.

DOD Field Failure Return Program (FFRP) Reliability Bulletin Board
This Bulletin Board provides information concerning the DOD FFRP program as well as providing a vehicle for both commercial and government users to exchange ideas and information on component and system problems.
1200 baud or less
8 Data bits, no parity, 1 stop bit
(315) 339-7120, Access
(315) 339-7043, Questions

VLSI Design For Reliability

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Introduction and Problem Definition:

The need to include reliability analysis in the design of VLSI microelectronic circuits is evident from the requirement to reduce the time-to-market while maintaining high confidence that the circuits are free of end-of-life failure mechanisms. Reducing the time from concept-to-delivery is necessary to provide the best technology, the most up-to-date technology in today's and tomorrow's electronic systems. This helps assure the technological edge which is so critical to success. However, having the latest and greatest technology in the field is of little value if the systems are failing, and unavailable for use. The systems, and hence the microcircuits, must be reliable. The use of conventional approaches for assuring the reliability of microelectronic devices including burn-in and accelerated life test, are after fabrication approaches. If the circuit does not meet the performance, power or reliability specifications because of some inherent problem such as oxide breakdown, threshold voltage shift, or metal failures, a second or even a third pass at design and fabrication is necessary. This is extremely time consuming and expensive.

An integral part of the rapid prototyping of application specific IC's is the inclusion of maintainability, supportability, testability, test automation and diagnostics, and reliability into the design process. Incorporating reliability into a design from its inception is essential for shortening the time-to-market of electronic systems. Rome Laboratory has been sponsoring research in the development of automated design tools for the analysis of reliability in digital integrated circuits.

Reliability analysis during design can be thought of as being similar to design verification by circuit simulation during design. It helps assure that only a single pass is necessary at design/fabrication/ evaluation. The reduction in the number of passes reduces the time-to-market and should also reduce the cost of development. Including reliability optimization in the design phase also helps assure that reliability is not an afterthought, just something extra thrown in at the end; but rather is an integral part of the circuit. Making reliability part of the design should also enhance the reliability of the final product, reducing down time in the field, increasing the time between failures, and reducing the costs associated with field replacements and upgrades.

Design for Reliability (DFR) combines the physics of device failure with the details of the circuit design. This is because the major failure mechanisms (hot electron degradation and electromigration) depend strongly on the "stress" present in the circuit elements. For electromigration the stress is the current density, for hot electron degradation it is the substrate current. These characteristics depend greatly on the details of the design; which gates are connected to which metal conductors and where they are connected, when do the gates switch states, the switching speed, etc.

The physics of the device failure depends upon the specifics of the fabrication process, and must be measured via some test structure evaluation. The physics of failure must be combined with the specifics or details of the design. The designer must be given information about how the design is limited or about how he might modify the design to improve the reliability.

The Semiconductor Industry Association, at their 1993 semiconductor technology workshop, pointed out the need for reliability models, verification with reliability models, and synthesis with reliability models. The work shop conclusions stated [1]:

> "Design for reliability and an understanding of the relationships between process contamination and reliability must be included in a systems approach to reliability and quality."

They spoke of the needs in regards to power [1]:

> "The management of power is already a major design challenge. It will become, arguably the greatest obstacle to achieving the extremely dense logic chips with the high levels of activity necessary to continue the growth of computing capabilities.
> ...
> Design Techniques must be developed that incorporate power minimization as a primary objective. In addition physical design must be capable of predicting and avoiding electromigration in on-chip metallization, ensuring efficient distribution of power
> ...
> For system design, partitioning and technology decisions must be made with the objective of power minimization and management at all levels."

Clearly research and development is needed to bring reliability and power analysis into the design process, and to examine the effects of design decisions on reliability and power.

Design for Reliability at Rome Laboratory:

Rome Lab has, over the last several years, invested nearly $2M on research and development of methods for DFR and prototype tools. The contractual efforts with the University of Illinois at Urbana/Champaign (UI), have resulted in the development of several prototype Design For Reliability tools. The work sponsored by Rome Laboratory has been published extensively in technical reports, IEEE journals, conference proceedings etc. [2-27].

Reliability Tools:

The most general and widely available software tool for reliability analysis of microcircuits is the BErkeley Reliability Tool (BERT)[28]. BERT is a UC Berkeley development and performs reliability analysis by using the SPICE simulator to

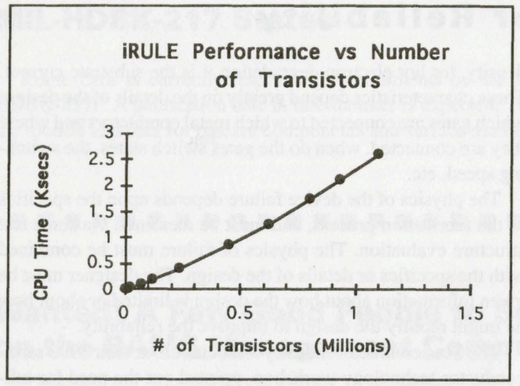

Figure 1. Computation complexity of iRULE [27].

determine the voltages and currents needed to compute conductor lifetimes and transistor degradation characteristics. BERT's usage of SPICE severely limits its applicability to VLSI circuits.

iPROBE [7,24] from UI, sponsored by Rome Laboratory, addresses the problem of VLSI devices with large numbers of inputs. It employs probabilistic simulation methods so that the AVERAGE effects over long periods of time and all possible input conditions are treated by the simulation. This approach at the present time has been restricted to digital combinational CMOS circuits and should be extended to sequential circuits. Probabilistic methods, which are geared to address the switching of the gates, have potential for addressing power dissipation and performance issues as well as reliability.

Another approach for analyzing VLSI circuit designs for susceptibility to hot electron degradation is the development of parametric macro-model based rules. This approach is being pursued by the University of Illinois and sponsored by Rome Lab. Designable parameters such as the input slew rate and the ratio of transistor width to capacitive load have been identified and incorporated into a prototype rule based reliability analyzer, iRULE [8,27]. These rules are similar conceptually to the geometric rules used in a "design rule checker", DRC. The algorithmic complexity of iRULE has been shown to be linear with respect to the number of transistors in a circuit[27], unlike simulation-based tools such as SPICE which have a super-linear cost-dependence on circuit size. This allows iRULE to run on large VLSI circuits in a reasonable amount of time.

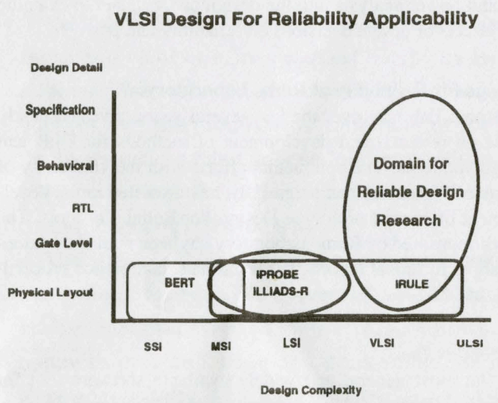

Figure 2. Design For Reliability Tools in relation to the world of design detail and design complexity.

Future Directions for DFR:

Future research in design for reliability should leverage off of previous research. Extending probabilistic simulation methods to deal with sequential circuits is a necessary step for addressing practical VLSI circuits. Rome Lab's FY-94 program includes research in this area. The rule based approach should be applied to additional failure mechanisms such as electromigration, Time Dependent Dielectric Breakdown (TDDB), and Electrostatic Discharge/Electrical Overstress (ESD/EOS). Integrating reliability analysis tools into a single unified system is also desirable. Research into the effects of the statistics of failure and the models and methods for extrapolating measured reliability characteristics to use conditions on specific designs is also necessary.

Research in VLSI DFR so far has been focused at low levels of design detail, gate and/or layout levels. Research is necessary to determine how to incorporate reliability analysis into all levels of the VLSI circuit design process. A unified top-down approach for reliability analysis of ULSI designs which maps high level reliability specifications, constraints and criteria into lower level design constraints needs to be developed. The constraints would impact design synthesis, standard/macro cell selection, floor planning and physical layout. Trade-offs between performance, reliability, area and power would be possible. This would bring reliability into the early phases of the design process, and make the inclusion of reliability an intrinsic characteristic of the device.

The problems associated with power, such as limiting power consumption, controlling power, and distributing power around ULSI chips, are more pressing to the semiconductor industry than reliability. Dealing with power distribution within the design flow, and enabling the trade-offs of power, reliability, area and performance is necessary. This entails bringing power estimation as well as reliability into the design synthesis and design optimization processes.

Summary:

VLSI Design for Reliability is important to Air Force, and DOD electronic systems, but has important implications for the microelectronic industry as a whole. This research is by its very nature dual-use. The need to reduce development time without sacrificing reliability is of particular importance to the DOD where the future trend is toward low volume acquisitions and extended system lifetimes. The microelectronics industry is also striving to minimize development time in its drive to get to market first. An investment in this area would not only benefit the DOD but the U.S. microelectronics industry as well.

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[1] Semiconductor Industry Association (SIA), Semiconductor Technology Workshop Conclusions, 1993.

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Conference Calendar

DATE & PLACE **CONFERENCE**

CALL FOR PAPERS

1995

8-10 March
Orlando, FL
USA

Second ISSAT International Conference on Reliability and Quality in Design

See advertisement on page 12.

The conference is sponsored by The International Society of Science and Applied Technologies (ISSAT) and PS Computers, Inc. with the cooperation of the IEEE Reliability Society, and the Quality Control and Reliability Engineering Division of IIE.

The conference is an international forum for presentation of new results, research development, and applications in reliability and quality in design. Papers may address any aspect of reliability and quality in design. Papers dealing with case studies, experimental results, or applications of new or well-known theory to the solution of actual reliability and quality problems in engineering design are of particular interest.

Submit four copies of papers (maximum 15 double-spaced pages) by 15 September 1994 to Program Chairman, Dr. Hoang Pham, Dept. Of Industrial Engineering, Rutgers University, P.O. Box 909, Piscataway, NJ 08855 USA, Tel: (908)445-5471, Fax: (908)445-5467, email: hopham@princess.rutgers.edu. Acceptance/rejection notification will be sent by 1 November 1994. Camera ready papers due 23 December 1994. All papers will be reviewed for merit and contents. Accepted papers will be published in the Conference Proceedings. Outstanding papers will be considered for publication in a special issue of the International Journal of Reliability, Quality and Safety Engineering.

3-6 April
Riviera Hotel
Las Vegas, NV
USA

International Reliability Physics Symposium

See advertisement on page 13.

CONFERENCES

1994

1-6 October
Phoenix, AZ
USA

1994 International Joint Power Generation Conference

The Reliability and Availability Committee (R&A) of the American Society of Mechanical Engineers (ASME) Power Division is requesting technical paper abstracts on the following suggested (but not inclusive) topics:

- Availability of Various Facilities
  - Repowering older power plant units and their resulting availability
  - Operating availability of independent power producers and cogeneration facilities
  - Impact of the Clean Air Act on availability
- Availability Evaluation
  - Economic benefits of improved availability
  - Data for availability modeling analysis
  - Determining availability of emerging technologies
  - Predicting, tracking or optimizing availability on a unit component level
  - Equipment reliability and availability specifications
- Reliability, Maintainability
  - Plant betterment programs and their impact on reliability
  - Reliability and availability aspects of on-line equipment performance monitoring
  - Practical application of statistical methods for reliability-related decision making
  - Practical applications of reliability centered maintenance concepts
  - Spare parts optimization

For information: Margaret A. Johnson, P.E., Paper Review Coordinator, ASME Reliability and Availability Committee, Houston Lighting & Power Company, 12301 Kurland Drive, Houston, TX 77034, Tel: (713)945-7783.

3-5 October
Washington, DC
USA

Third IASTED International Conference
Reliability, Quality Control and Risk Assessment

Sponsors:

- The International Association of Science and Technology for Development - IASTED
- The Reliability Division of The American Society for Quality Control -ASQC
- With the cooperation of the IEEE Reliability Society

Scope:

- Reliability
- Quality Control
- Maintainability
- Reliability based design
- Fault Detection
- Network Reliability
- Probability Assessment
- Decision Making
- Modeling
- Testing
- Software
- Trend Anaylsis
- Safety Management
- Physics of Failure
- Expert Systems
- Tutorials
- Simulation
- Quality Cost
- Concurrent Design
- Risk Management
- Security
- Aging of Systems and Components
- Applications
- Artificial Intelligence Applications
- Fault-tolerance
- Availability
- Algorithms
- Human Factors
- Statistics
- Surveys

For more information contact:
V. Selman, General Chairman, The American University, Department of Management, 4400 Massachusetts Avenue, Washington, DC 20016 USA, Tel: (202)885-1903, Fax: (202)885-1992.
Hoang Pham, Program Chairman, Rutgers University, Dept. of Industrial Engineering, P.O. Box 909, Piscataway, NJ 08855 USA, Tel: (908)932-5471, Fax: (908)932-5467, Email: hopham@princess.rutgers.edu

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4-6 October
Berlin, Germany

EDCC-1
First European Dependable Computing Conference

Organized By:

- Joint Technical Interest Group "Fault-Tolerant Computing Systems" of the GI, ITG and GMA, Germany
- AFCET Working Group "Dependable Computing", France
- AICA Working Group "Dependability in Computer Systems", Italy

Under the auspices of the Council of European Professional Informatics Societies (CEPIS)

In Cooperation With:

- GI Technical Interest Group "Dependable IT Systems"
- GI Technical Interest Group "Test and Reliability of Circuits and Systems"
- IFIP Working Group 10.4 "Dependable Computing and Fault-Tolerance"
- IEEE TC on Fault-Tolerant Computing
- EC-ESPRIT CaberNet Network of Excellence on Distributed Computing System Architecture
- EWICS Technical Committee on Safety, Reliability and Security (TC7)

Organizations and individuals are becoming increasingly dependent on sophisticated computing systems. In differing circumstances, this dependency might for example center on the continuity of the service delivered by the computing system, the overall performance level achieved, the real-time response rate provided, the extent to which catastrophic failures are avoided, or confidentiality violations prevented. These various concerns can be subsumed into the single conceptual framework of dependability, for which reliability, availability, safety and security, for example, can be considered as particular attributes.

This, the first European Dependable Computing Conference, aims to provide a venue for researchers and practitioners to present and discuss their latest research results and developments. Papers will be presented on theory, techniques and tools for the design, validation, operation and evaluation of dependable computing systems such as:

- Fault-Tolerant Systems and Components
- Safety Critical Systems
- Validation and Verification
- Secure Systems
- Test and Evaluation
- Dependable Software

EDCC-1 is the successor of two European conference series on fault tolerance and dependability as well as on aspects of testing and diagnosis. The first series, known as the "International Conference on Fault-Tolerant Computing Systems" was organized (from 1982 up to 1991) by the German Technical Interest Group "Fault-Tolerant Computing Systems". The other series, known as the "International Conference on Fault-Tolerant Systems and Diagnostics", was annually organized (from 1975 up to 1990) by Universities and academic research institutions in the former Czechoslovakia, Poland, Bulgaria and the former GDR. EDCC will be organized every two or three years in different European countries.
For more information contact: Dr. David Powell, LAAS-CNRS, 7 Avenue du Colonel Roche, 31077 Toulouse, France, Tel: +(33) 61 33 62 87, Fax: +(33) 61 33 64 11, E-mail: David.Powell@laas.fr

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14-17 November
Jerusalem Crowne Plaza Holiday Inn
Convention Center
Jerusalem, ISRAEL

Tenth International Conference of the Israel Society for Quality

This year's theme will be "Quality: The Star that Leads to a Better World." A commercial exhibition will take place within the framework of the conference. The conference will be conducted in English and Hebrew. Some simultaneous translations will be offered. Hotel accommodations within walking distance have been reserved by I.G.T. Group Travel Ltd. Registration fees are US$310 for 3 days (includes technical sessions, tutorials, book of proceedings, conference kit, welcome reception, lunch and coffee breaks), US$225 for 2 days (sessions only), US$150 for 1 day, and US$170 for tutorials only. For more information contact: Conference Secretariat, c/o ISAS International Seminars, P.O. Box 574, Jerusalem, 91004, Israel, Fax: 972-2-666154, Phone: 972-2-661356.

1995

16-19 January
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Washington, D.C.
USA

Annual Reliability and Maintainability Symposium

Theme: **Reliability and Maintainability — The Next Generation**

The changing role of the Reliability and Maintainability Engineer presents opportunities to examine our skills and capabilities, and explore new applications for our talents. As we become more visionary, we realize that we have skills which can be applied beyond the perceived limitation of our title "Reliability and Maintainability Engineer". We now move forward to "Reliability and Maintainability - The Next Generation."

Our challenge is to recognize and define how new and existing product assurance tools can be developed, applied and implemented to enhance and advance the assurance disciplines. The symposium is an excellent forum in which to share your experience and knowledge with your colleagues.

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THEME

The ISSAT International Conference on Reliability and Quality in Design is an international forum for presentation of new results, research development, and applications in reliability and quality in design. Papers may address any aspect of reliability and quality in design. Papers dealing with case studies, experimental results, or applications of new or well-known theory to the solution of actual reliability and quality problems in engineering design are of particular interest.

TOPICS OF INTEREST

- Reliability
- Modeling Analysis and Simulation
- Fault Tolerance
- Quality Assurance
- Optimization
- Software Reliability and Testing
- Quality Cost
- Maintainability and Availability
- Data Collection and Analysis
- Human Factors and Reliability
- Concurrent Engineering and Design
- Performance Analysis
- Experimental Design for Quality Control
- Software and Algorithms
- Methodologies for Quality Control
- Systems Design
- Safety-Critical Systems
- Risk Assessment Modeling
- Reliability Modeling and Testing
- Network Reliability
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All submitted papers will be reviewed for merit and contents. Accepted papers will be published in the Conference Proceedings. Outstanding papers will be considered for publication in a special issue of the International Journal of Reliability, Quality and Safety Engineering.

IMPORTANT DATES

Manuscript must be submitted no later than	September 15, 1994
Notification of Acceptance/Rejection	November 1, 1994
Camera Ready Papers Due	December 23, 1994

1995 International Reliability Physics Symposium

April 3-6, 1995 – Riviera Hotel – Las Vegas, Nevada USA

IEEE IEEE

CALL FOR PAPERS

The 1995 Symposium will continue emphasizing building-in reliability for VLSI devices and hybrid components during their design, manufacture and test. Papers are solicited that illustrate the incorporation of reliability physics, reliability engineering, out-of-spec design tolerance, fabrication, assembly, and manufacturing process control to improve system reliability. We encourage papers that address the identification of new microelectronic failure mechanisms, improve insights into existing failure mechanisms, and new or innovative analytical techniques. Papers demonstrating the reliability of advanced packaging techniques/concepts for multichip modules incorporating known good die are also requested.

YOUR PAPERS ARE SOLICITED ON:

- BUILDING-IN RELIABILITY:
  - Integration of reliability engineering with all elements of design
  - Establishing effects of input parameters on product reliability & control
  - Physical basis for design rules & concepts for minimizing jeopardy with experimental validation
  - Particulate control and its effects on reliability
  - Improved manufacturing techniques for wafer fabrication and assembly
- TESTING METHODOLOGIES FOR RELIABILITY, including:
  - In-process wafer fabrication control and assembly, monitors, and sensors
  - Novel test structures and materials
  - Evaluation at wafer level or after full or partial processing
  - Reliability modeling & field failure rate prediction
- ANALYZING FOR RELIABILITY:
  - VLSI failure mechanisms and models applied to:
    - dielectric integrity - electromigration - hot-carriers
    - low power/low voltage issues - corrosion - latchup/ESD/EOS
  - Optoelectronic failure mechanisms and models applied to:
    - LED/laser degradation - lithographic wave guide - burn-in/aging/wearout
    - passive element degradation - optical fiber issues - ESD/EOS
  - Assembly related failure mechanisms and models applied to:
    - bonding - surface mount issues - multichip packages
    - package integrity - thermomechanical stress - die overcoats
  - System related failure mechanisms, including:
    - automotive - consumer - military & aerospace
  - Failure analysis techniques: new, advanced, & simplified
  - Analytical instruments & techniques
  - Computer-Aided Reliability (CAR) applications & simulation with experimental validation

SUBMISSION DEADLINE: Received no later than September 23, 1994

Please submit 20 copies of both a one page 50-word abstract, and a two-page summary (including figures) that states clearly and concisely the specific results of your previously unpublished work, why the results are important, and how the results relate to prior work. Authors should specify in their cover letter one of these categories: 1. BIR, 2. Packaging, 3. Dielectrics, 4. Failure Analysis/ESD/Latch-up, 5. Hot Carriers, 6. Devices & Process, 7. Compound Semiconductor and Photonics, 8. Metalization, 9. Other. The 20 copies of the abstract and summary must be either on 8-1/2 by 11-inch or A4 paper and include the title of the paper, and the name, affiliation, complete return address, telephone and telefax numbers, and **e-mail address, if available,** for each author. Line drawings, key references, and coarse halftones may be included, but please no continuous-tone photographs. **Submissions should be post or express mail** rather than telefax, because of legibility after subsequent duplication. Please allow three weeks for acknowledgment of your submission. Contact the Technical Program Chair if not received in this timeframe. A limited number of late papers reflecting **important last-minute** developments will be considered on a space available basis. Abstract and summary must be received no later than December 1, 1994. Please note that the most common causes for rejection are: incomplete data, prior publication, and insufficient novelty, significance, or relevance to the Symposium.

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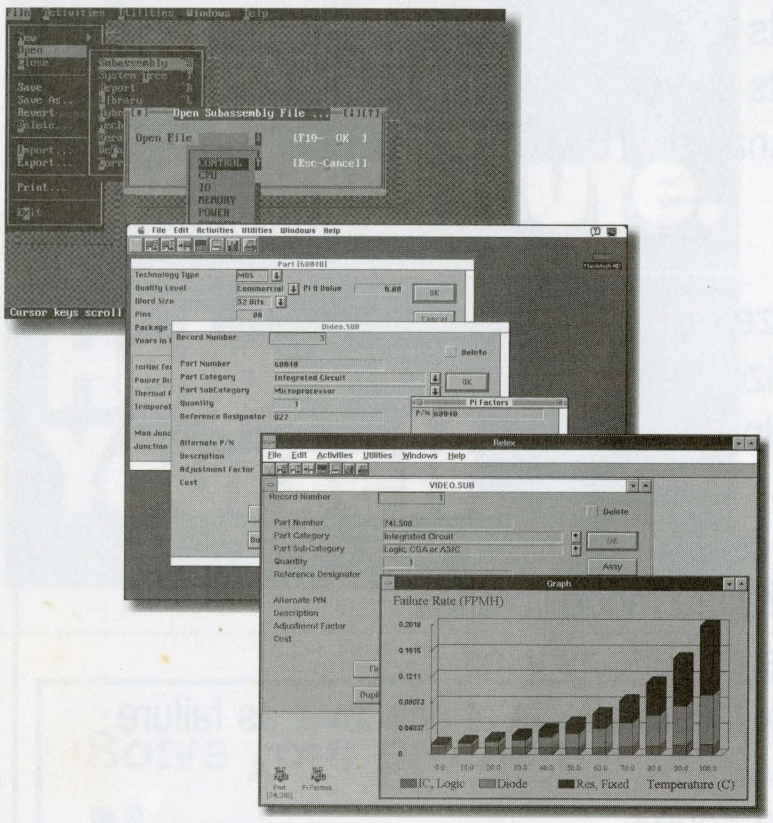

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