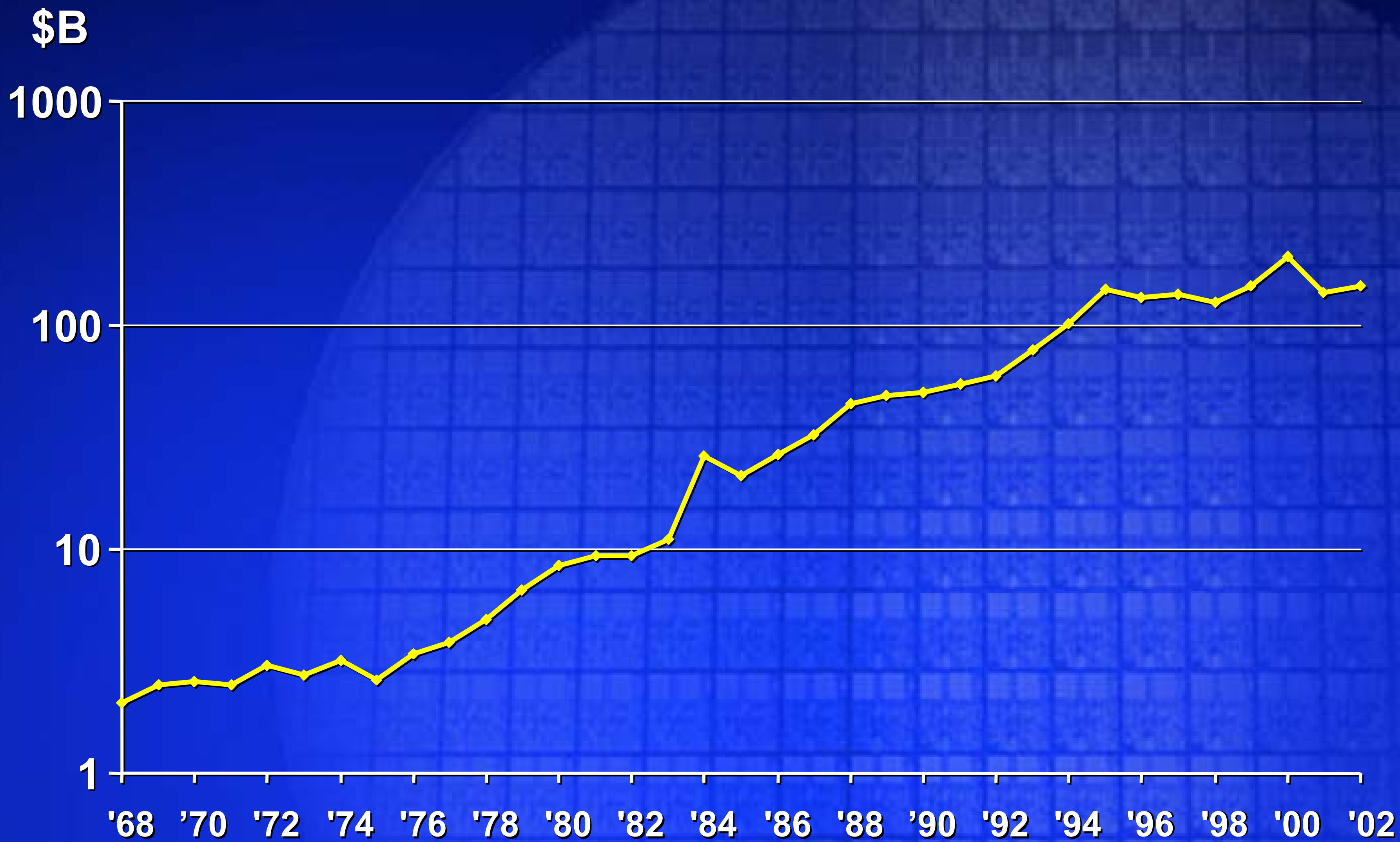
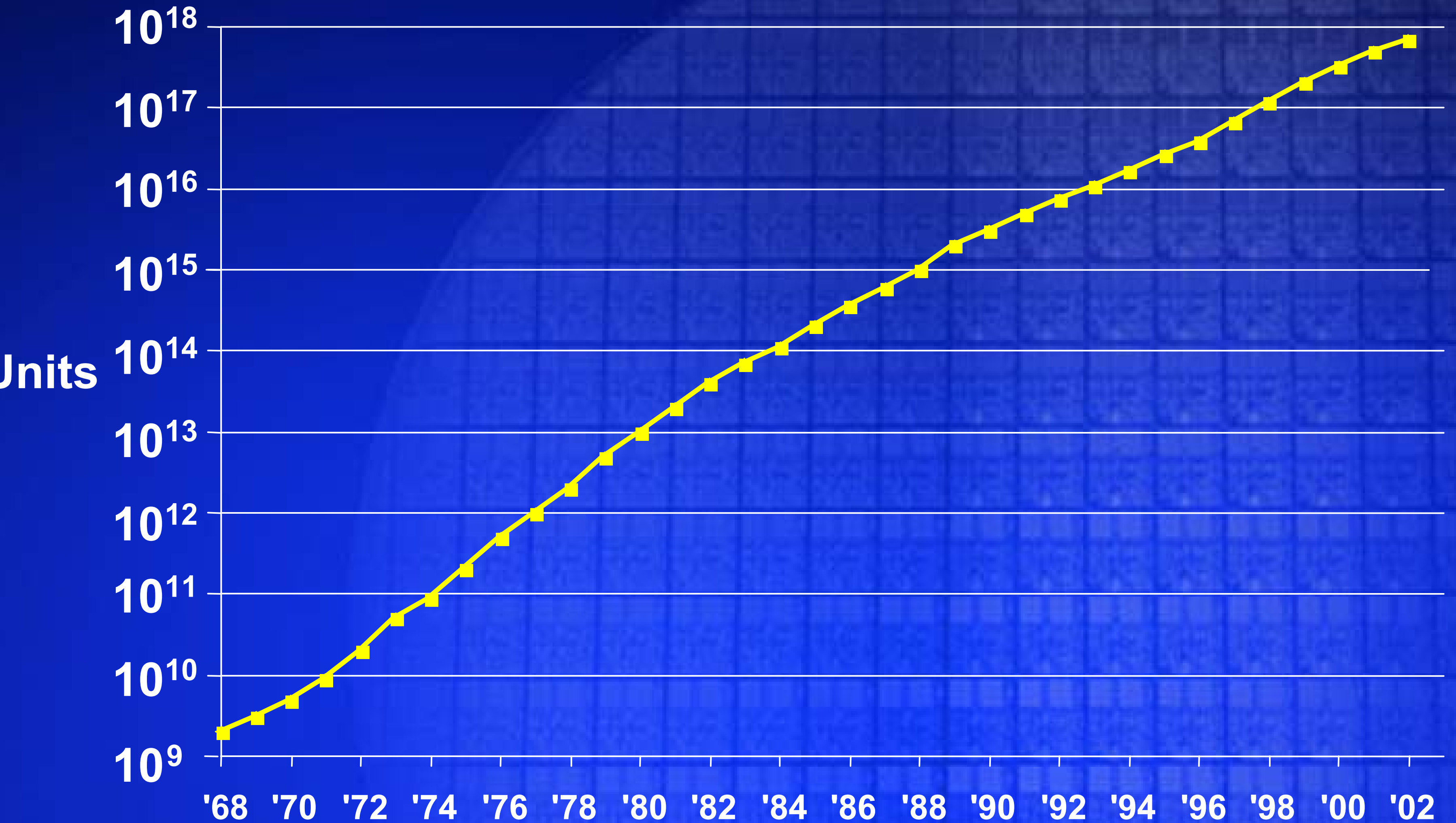
NO EXPONENTIAL IS FOREVER . . .

Gordon E. Moore

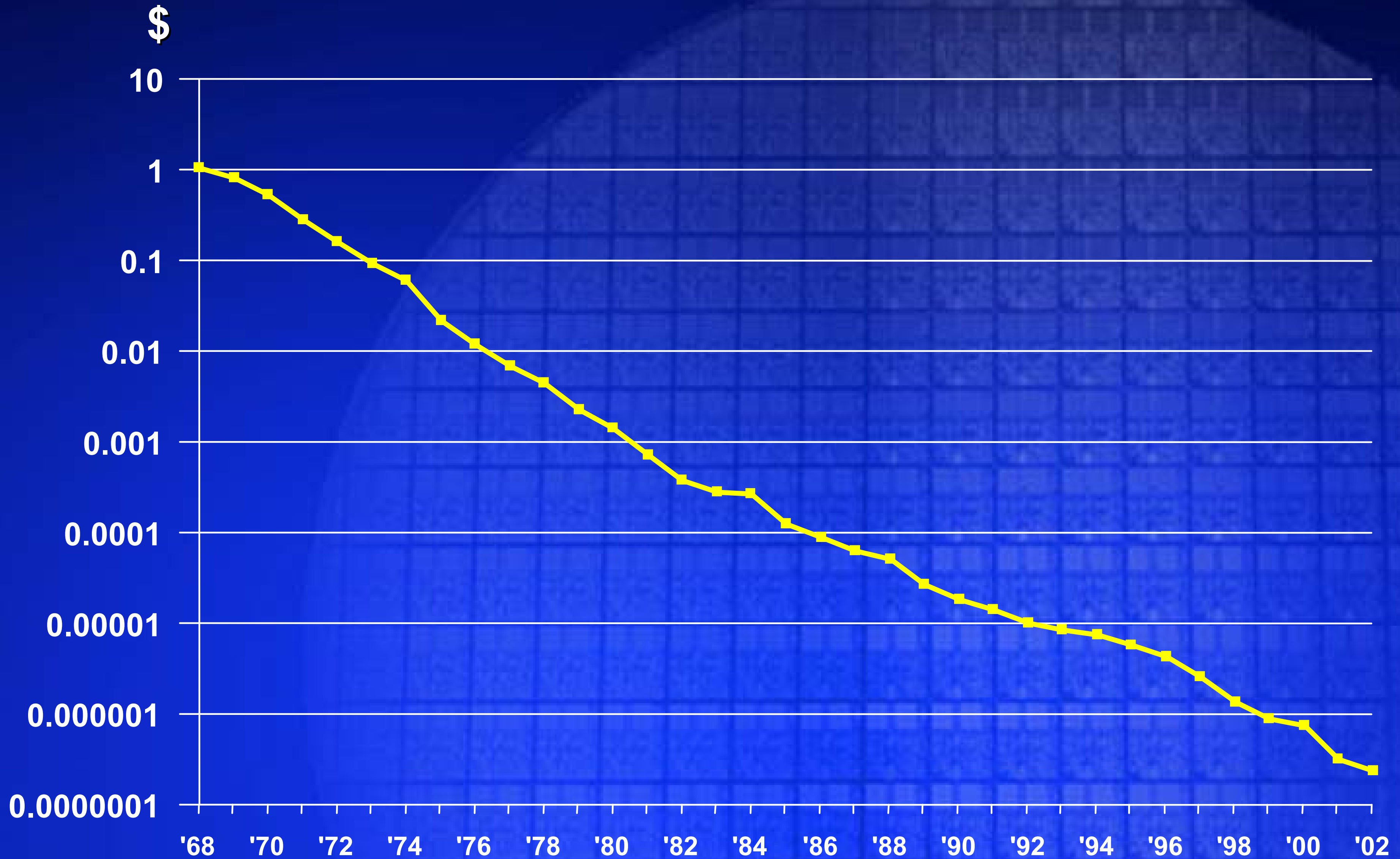
Worldwide Semiconductor Revenues



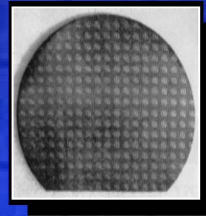
Transistors Shipped Per Year



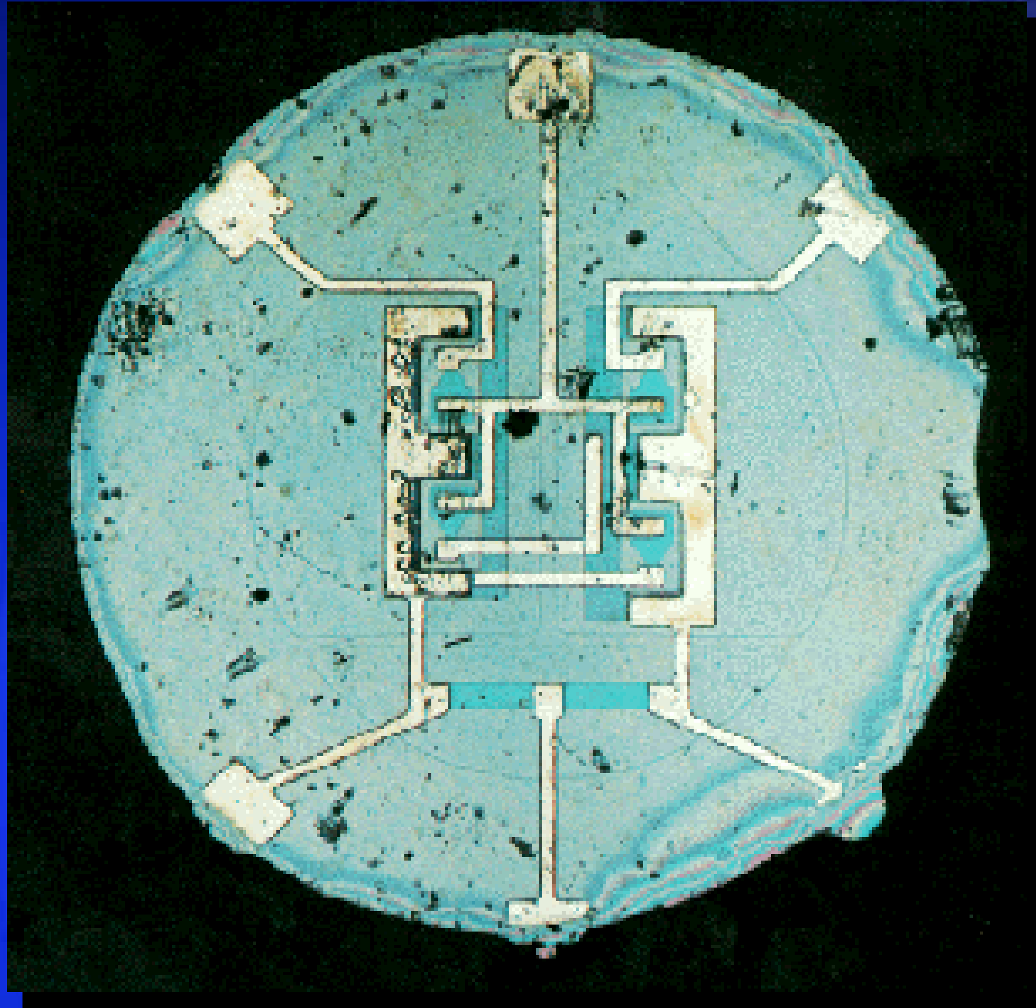
Average Transistor Price By Year



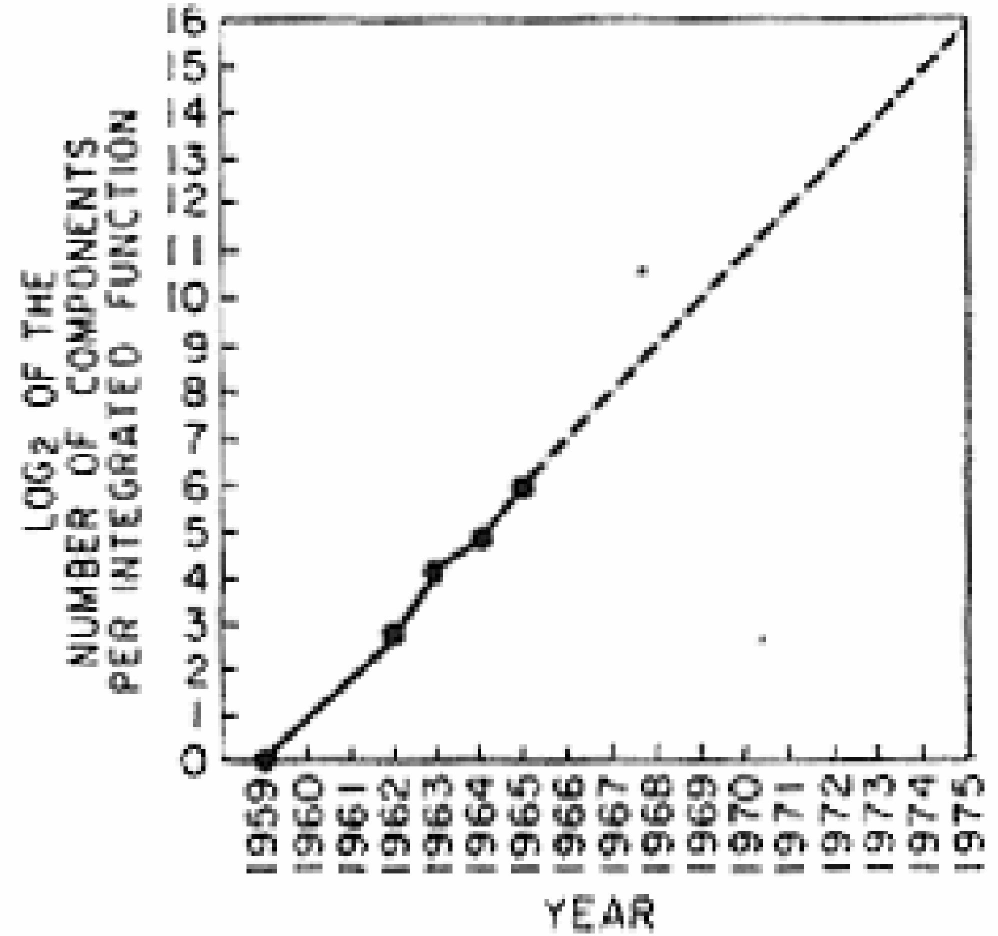
1” Wafer Of Planar Transistors, ~1959



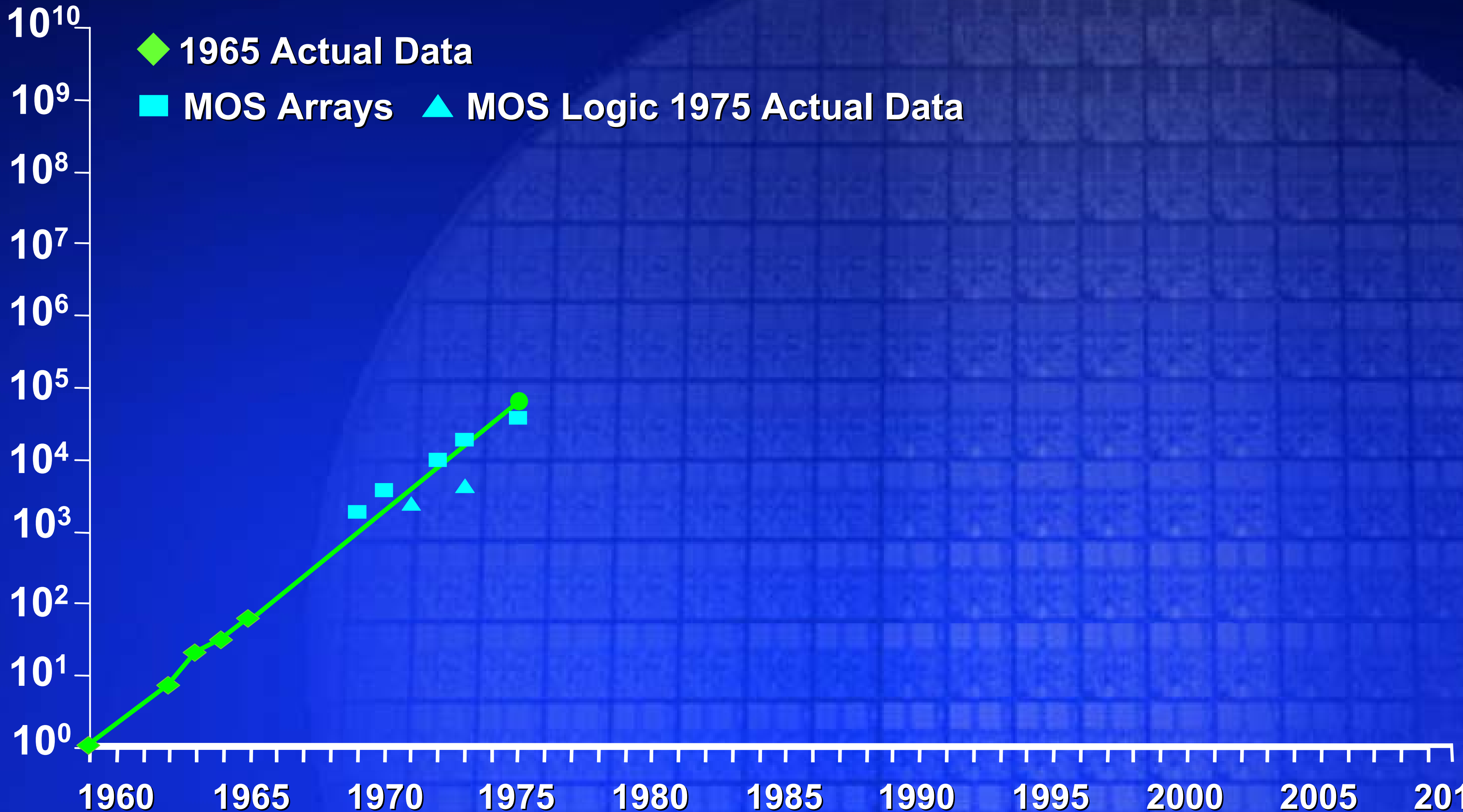
The First Planar Integrated Circuit, 1961



1965 Transistor Projection

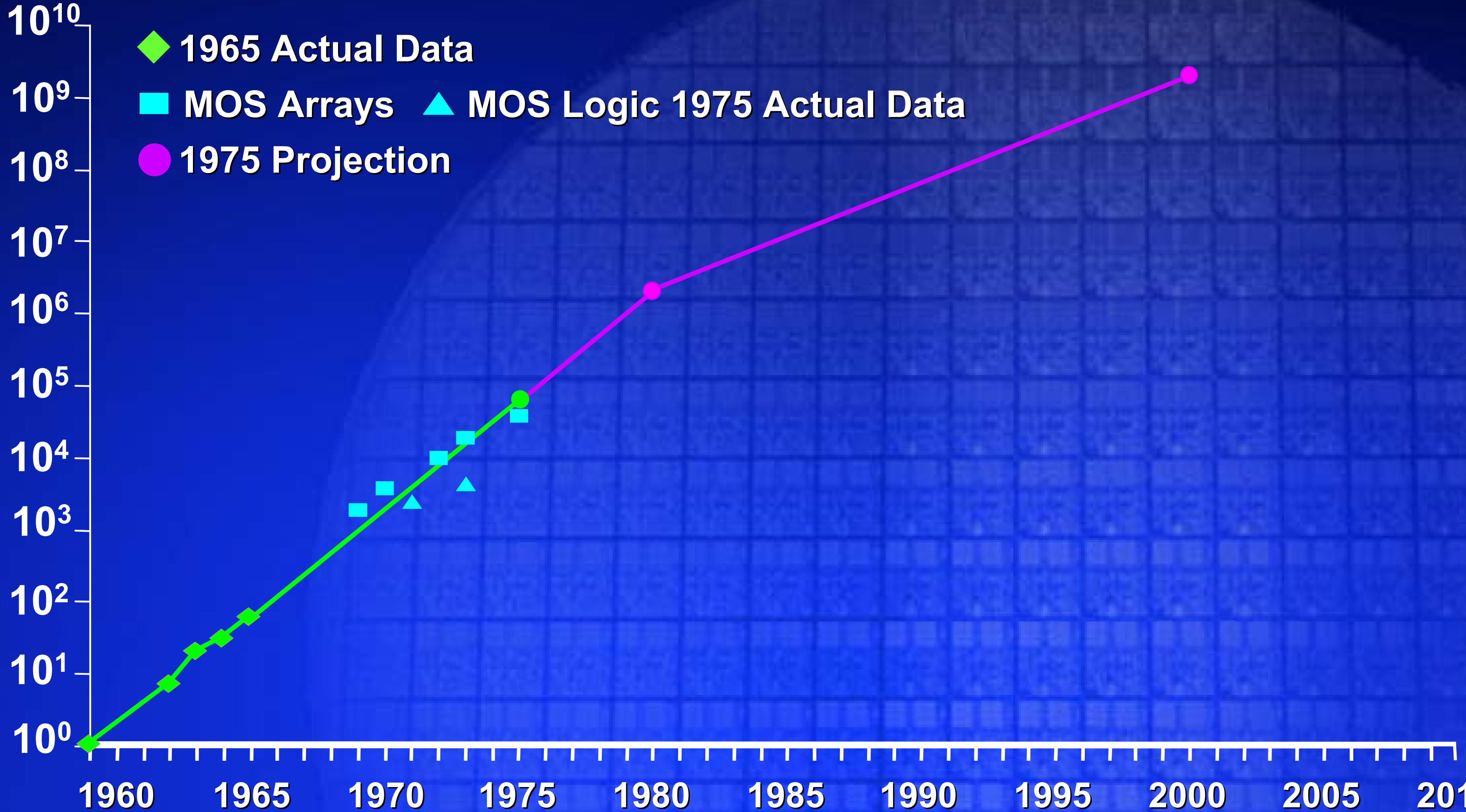


Integrated Circuit Complexity

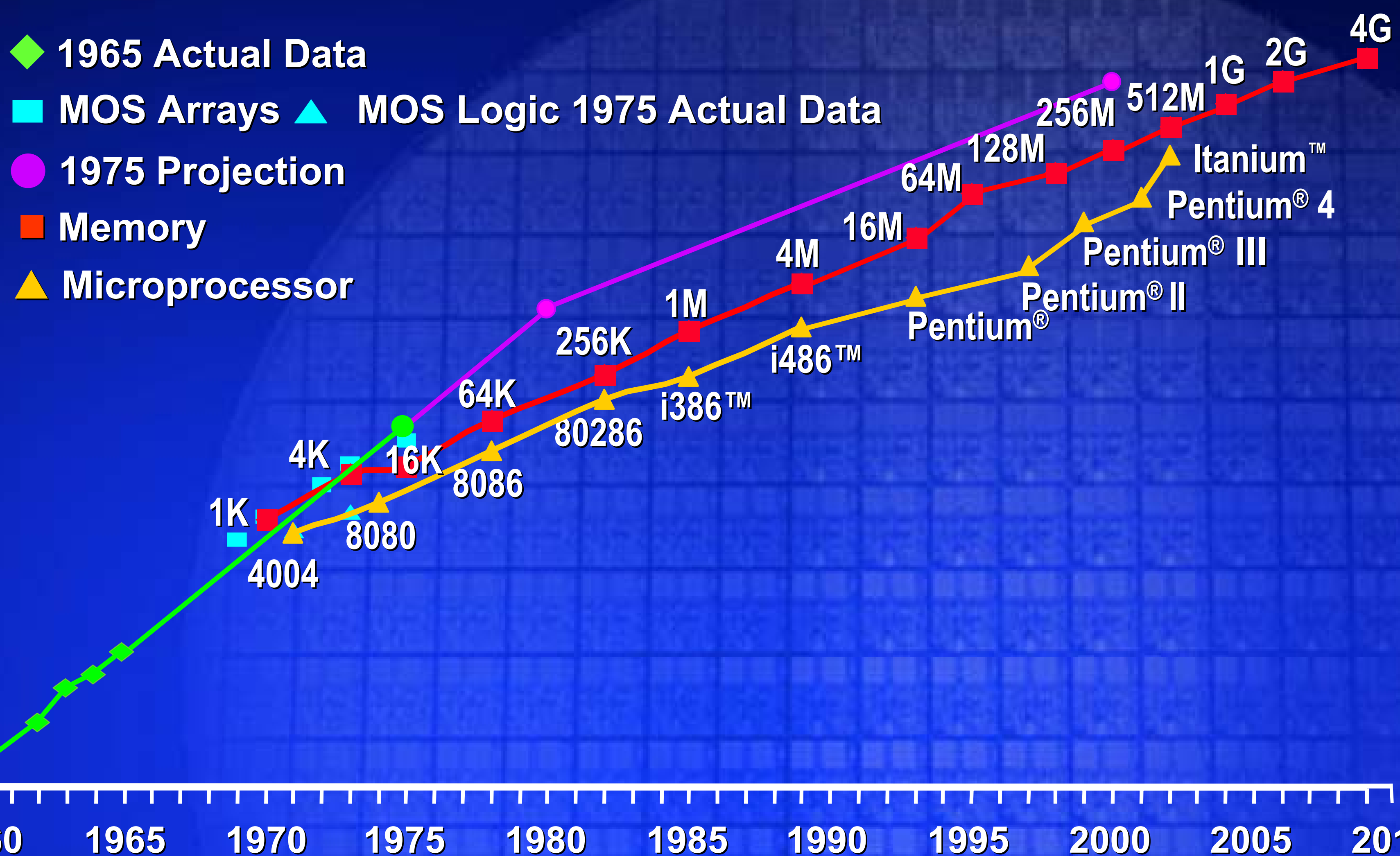


Integrated Circuit Complexity

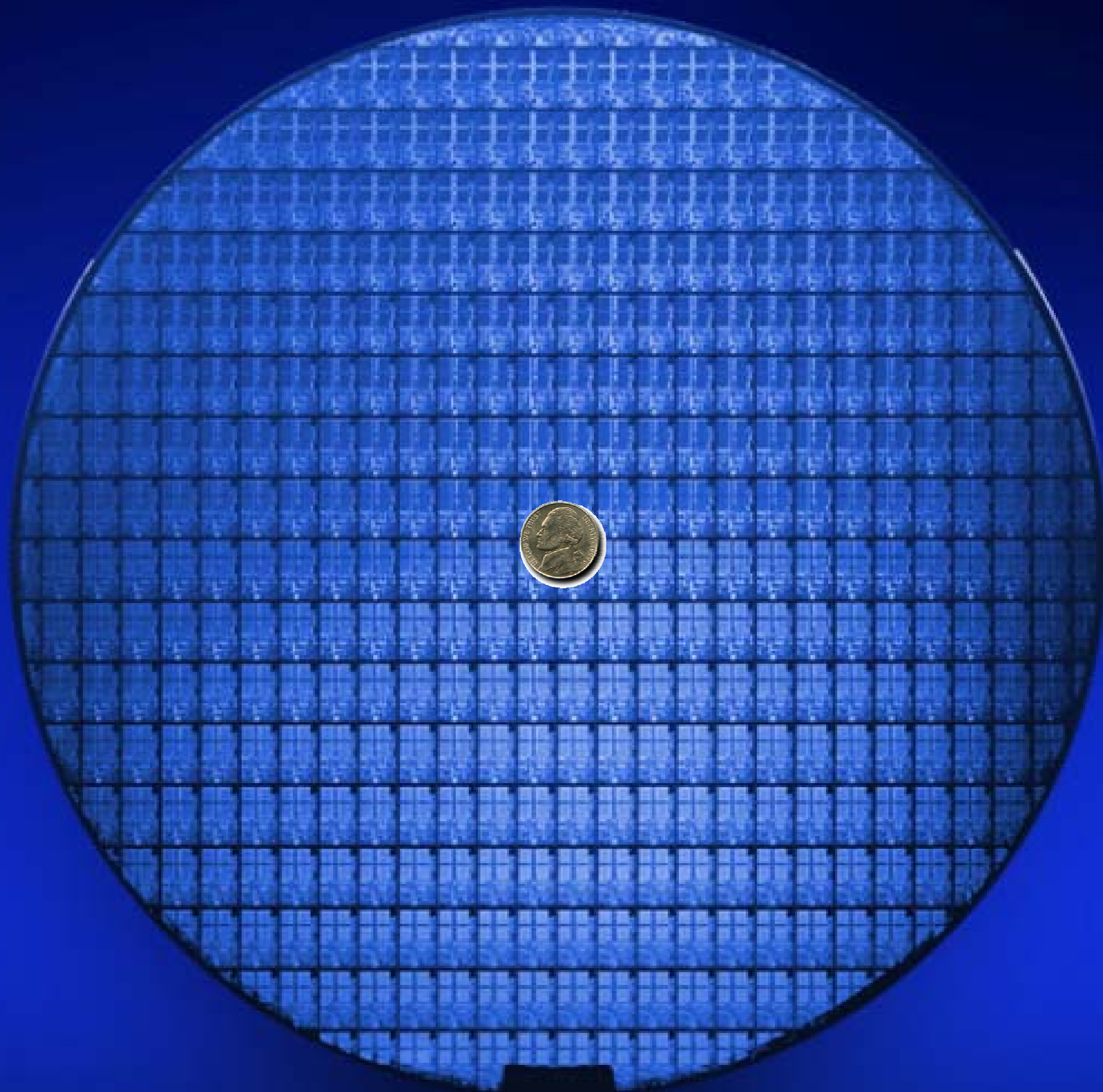
Transistors
Per Die



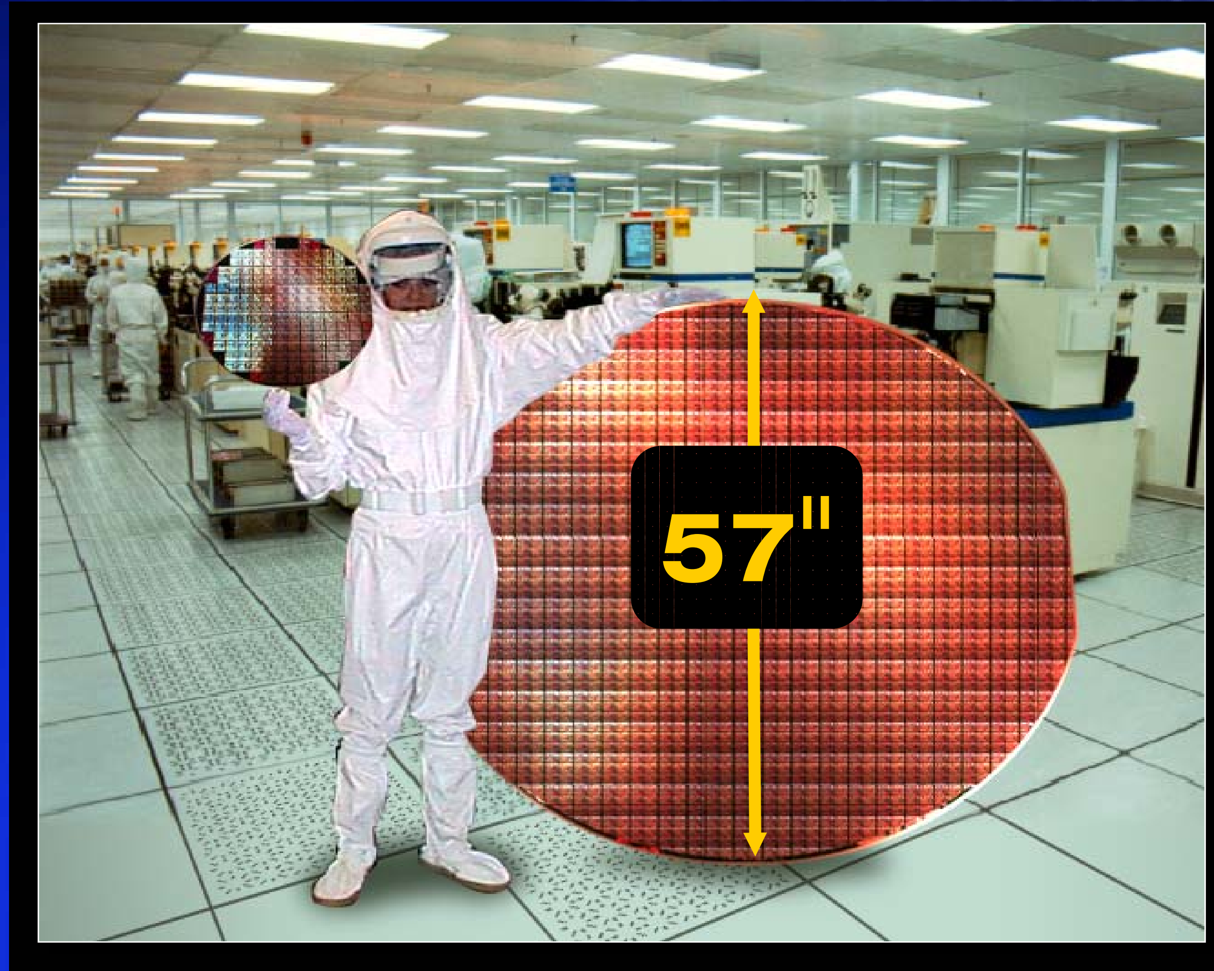
Integrated Circuit Complexity



300mm Wafer

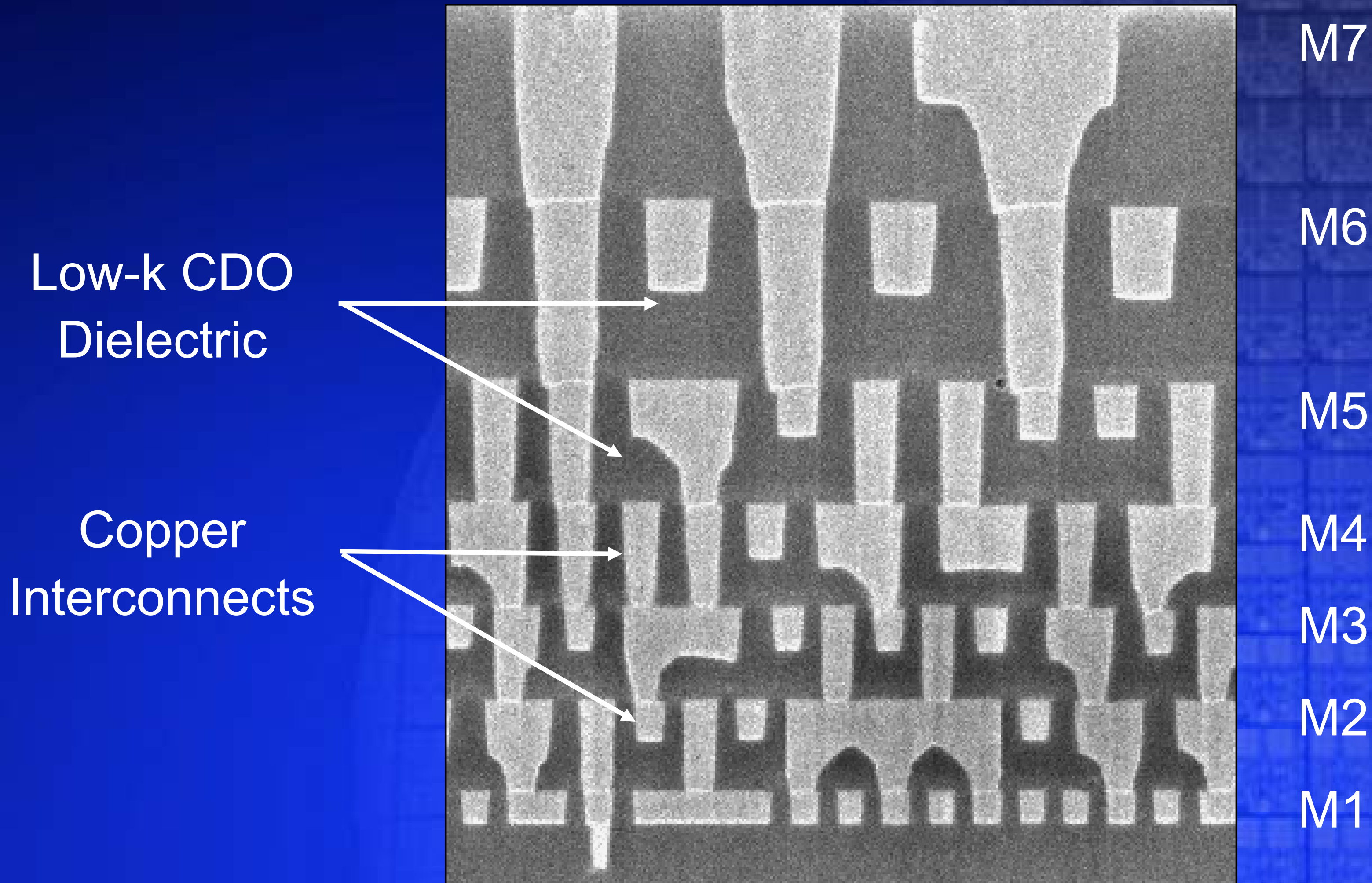


Projected 2000 Wafer, circa 1975



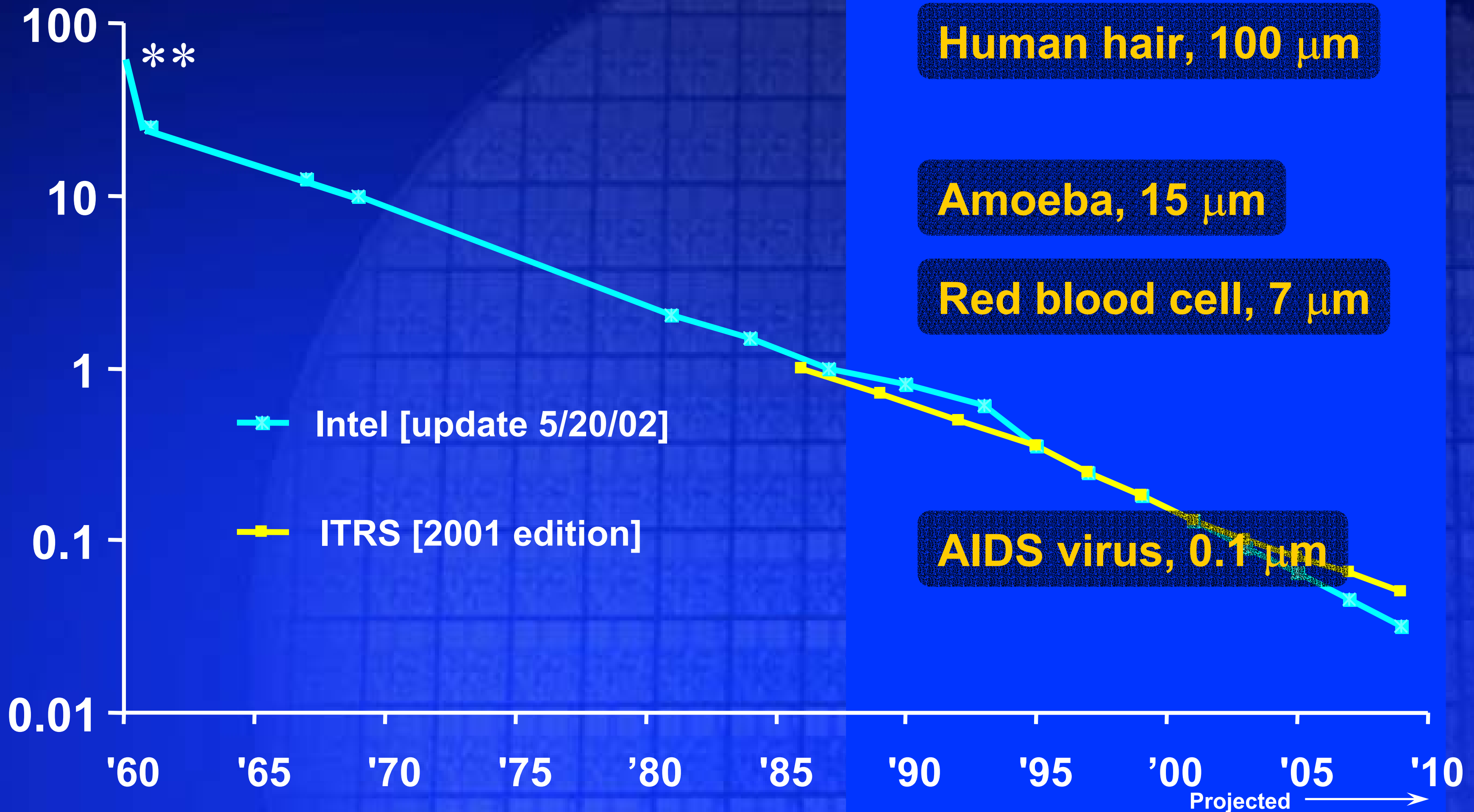
Moore was not always accurate

90 nm Generation Interconnects



Combination of copper + low-k dielectric now meeting performance and manufacturing goals

Minimum Feature Size



** Planar Transistor; remaining data points are ICs.
Source: Intel, post '96 trend data provided by SIA International Technology Roadmap for Semiconductors (ITRS)

1 μm^2 SRAM Cell

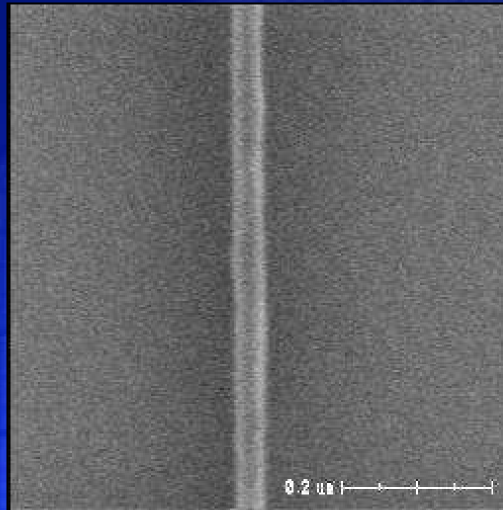
P501 Contact
1978

P1262 SRAM Cell
2002

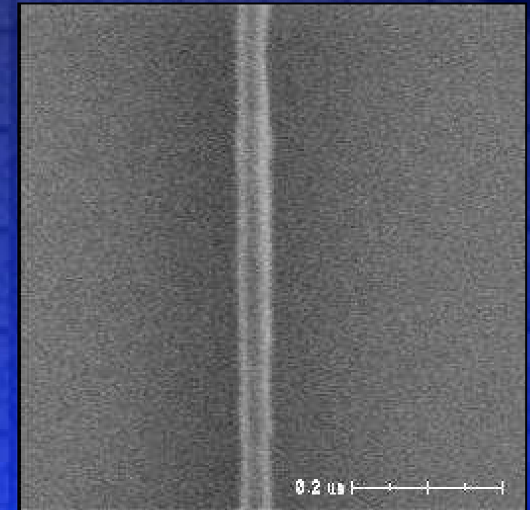
1 μm

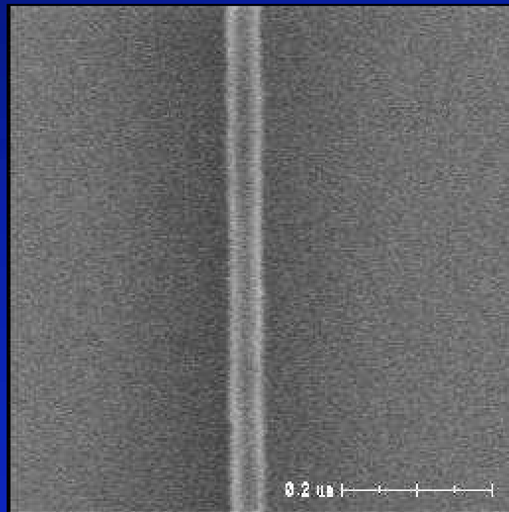
50nm Resist Lines With 193nm Light

-0.2um focus

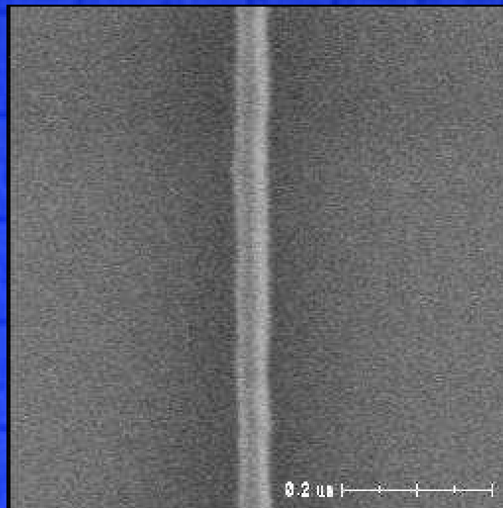


-0.3um focus

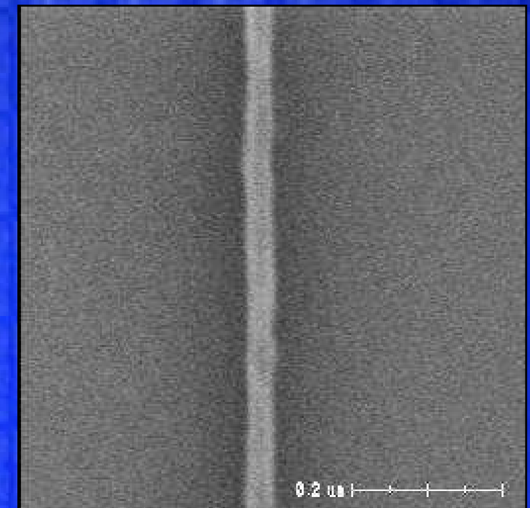




"best focus"



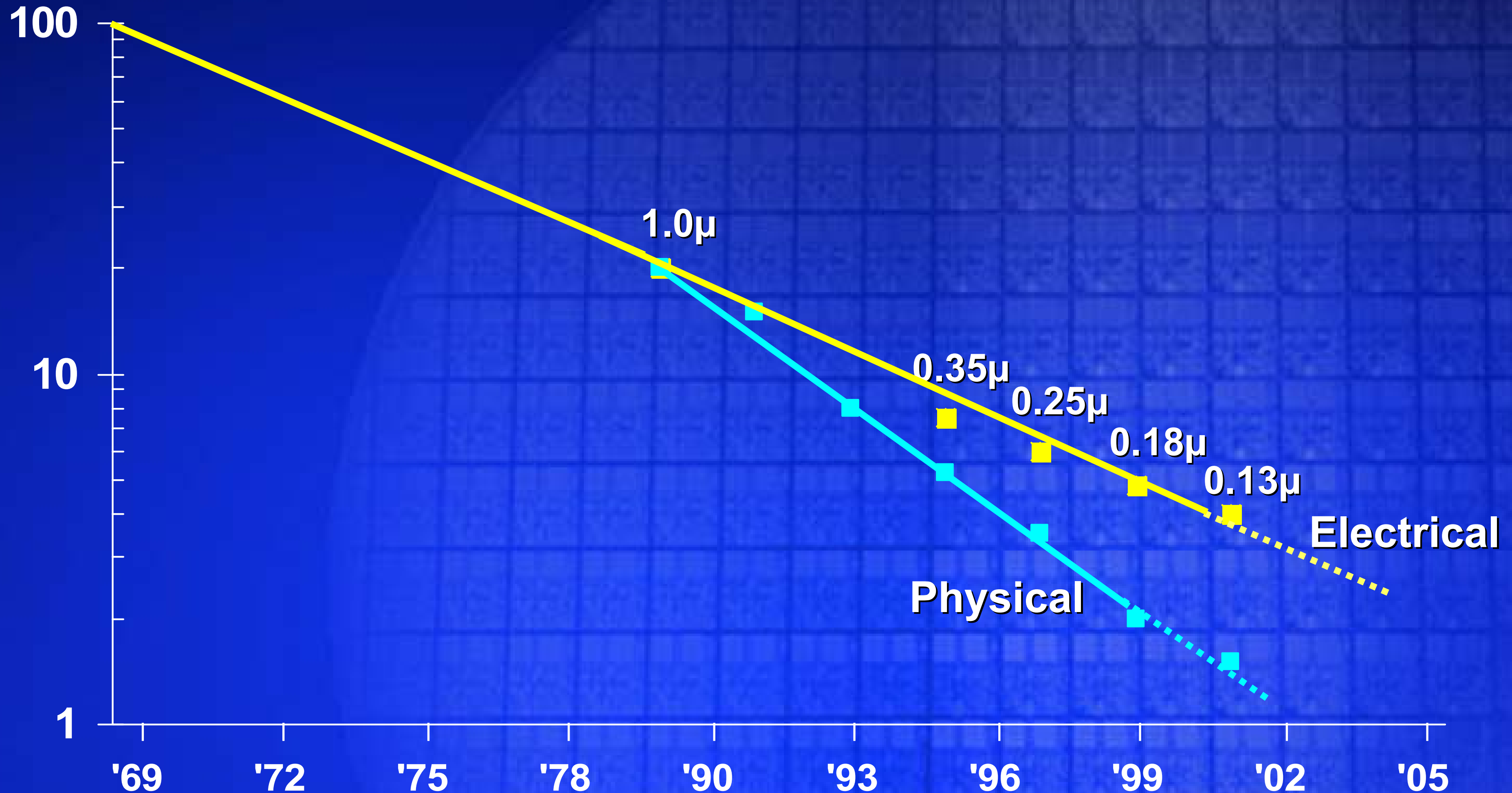
+0.2um focus



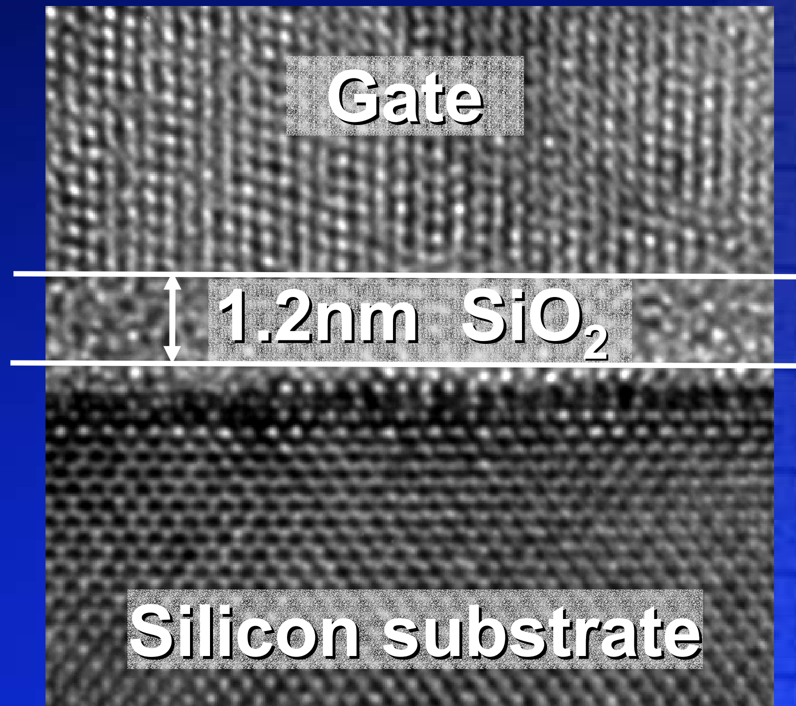
+0.3um focus

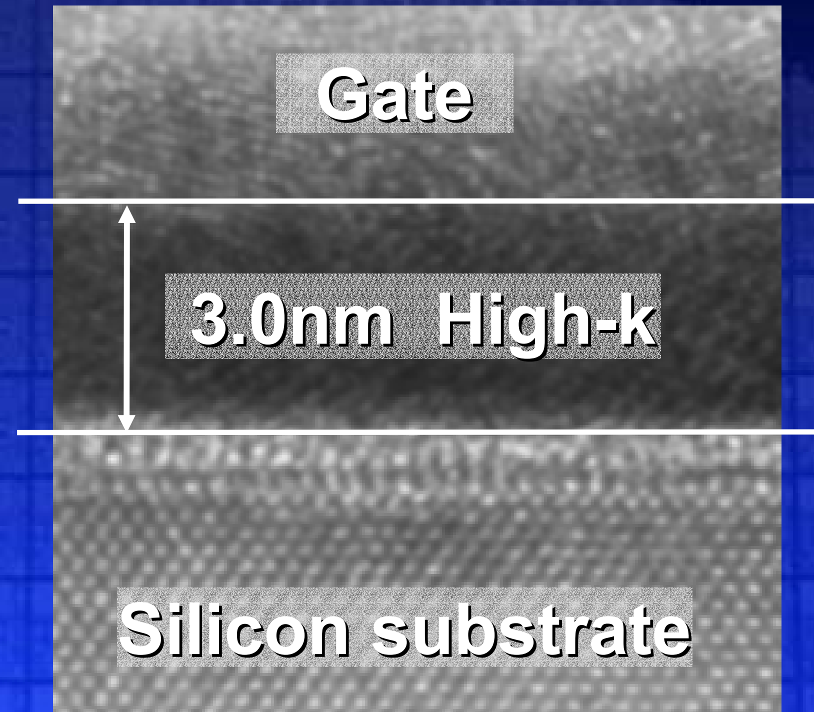
193nm Step and Scan Production Tool

Minimum Insulator Thickness vs Time



High K for Gate Dielectrics



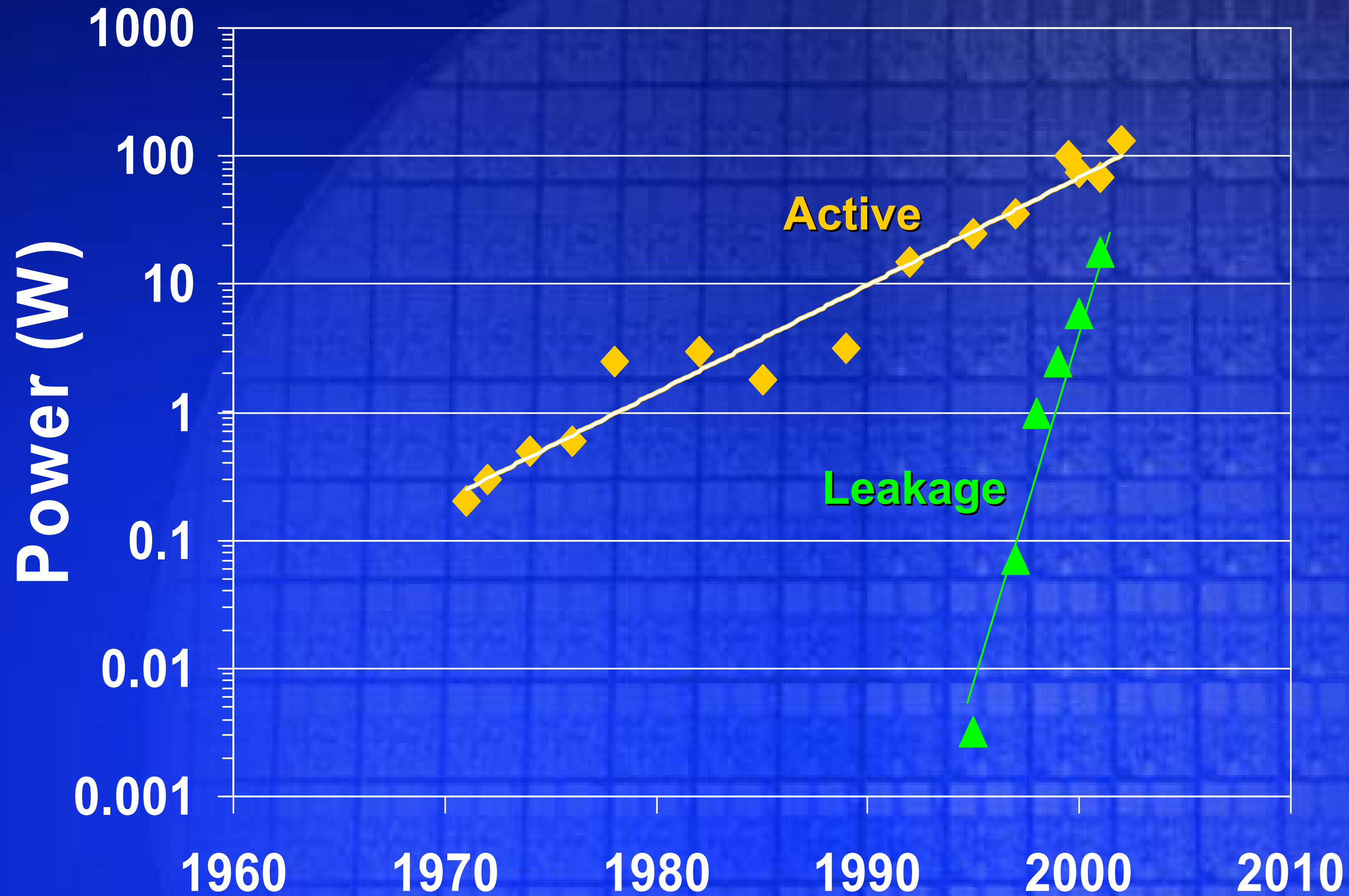


	90nm process	Experimental high-k
Capacitance	1X	1.6X
Leakage	1X	< 0.01X

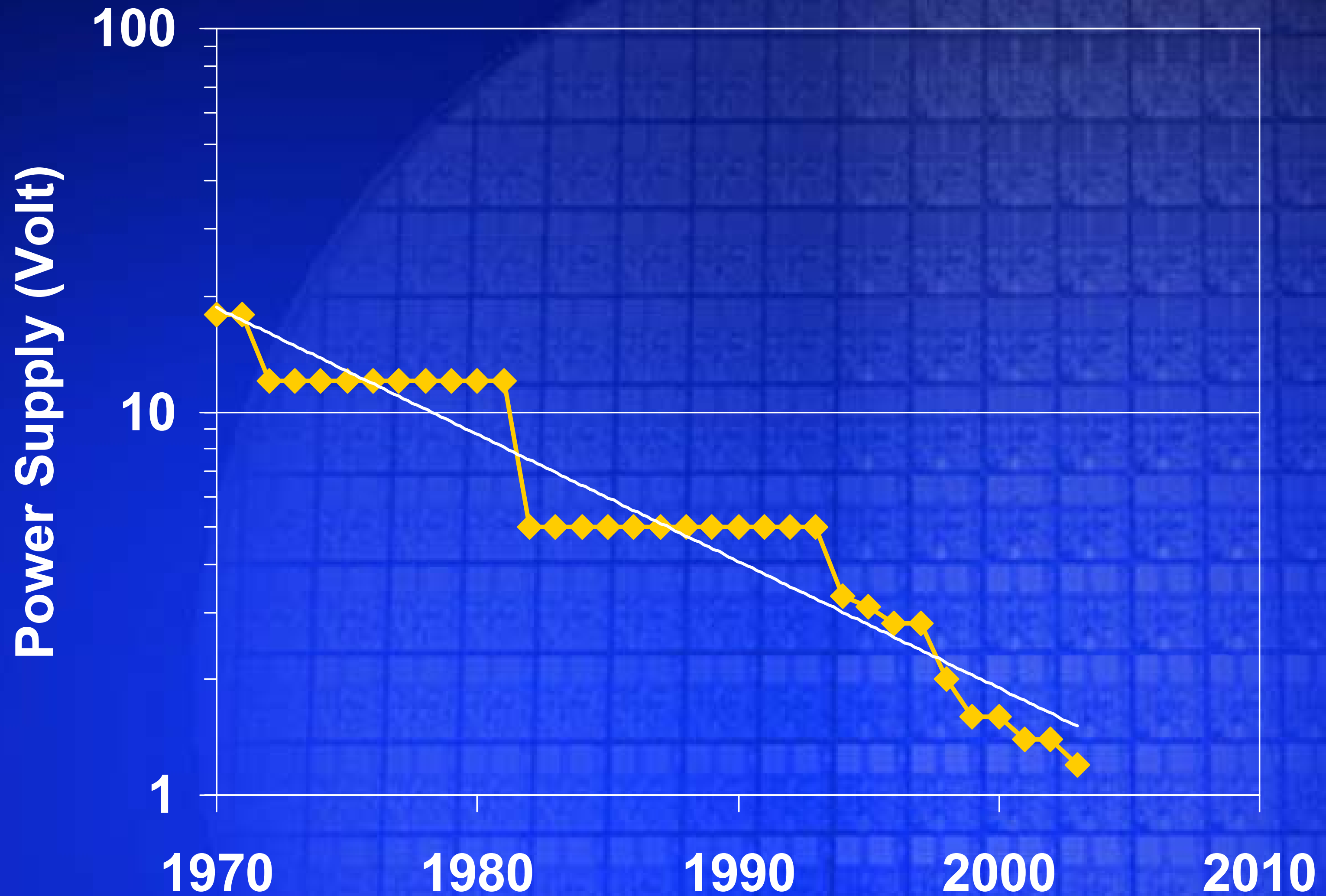
Source: Intel

Processor Performance (MIPS)

Processor Power (Watts) - Active & Leakage



Processor Supply Voltage

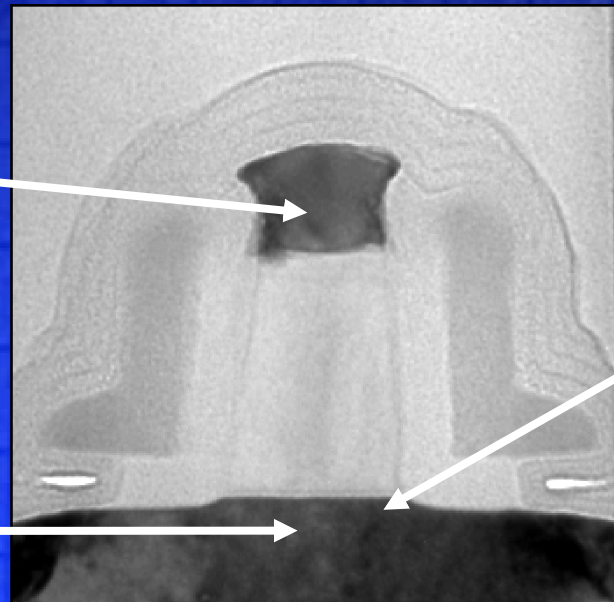


New Materials and Device Structures Extending Transistor Scaling

Changes Made

<u>Gate</u>
Silicide Added

<u>Channel</u>
Strained Silicon



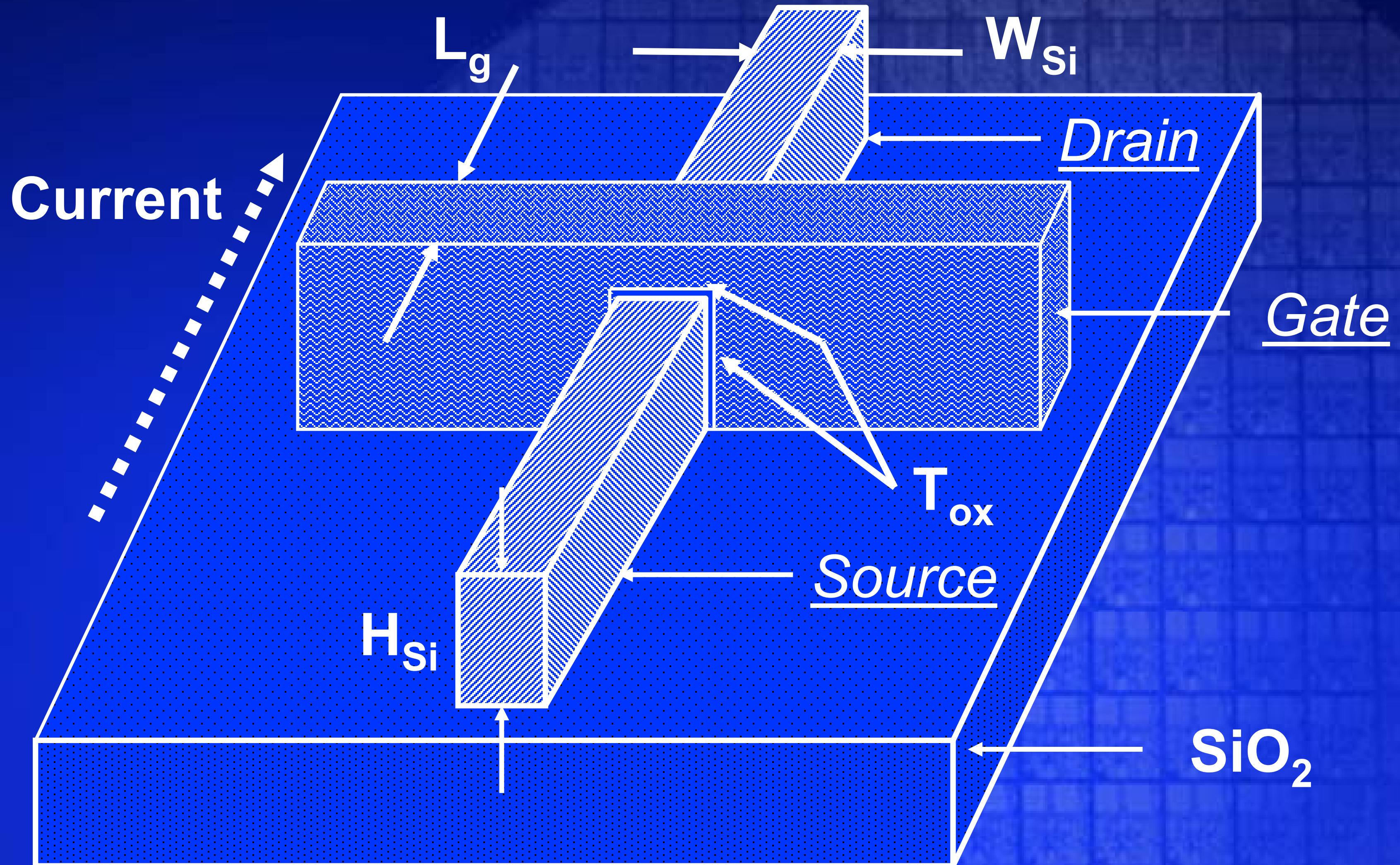
Transistor

Future Options

High-k Gate Dielectric

New Transistor Structure

Tri-Gate Transistor Structure



Technology Generations to Come

Double the Density
Reduce Line Width by 0.7x

130nm→90nm→60nm→45nm→30nm→?

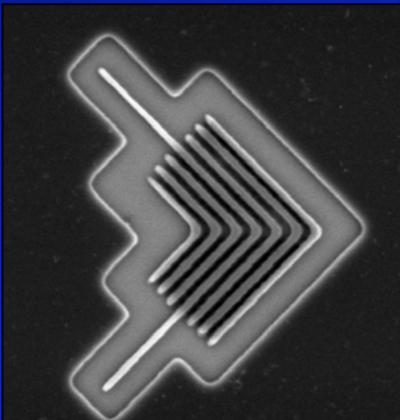
2 or 3 years between generations

∴

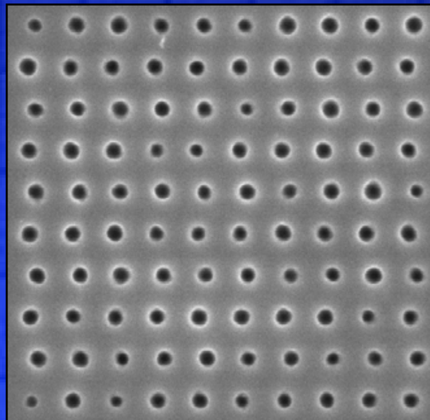
~10 ± 2 Years

EUV Printed and Etched Lines

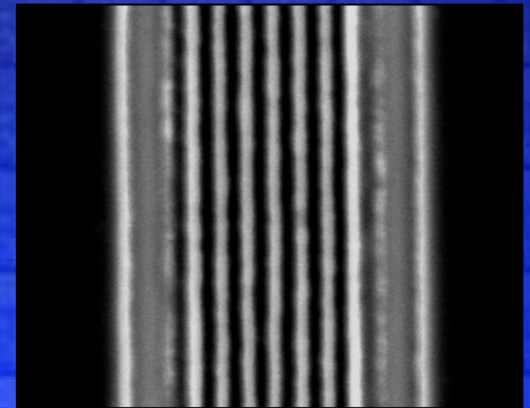
100 nm, k_1 = 0.75



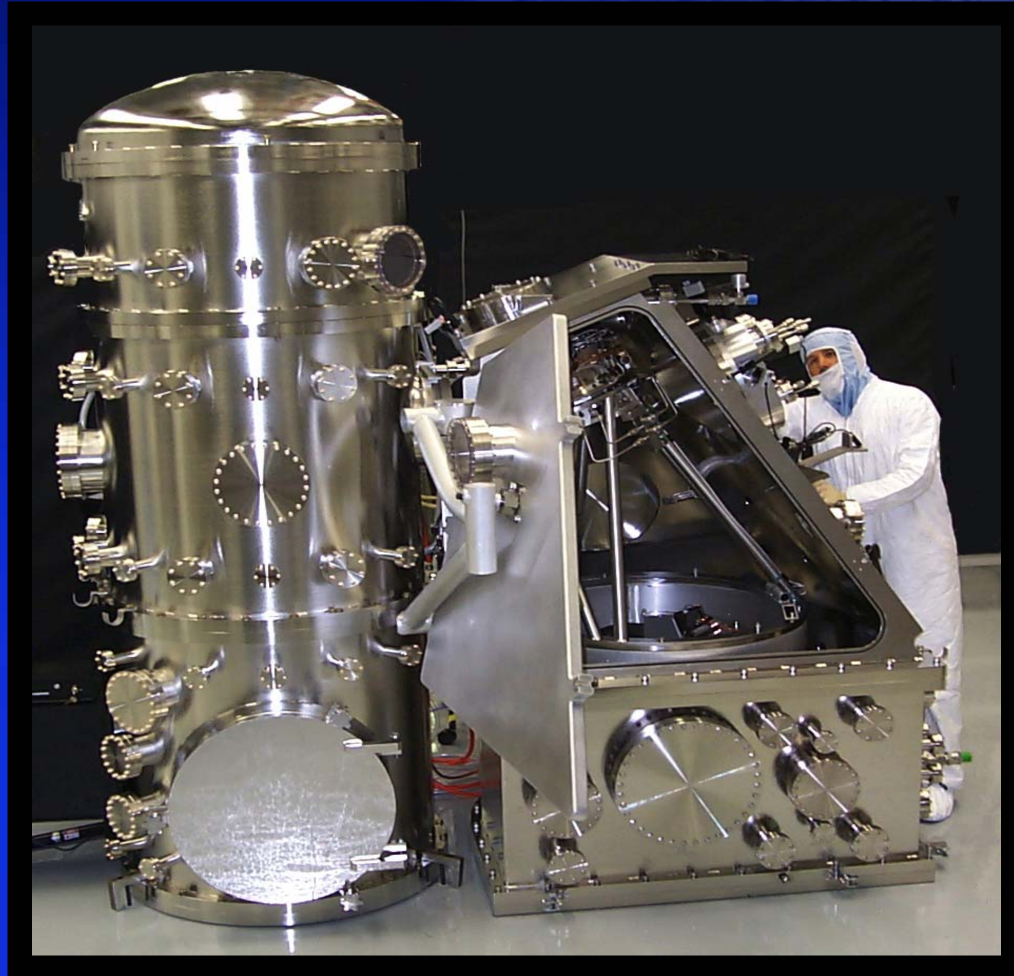
80 nm, k_1 = 0.60



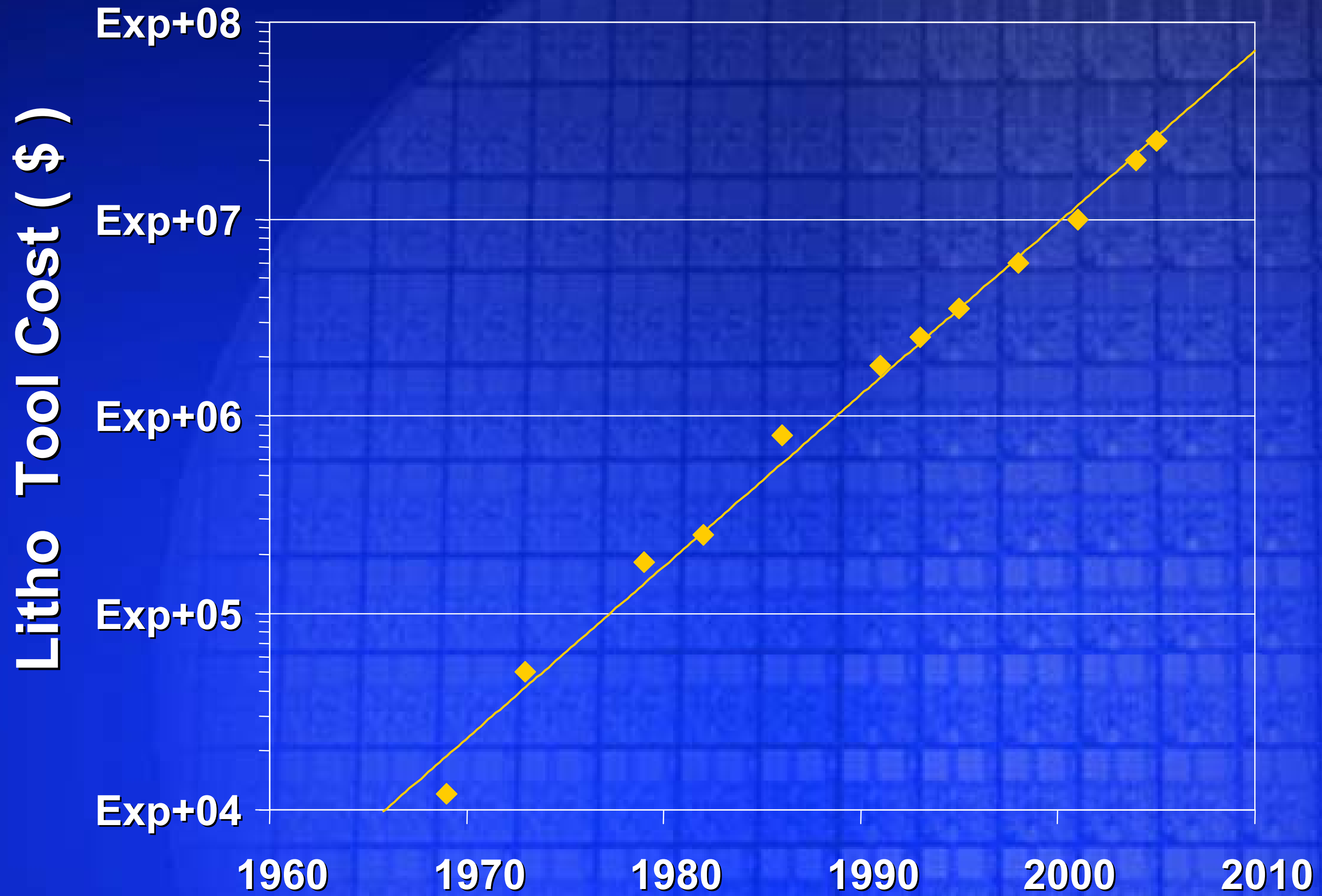
50 nm dense, k_1 = 0.37



Extreme Ultraviolet (EUV) Lithography



Lithography Tool Cost ($)



NO EXPONENTIAL IS FOREVER . . .

BUT

WE CAN DELAY “FOREVER”